

Question Paper Code : 55385

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2011.

Seventh Semester

Electronics and Instrumentation Engineering

EI 2403 — VLSI DESIGN

(Regulation 2008)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is the advantage of CMOS over PMOS and NMOS technology.
2. Write the reasons for the limited load driving capabilities of MOS transistors.
3. Draw the stick diagram of a p-well CMOS inverter.
4. Why BiCMOS technology does not offer speed advantage in applications like ALU and ROM subsystems?
5. Draw a 2 to 1 multiplexer using NMOS transistors.
6. What are the advantages of AOI implementation of two level logic functions?
7. What are the benefits of implementing combinational logic functions using PLAs when compared with ROMs?
8. Give the applications of dynamic logic arrays.
9. Write the VHDL entity for a full adder.
10. Write a VHDL code for a D flipflop.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the operation of NMOS enhancement and depletion mode transistors with neat diagrams. (6)

- (ii) Enumerate the different steps involved in twin tub CMOS fabrication process with neat diagrams. Compare the performance of CMOS inverters fabricated using twin tub process and n-well process. (7 + 3)

Or

- ✓ (b) (i) Explain the characteristics of NMOS transistors with necessary equations for the drain current in the different regions of operation and necessary diagrams.

- (ii) Explain the second order effects. (8)

12. (a) (i) Draw and explain briefly the lambda based design rules for NMOS and CMOS transistors.

- (ii) Give a brief note on steering logic. (6)

Or

- (b) Draw and explain the operation of

- ✓ (i) An NMOS and a CMOS superbuffer (5 + 5)

- (ii) BiCMOS two input NAND gate. (6)

13. (a) (i) Describe the operation of a dynamic CMOS three input NOR gate with necessary diagrams. (8)

- ✓ (ii) Explain the operation of a four input tally circuit designed with pass transistors. (8)

Or

- (b) (i) Explain the operation and implementation of a basic four bit adder, Describe the different approaches of improving the speed of the adders. (8)

- (ii) Draw and explain the operation of four bit multiplier array with necessary diagram and expressions. (8)

14. (a) (i) Explain the NMOS NOR-NOR PLA realization with a neat stick diagram. (8)
✓ (ii) Draw and describe the structure of clocked PROM and PAL. (8)

Or

- (b) (i) Describe the implementation of FSM using PLA and also describe the importance of PLA/FSM in VLSI. (8)
(ii) Explain the logic cells and interconnects used in FPGA. (8)
15. (a) (i) Write the VHDL entity and behavioral description of a 4 to 1 MUX and 4 bit counter. (10)
(ii) Explain the different timing controls available in VHDL with suitable examples. (6)

Or

- (b) (i) Write a VHDL code for 1:8 demultiplexer. (10)
(ii) Write a test bench for a FSM used to detect the sequence 1101. (6)

