



LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

BQ24728
System Charge Power (+BATCHG)

G5934RZ1U
System Discharge Power
(+1.5V/+3V/+5V)
(+3VSUSV/+3VLAVCC/+1.1V)

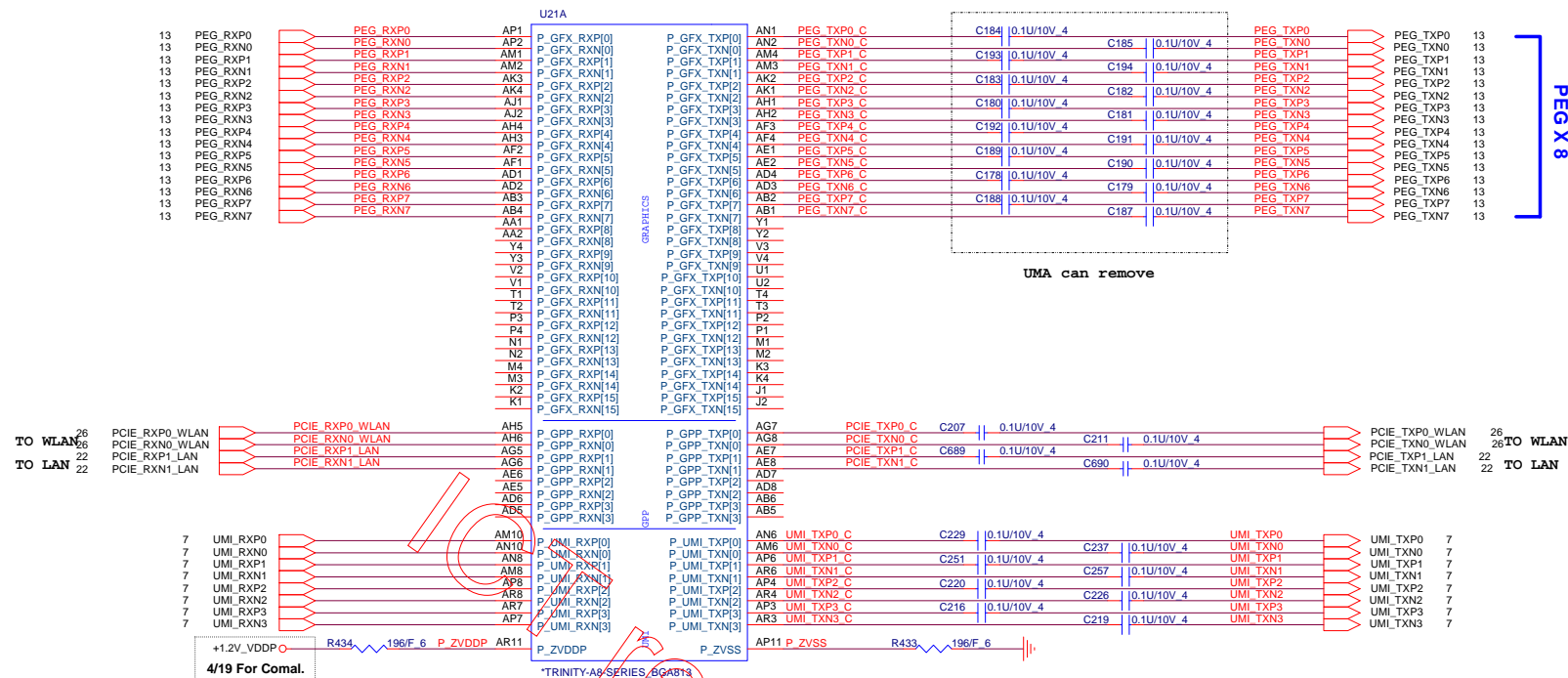
Ricktek RT8223PZ
System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

SL6277/RT8228AZ/AP3407A/ISL6208BCRZ
Processor Power (+VCC_CORE/
+1.2V/+2.5V/+VDDNB_CORE)

TPS51216RUKR
System Memory Power (+1.5VSUS/
+0.75V DDR_VTT)

AOZ1237QI-02
PCH Power (+1.1VS5)

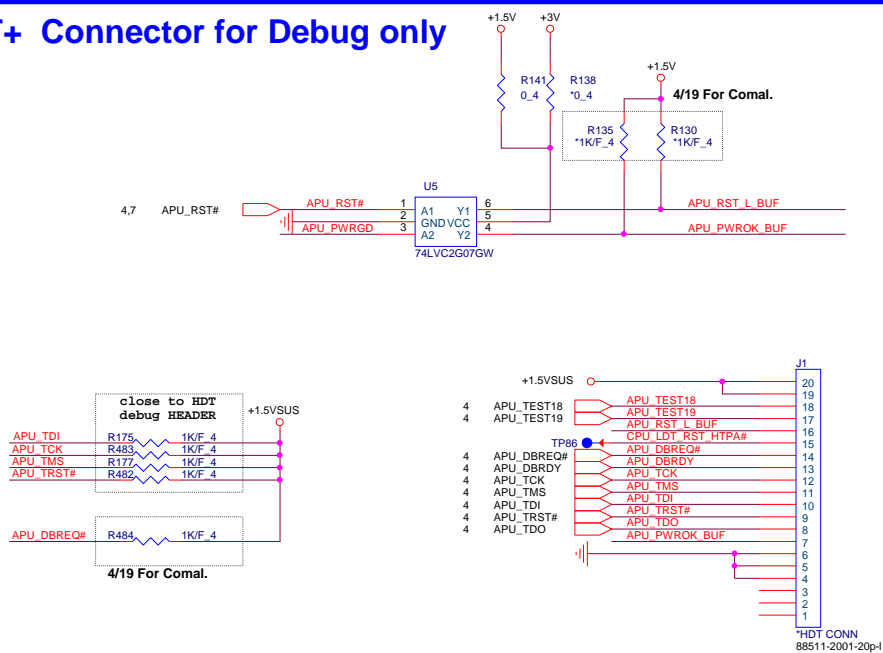
ADP3211A
DGPU Power (+VGA_CORE/+1.0V_VGA/+3V_VGA/
+1.5V_VGA/+1.8V_VGA/+VDDCI)



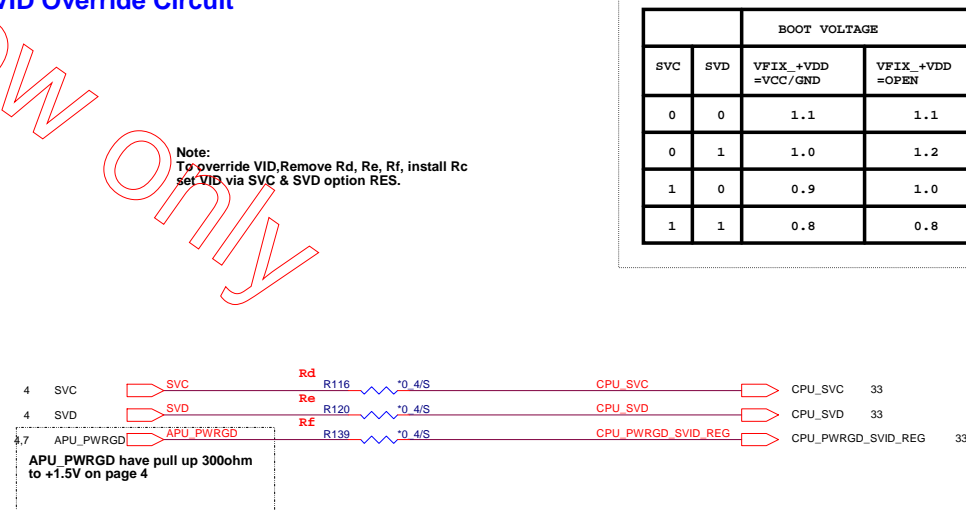
PEG X 8

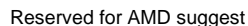
TO WLAN
TO LAN

HDT+ Connector for Debug only

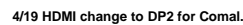


VID Override Circuit





Display port power 1.5V min 1.2v max : 1.65v

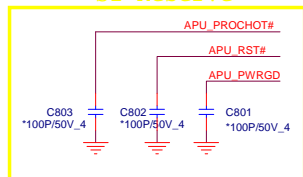


DP2 output to HDMI connector

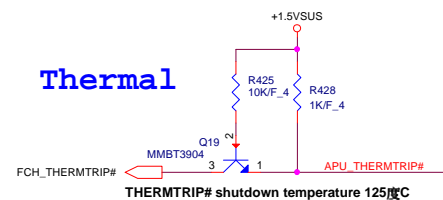
note -HDMI P&N can not swap

Note: CLK_APU_HCLKP/N is 100MHZ SSC

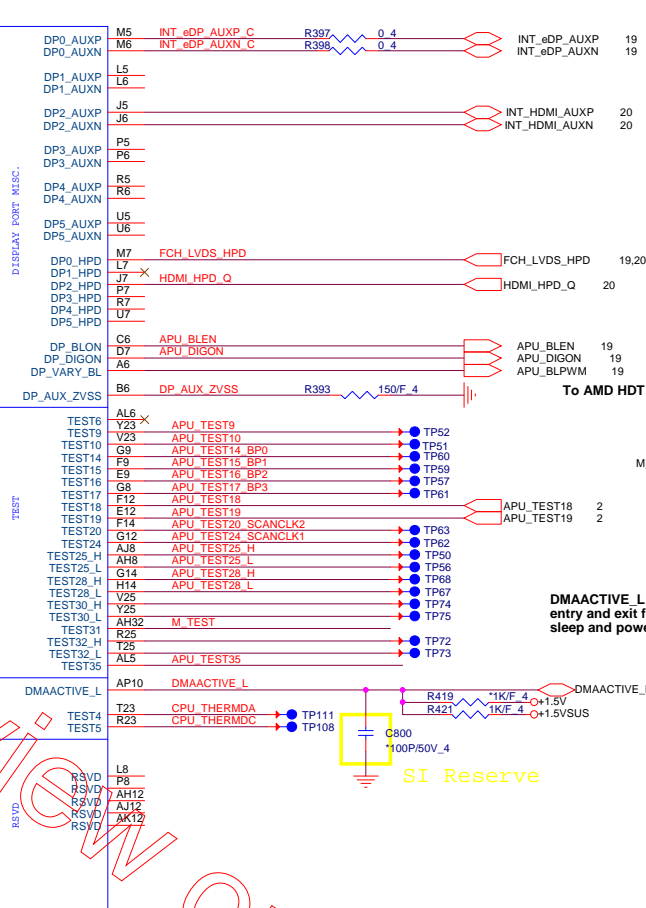
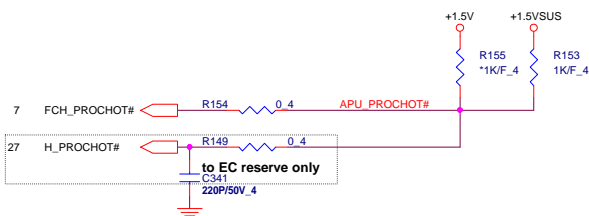
Note: CLK_DP_NSSCP/N is 100MHZ non-S



Thermal

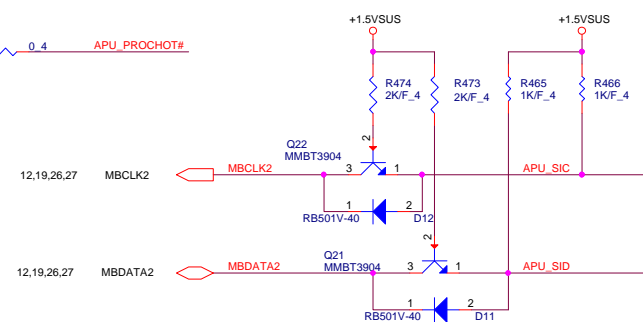


**4/19 For Comal,
close to APU.**



To AMD HDT

DMAACTIVE_L controls entry and exit from the sleep and power states

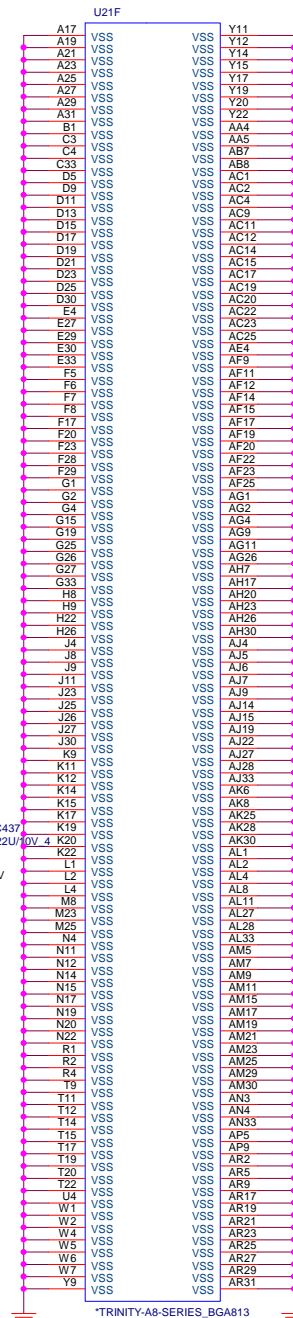
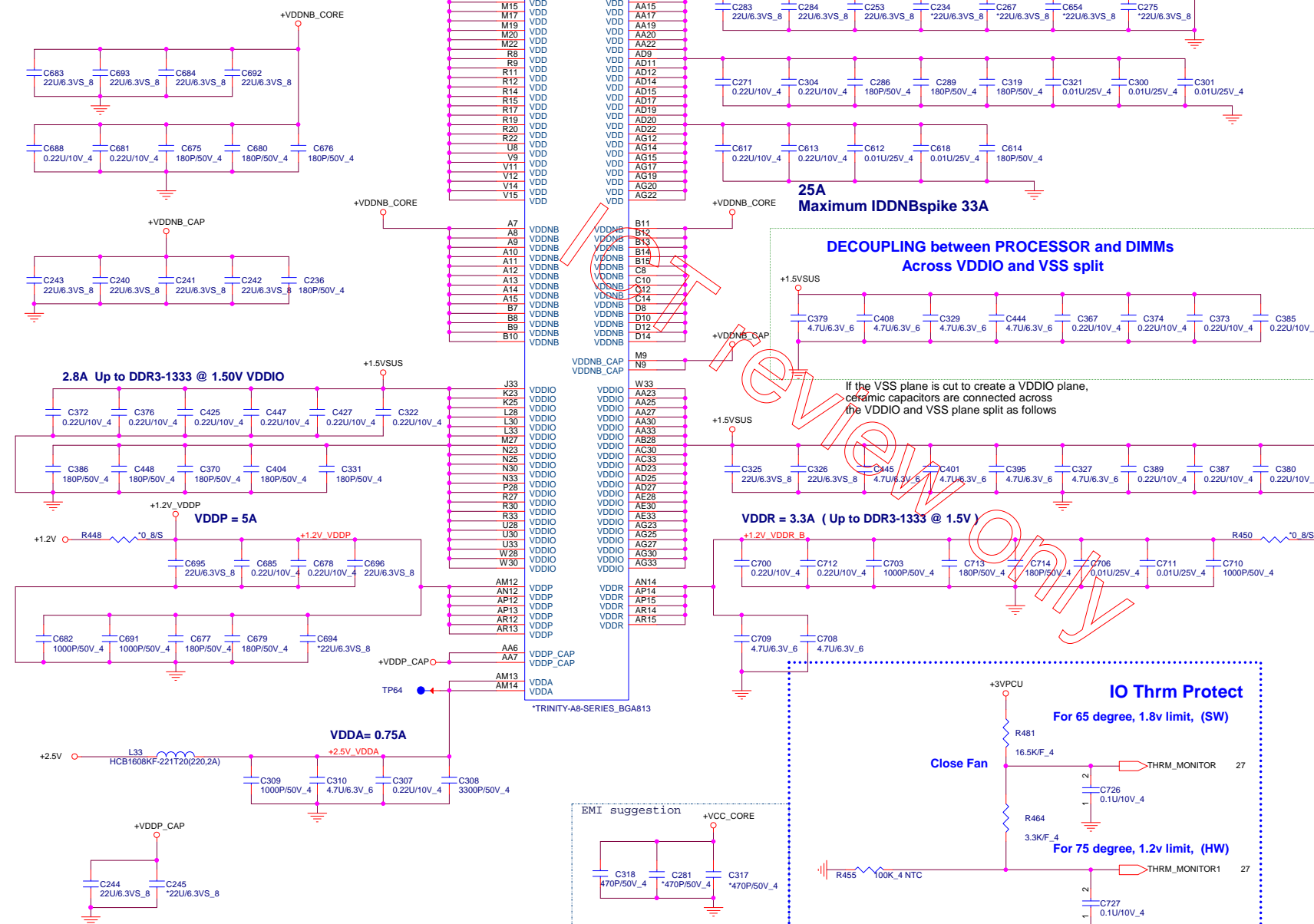


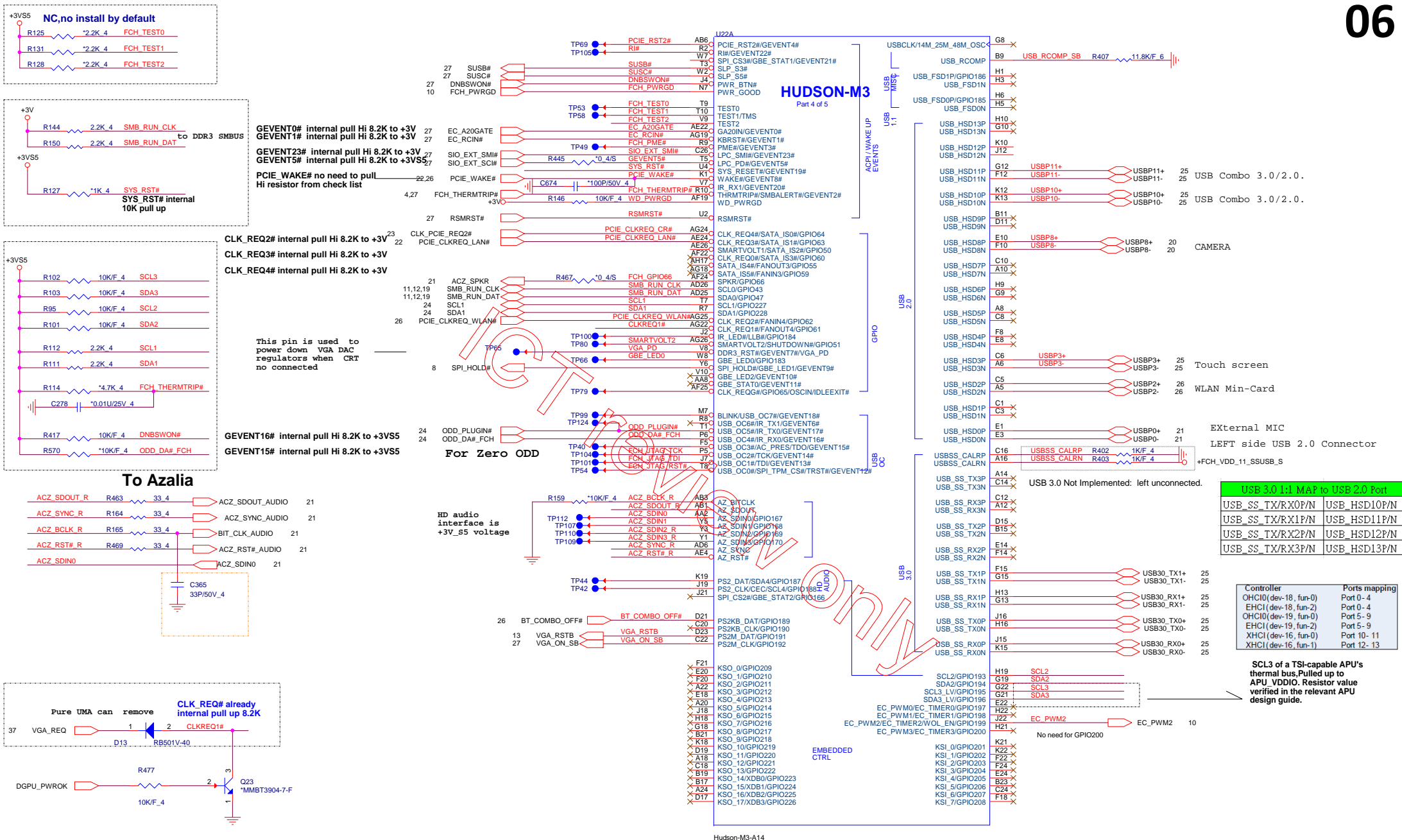
PROJECT : U92
Quanta Computer Inc.

Size	Document Number Llano Display/Misc	Rev 1A
Date:	Wednesday, March 27, 2013	Sheet 4 of 37

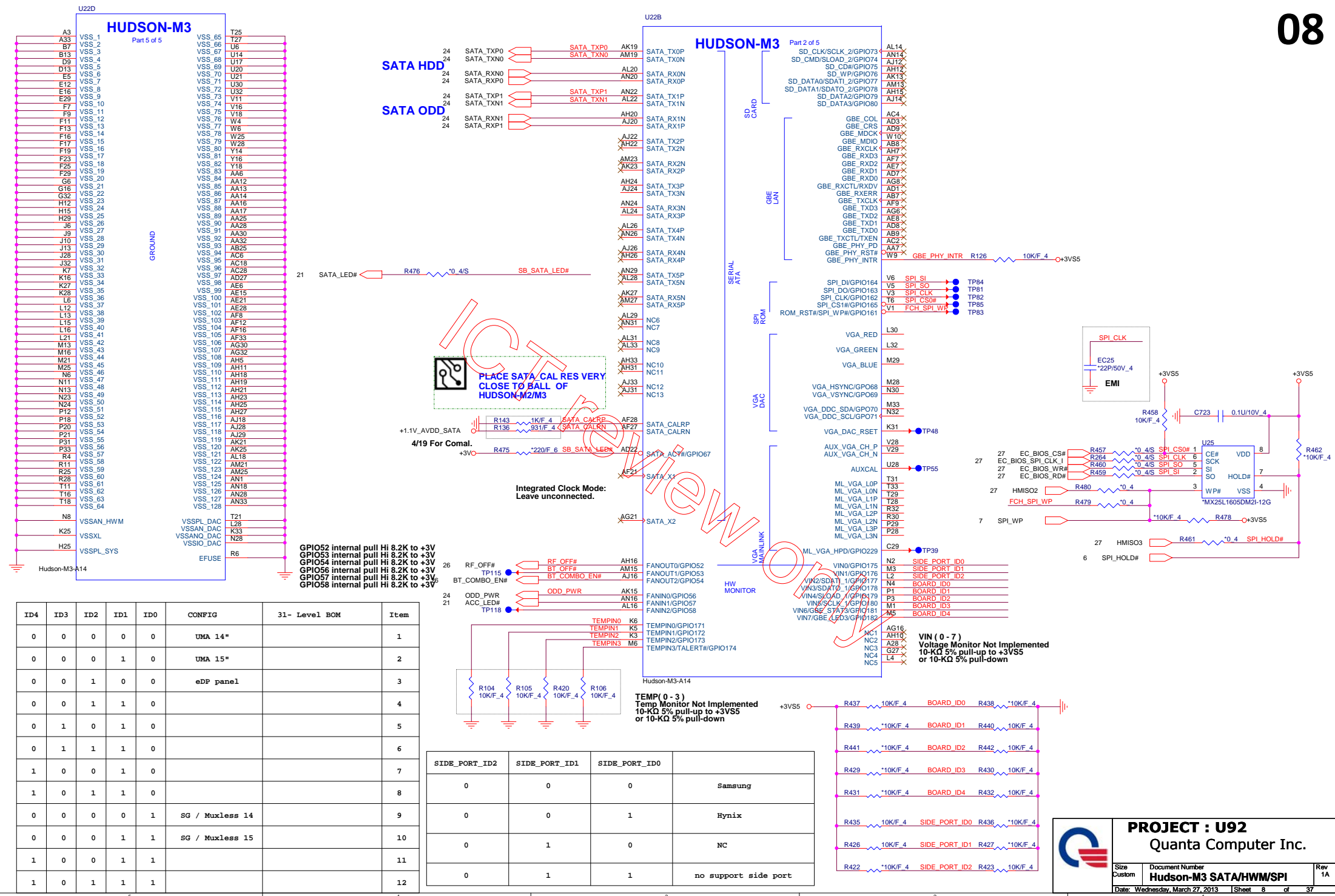
APU POWER TABLE

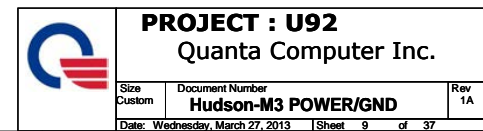
PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V





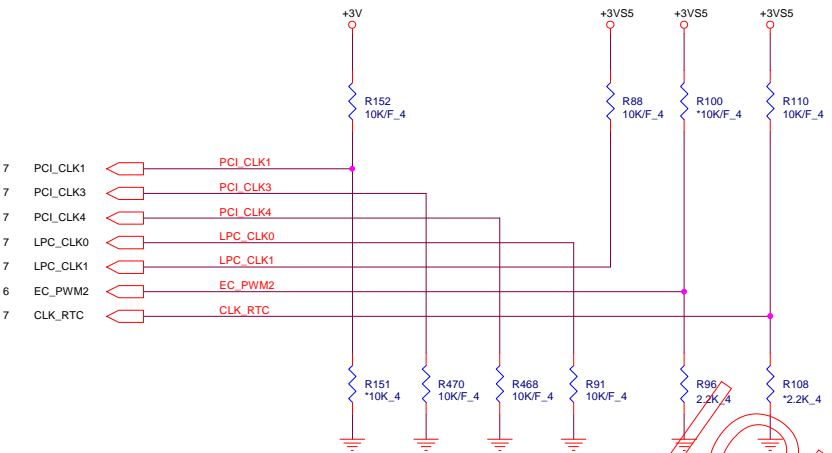






STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE ENABLED DEFAULT
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE DISABLED

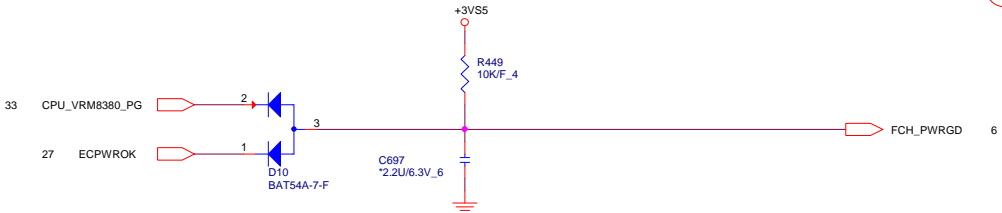
DEBUG STRAPS

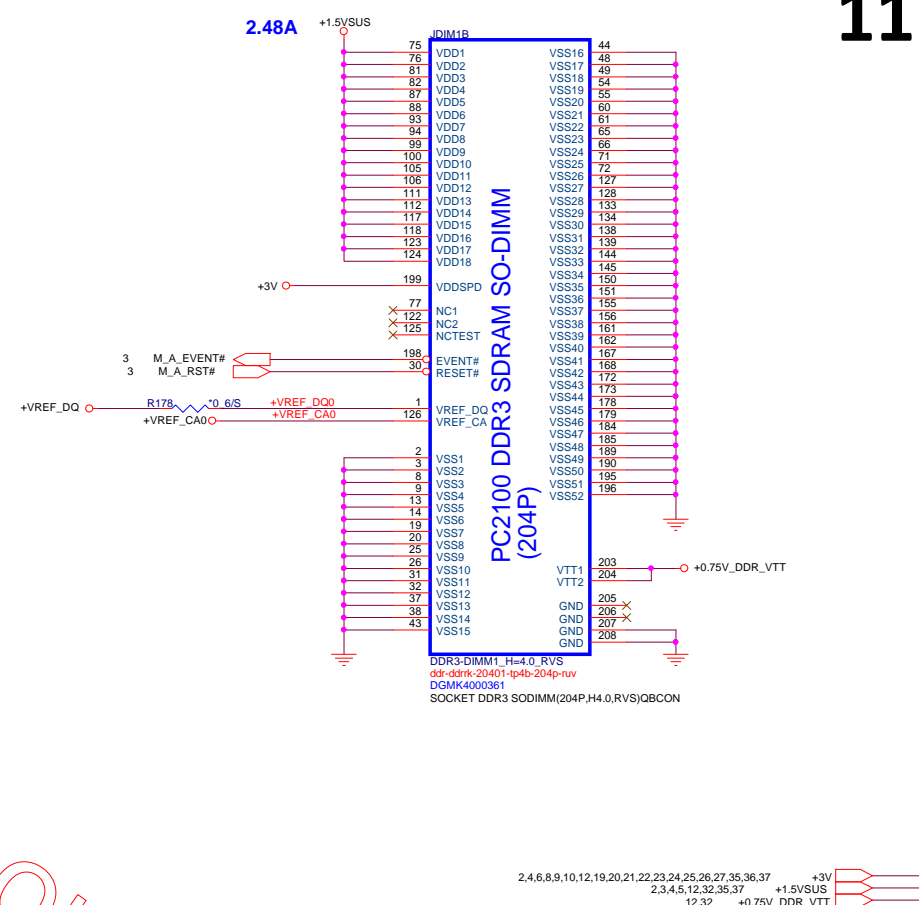
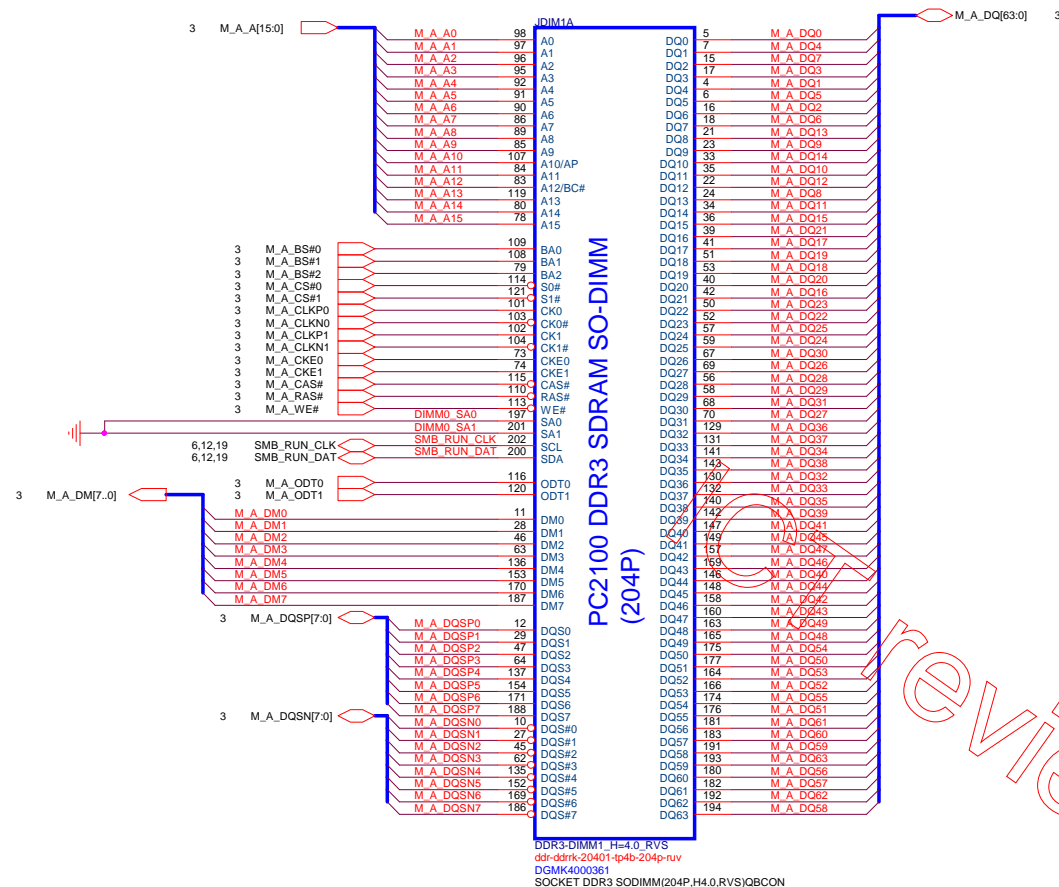
FCH has 15K Internal Pull Up for PCI_AD[27:23]



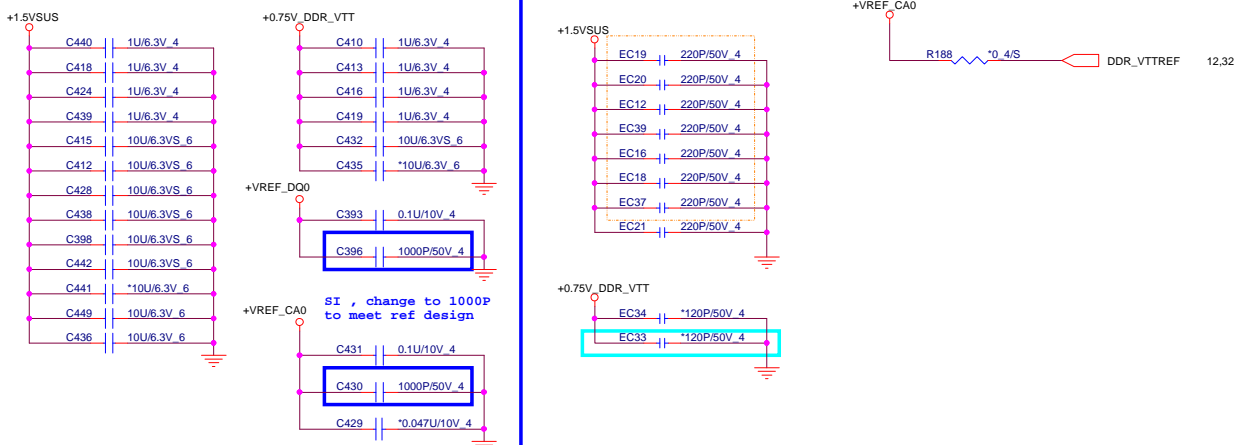
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH_PWRGD

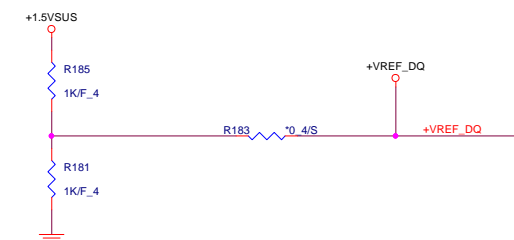





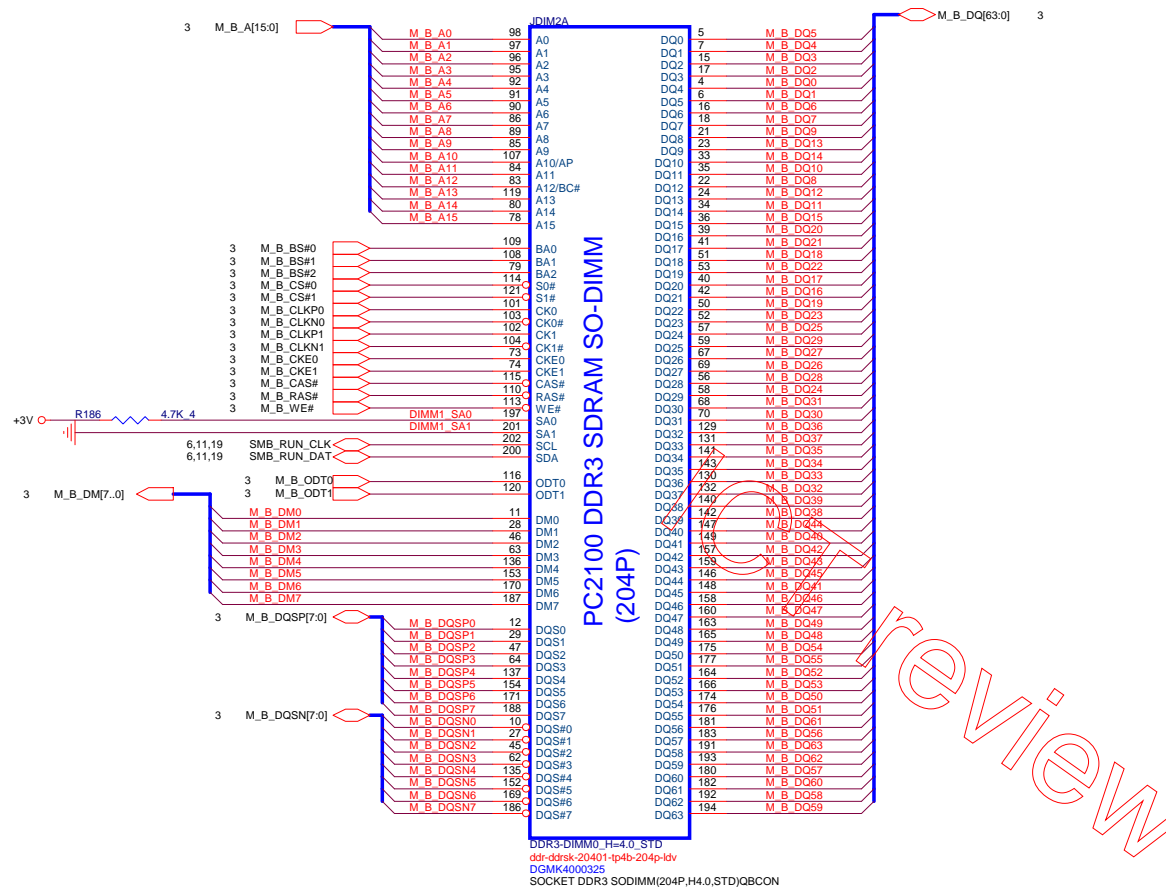
Place these Caps near So-Dimm0.



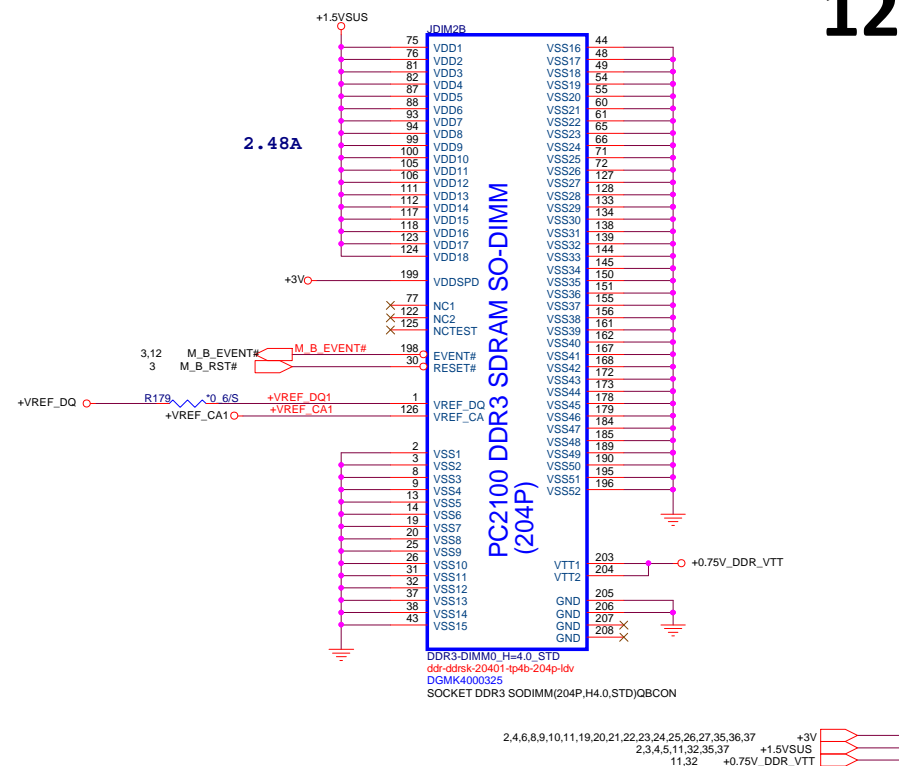
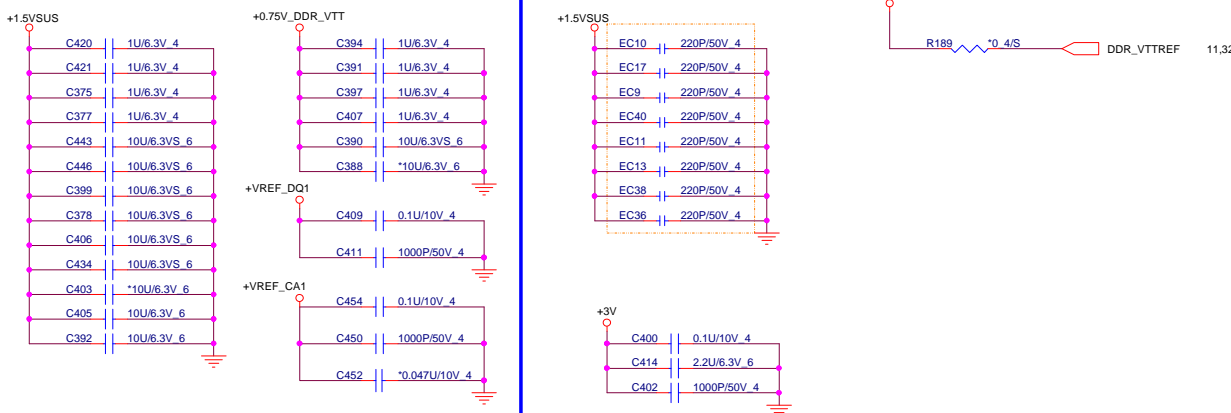
Reserved for AMD suggest



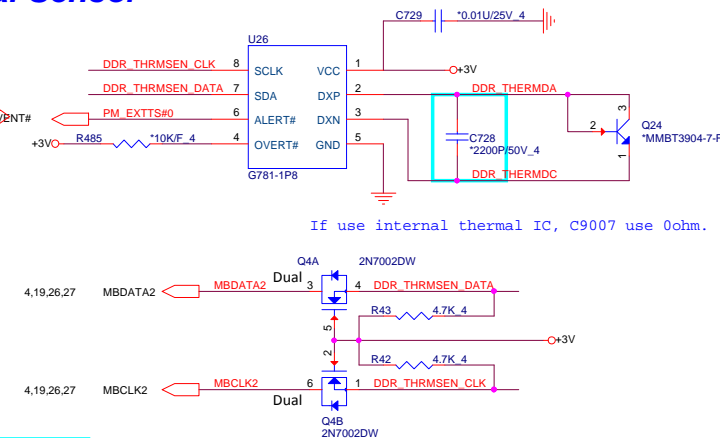
 PROJECT : U92 Quanta Computer Inc.		
Size Custom	Document Number System Memory 1/2 (5.2H)	Rev 1A
Date: Wednesday, March 27, 2013	Sheet 11 of 37	



Place these Caps near So-Dimm1.

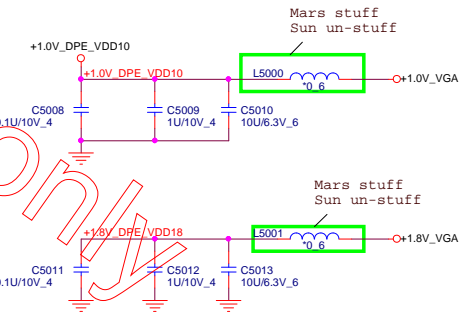
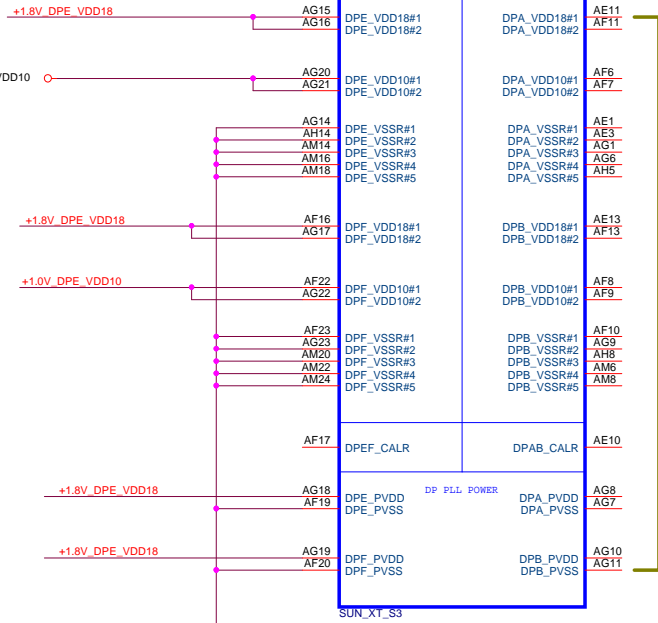
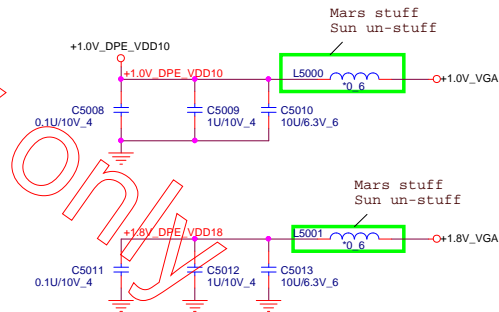


Local Thermal Sensor

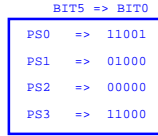
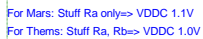


Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

PROJECT : U92		
Quanta Computer Inc.		
Size	Document Number	Rev
Custom	System Memory 2/2 (9.2H)	1A
Date:	Wednesday, March 27, 2013	Sheet 12 of 37



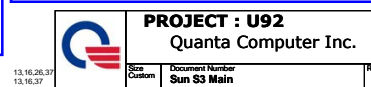
Default

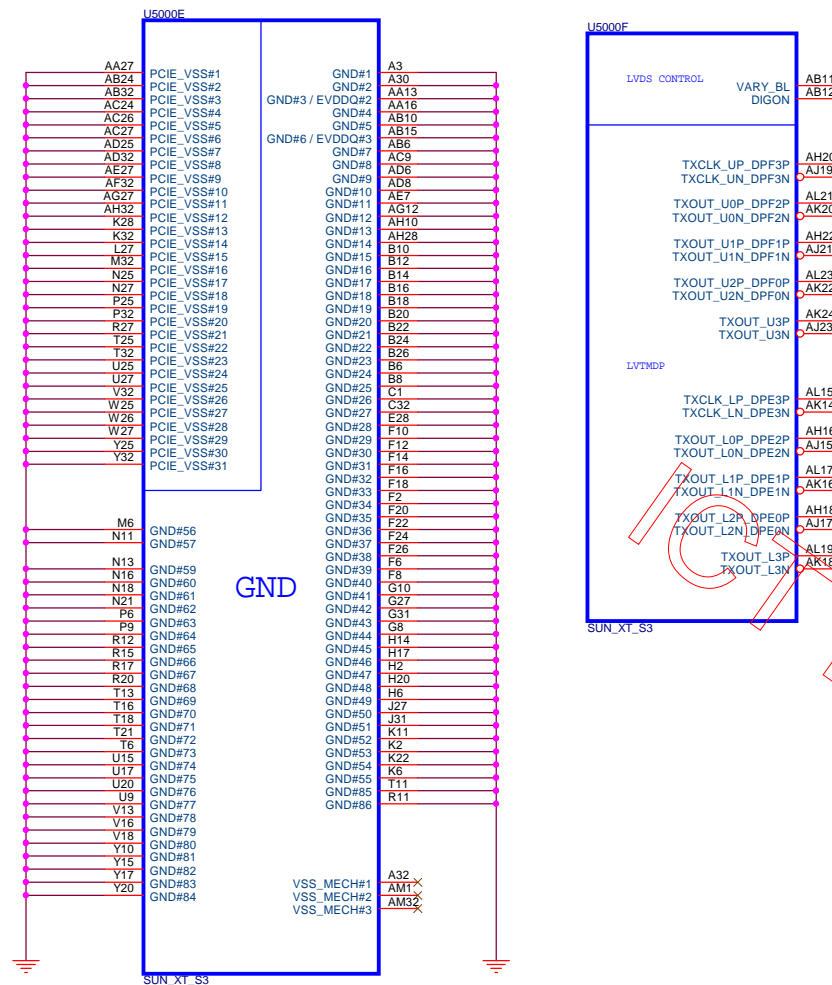


- Connect GPIO_28 to 10K pulldown to enable MFS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_{pu}, R_{pd} and C must be properly populated per tables below
- Place MFS circuit components as close to the ASIC as possible
- Total DC resistance of trace between Ps pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table		Resistor Divider Lookup Table		
C (nF)	Bits[5:4]	R _{DN} (Ohm)	R _{UP} (Ohm)	Bits[3:2,1]
680	00	NC	4750	000
82	01	8450	2000	001
10	10	4530	2000	010
NC	11	6980	4990	011
		4530	4990	100
		3240	5620	101
		3400	10000	110
		4750	NC	111

PS_3[5]	aud_port_cp[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[4]	aud_port_cp[1]			
PS_3[3]	aud_port_cp[0]			





CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1 = INSTALL 3K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

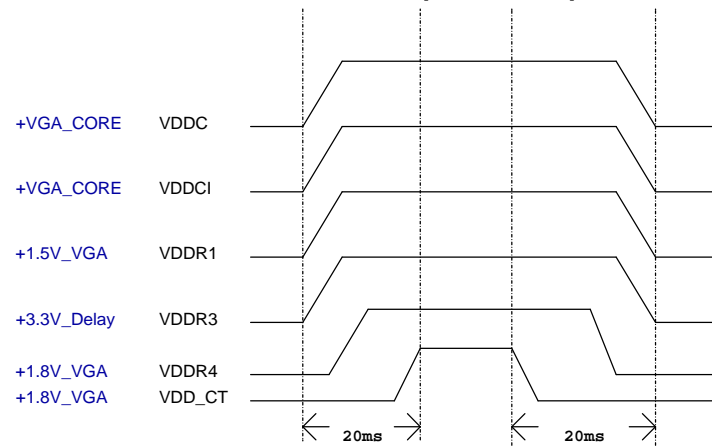
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUDI[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUDI[0]	VSYS	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

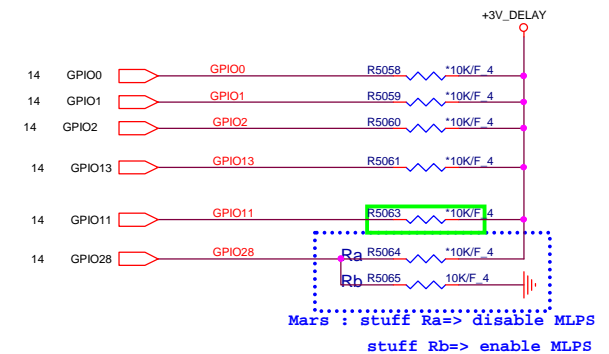
Power Up/Down Sequence



Memory Aperture size(Seymour)

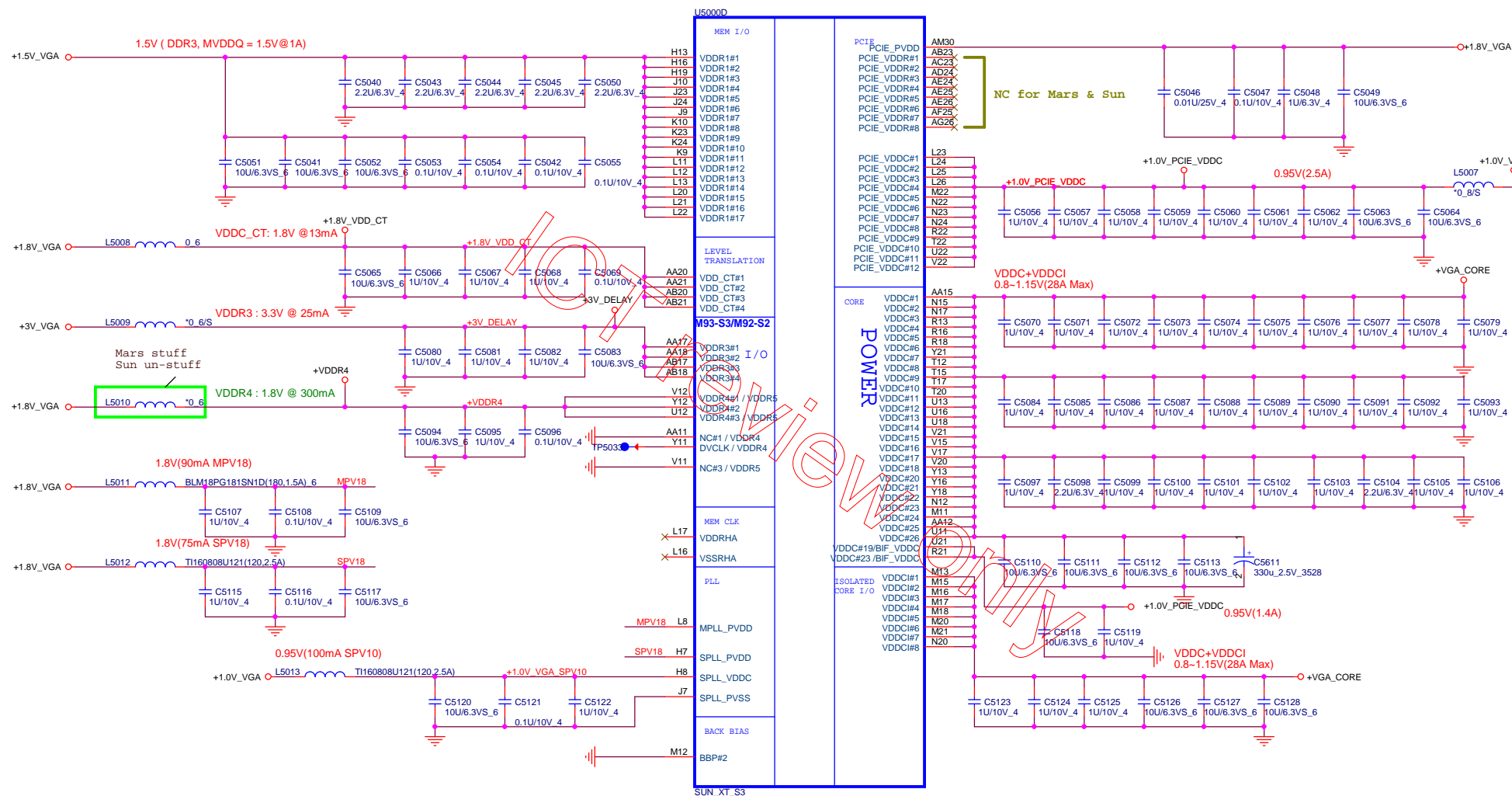
GPIO9		GPIO13	GPIO12	GPIO11
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

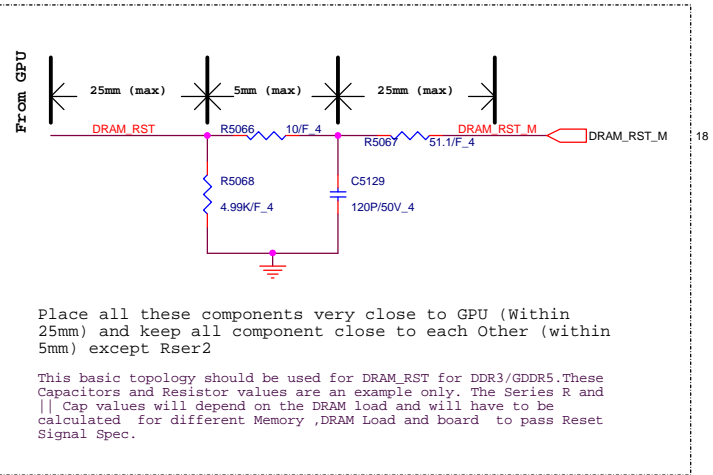


PROJECT : U92
Quanta Computer Inc.

Size Custom Document Number Sun S3 GND / LVDS/ Straps Rev 1A
 Date: Wednesday, March 27, 2013 Sheet 15 of 37

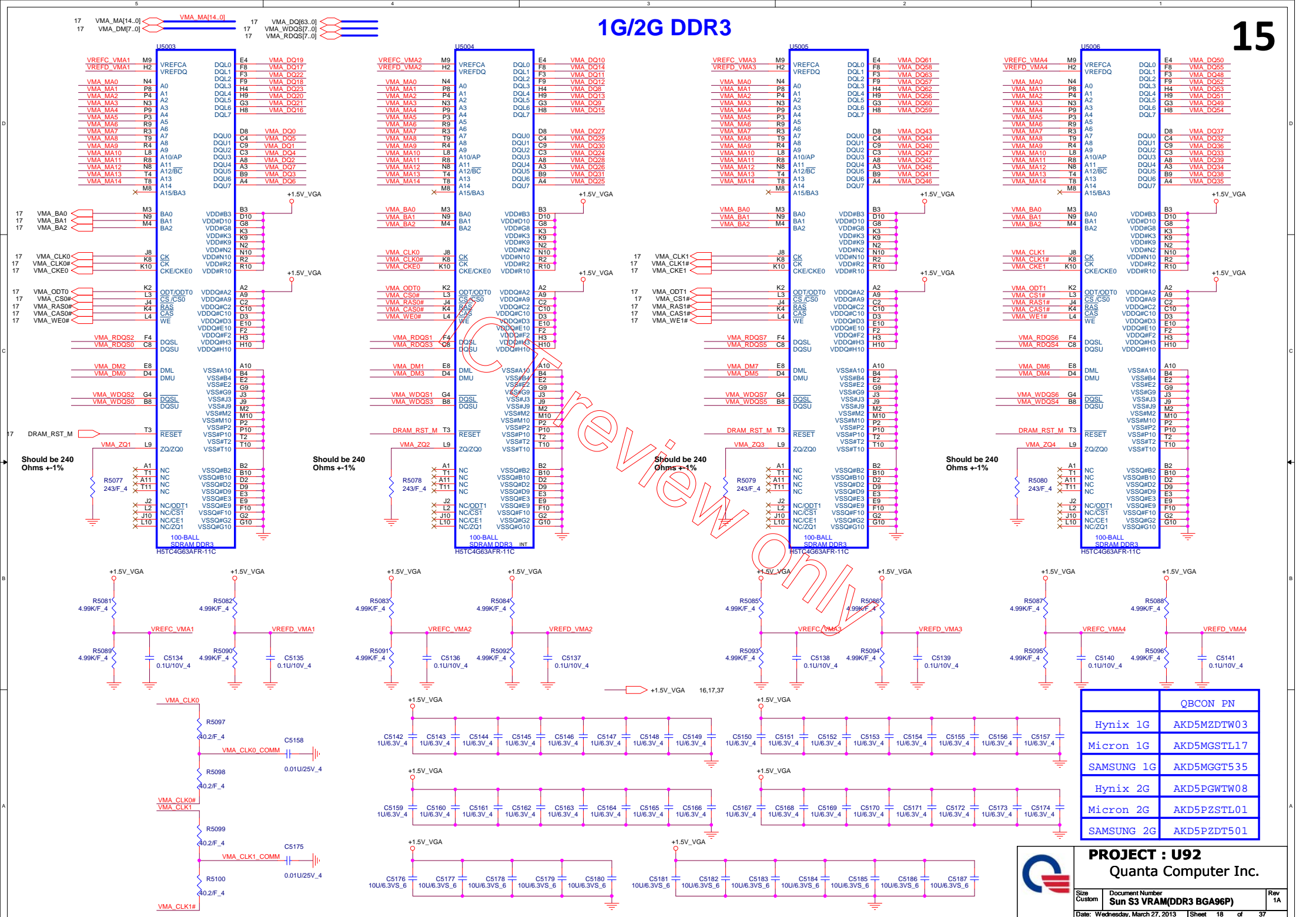


+1.5V_VGA	17,18,37
+1.8V_VGA	13,14,26,37
+1.0V_VGA	13,14,37
+VGA_CORE	36,37
+3V	2,4,6,8,9,10,11,12,19,20,21,22,23,24,25,26,27,35,36,37
+5V	20,21,24,25,35



1G/2G DDR3

15



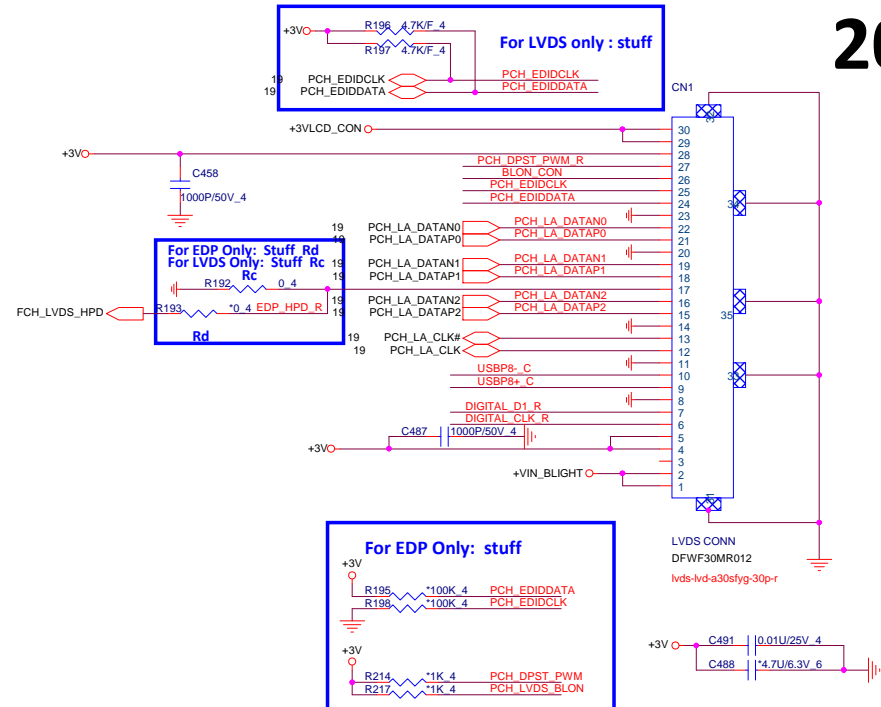
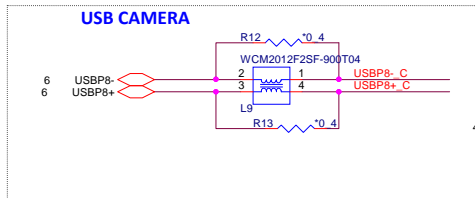
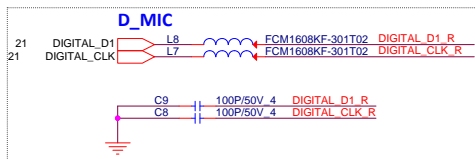
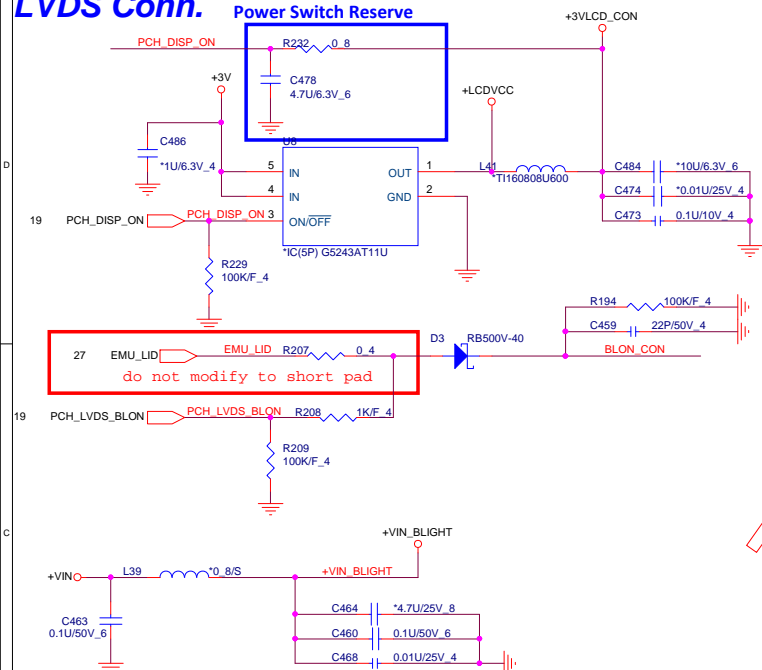
	QBCON PN
Hynix 1G	AKD5MZDTW03
Micron 1G	AKD5MGSTL17
SAMSUNG 1G	AKD5MGGT535
Hynix 2G	AKD5PGWTW08
Micron 2G	AKD5PZSTL01
SAMSUNG 2G	AKD5PZDT501

PROJECT : U92
Quanta Computer Inc.

Size Custom	Document Number Sun S3 VRAM(DDR3 BGA96P)	Rev 1A
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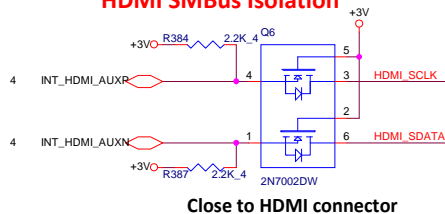
LVDS Conn.

Power Switch Reserve



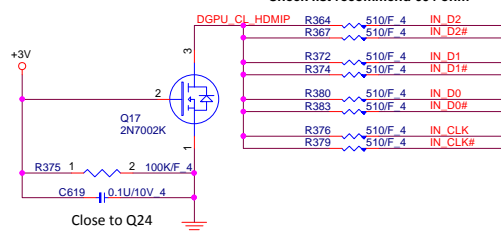
HDMI Conn.

HDMI SMBus Isolation

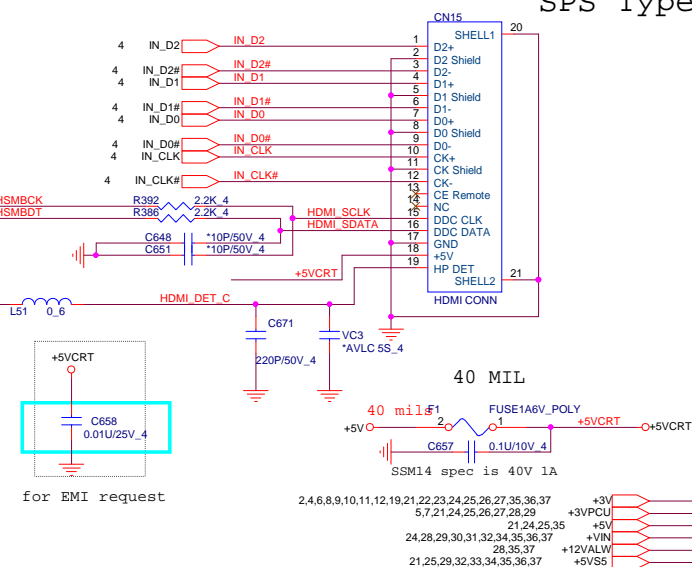
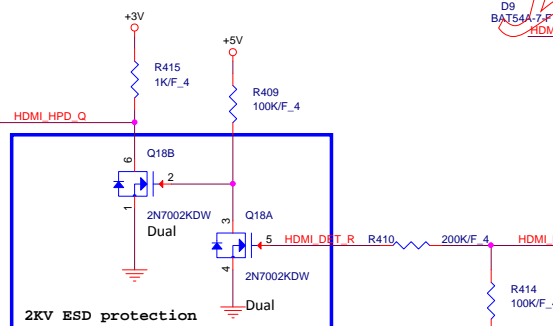
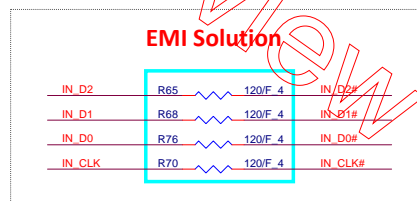


Close to HDMI connector

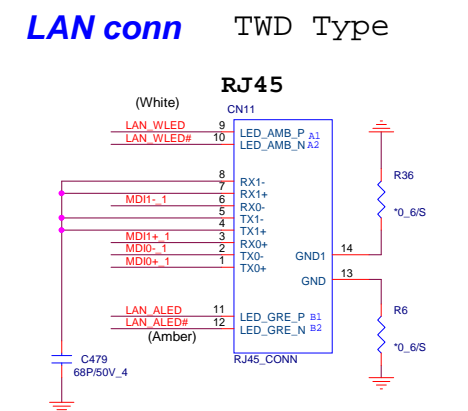
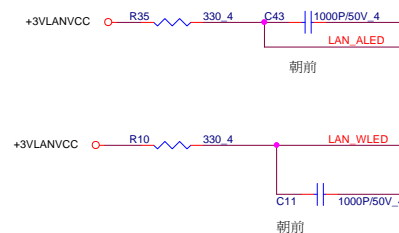
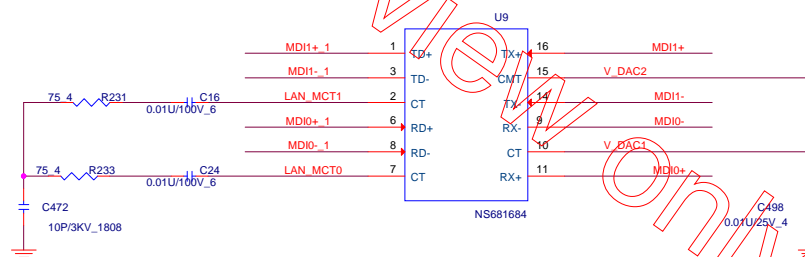
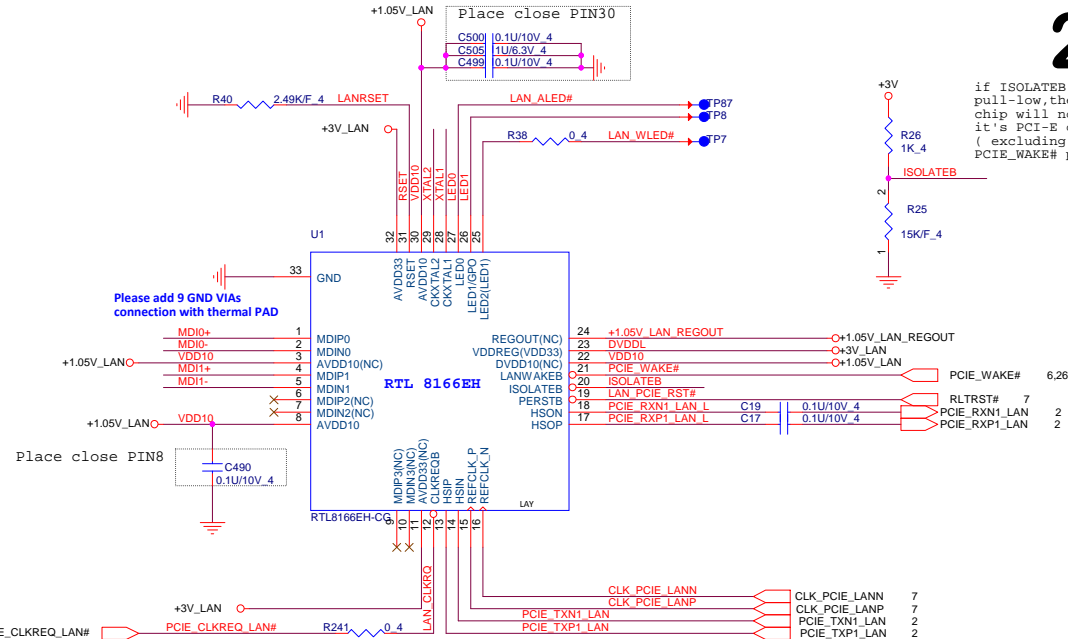
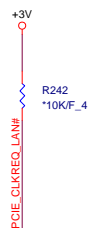
Check list recommend 604 ohm



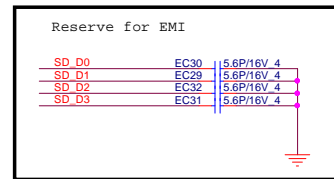

HDMI HPD SENSE




SPS Type



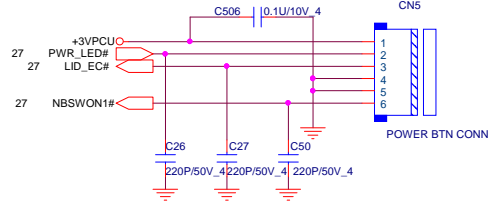
6V 4
6V 4
6V 4
6V 4



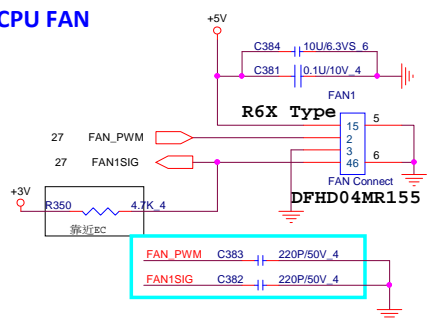
	PROJECT : U92 Quanta Computer Inc.		
	Size Custom	Document Number RTS5239 & CR SOCKET	Rev 1A
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Power Button Connector

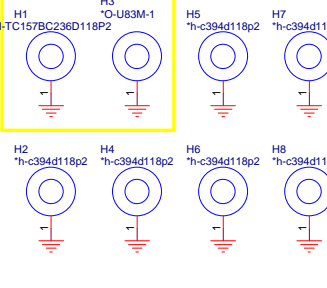
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



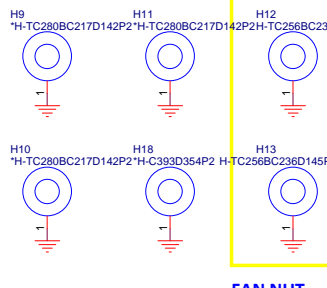
CPU FAN



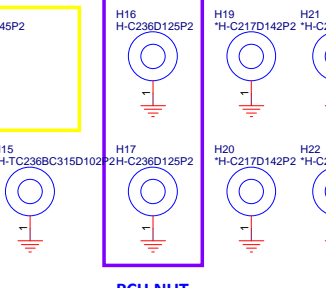
HoleSI change footprint



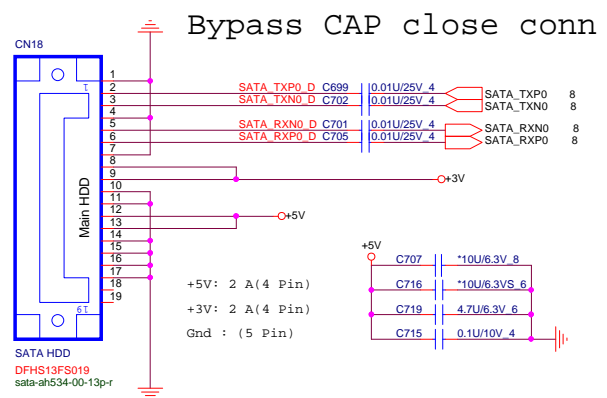
SI change FAN NUT P/N



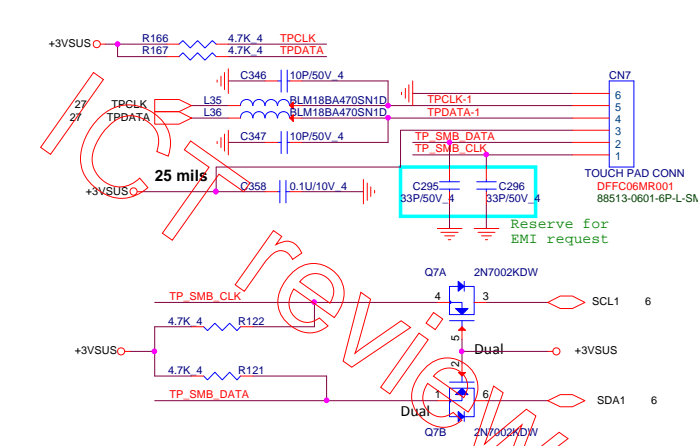
SI Del WLAN NUT



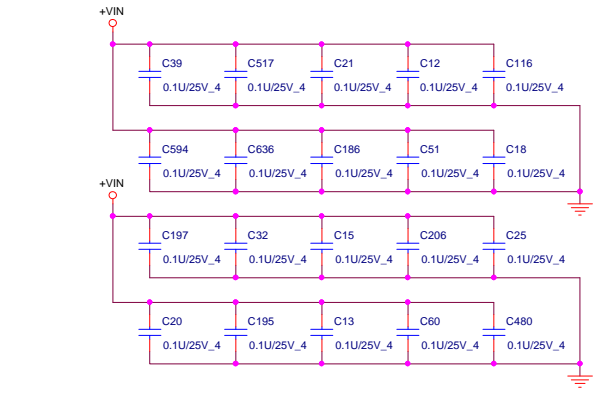
SATA HDD Connector(Cable type)



Touch Pad

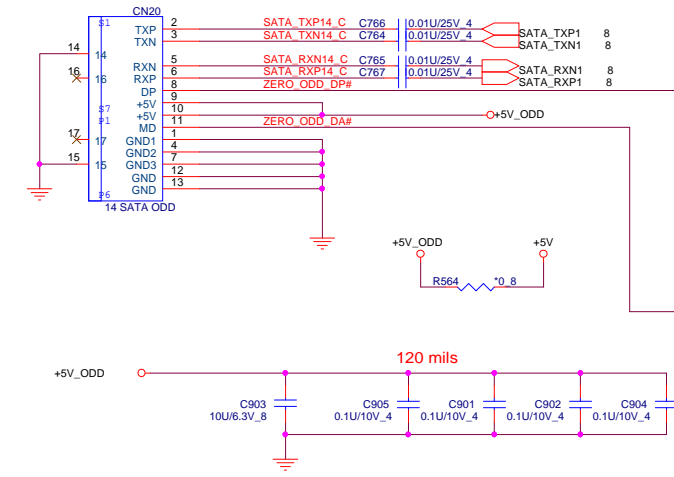


+VIN Cap

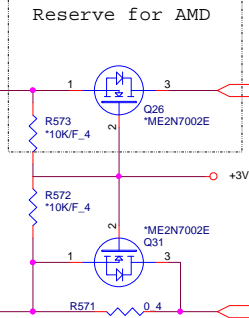


SATA ODD CONNECTOR

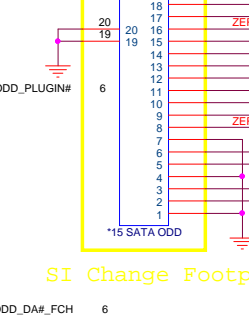
NEW Type Bypass CAP close conn



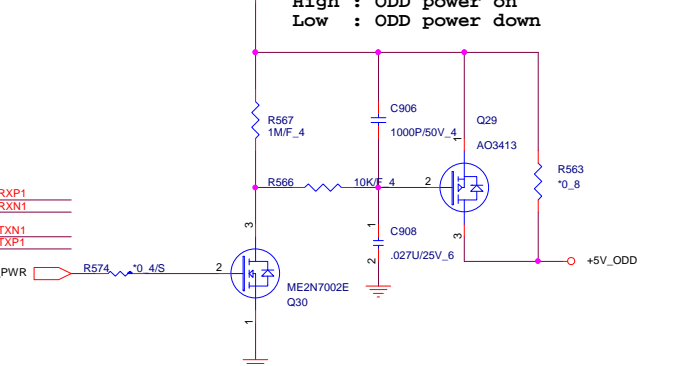
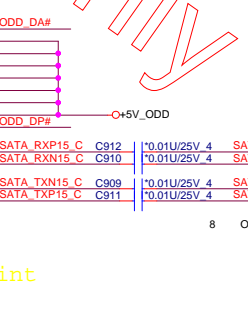
Reserve for AMD



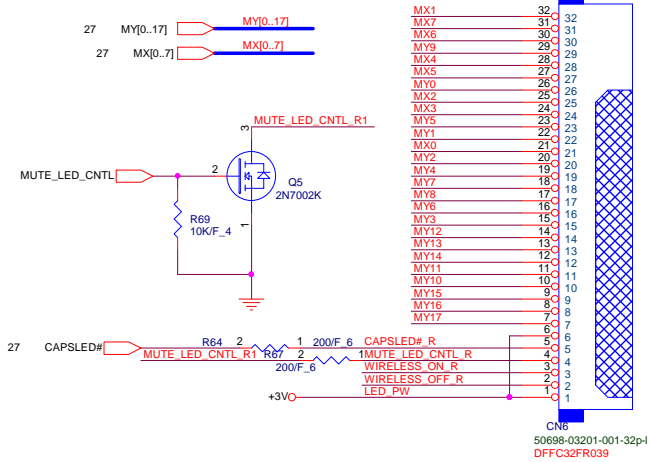
New Type



SI Change Footprint

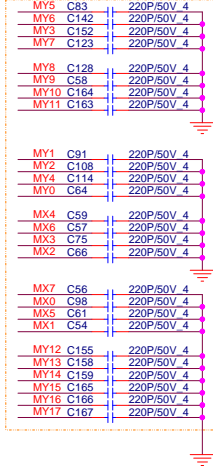
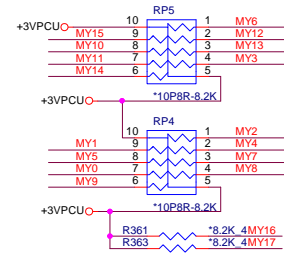


KEYBOARD Con.

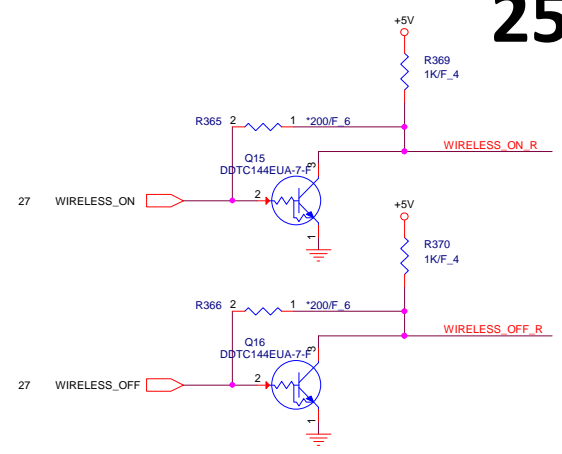


R6X Type

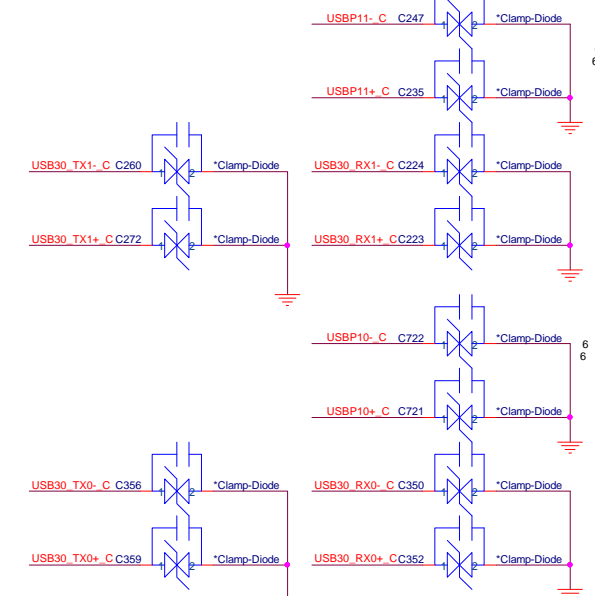
KEYBOARD PULL-UP



25

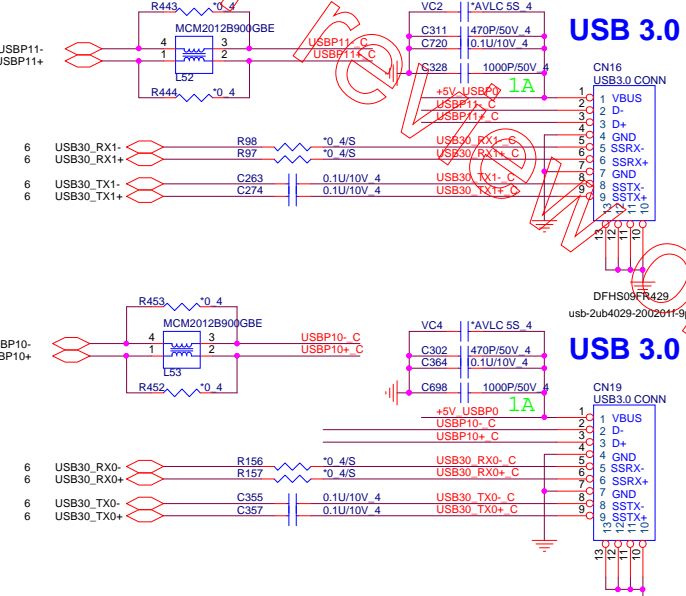


USB 2.0/3.0 Combo

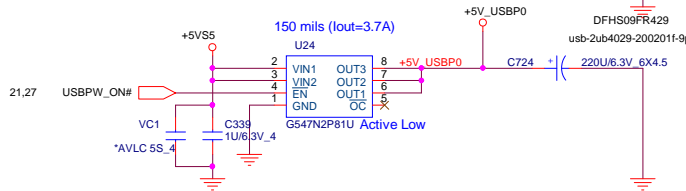


SPS Type

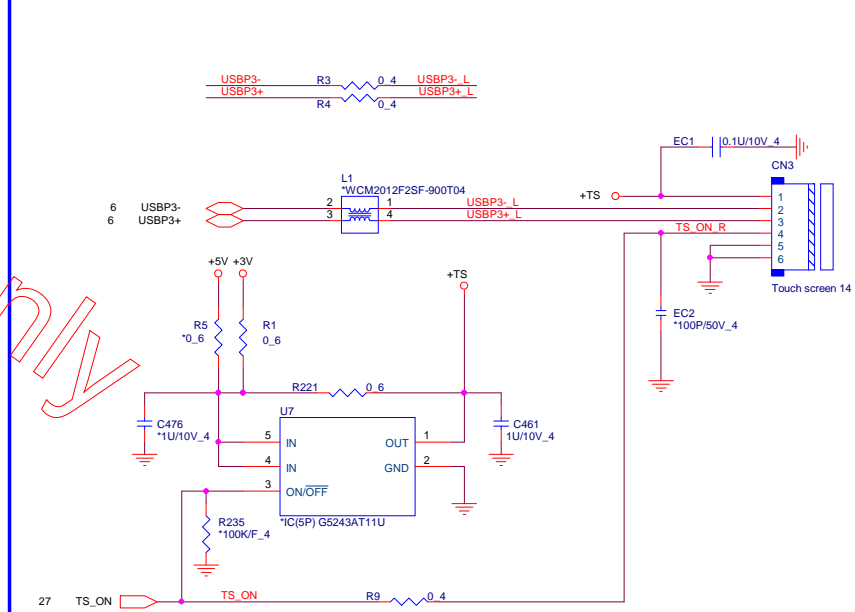
USB 3.0



USB 3.0



Touch screen



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USB 3.0/KB/Green CLK		
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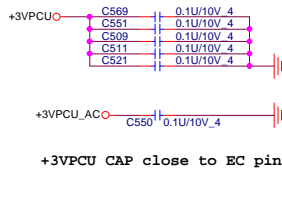
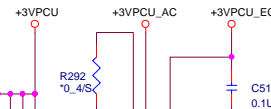
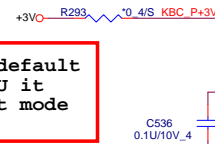
21,29,32,33,34,35,36,37
5,7,21,24,26,27,28,29

+5VS5
+3VPCU

2,4,6,8,9,10,11,12,19,20,21,22,23,24,25,26,35,36,37
5,7,21,24,25,26,28,29

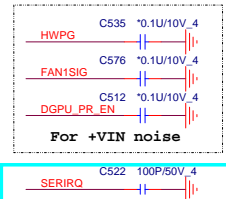
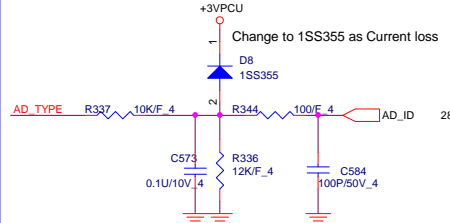
+3V
+3VPCU

ITE pin 100 , 104 , 106 default
can not pull up to +3VPCU it
will cause chip into test mode



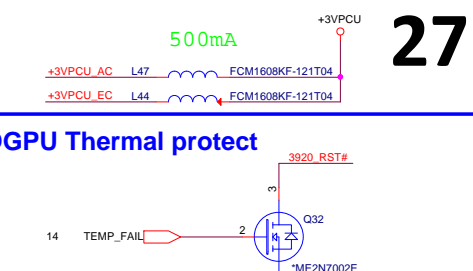
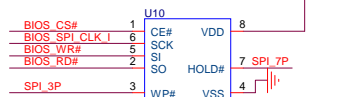
+3VPCU CAP close to EC pin

Smart adapter Type check

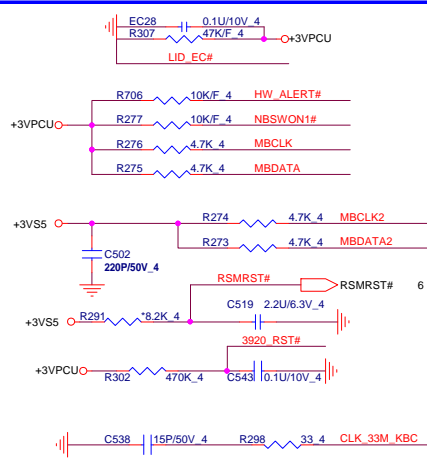


Vender	Size	P/N
AMIC	4M	AKE39F-0800
EON	4M	AKE392N0Q02
Socket		DFHS08FS023

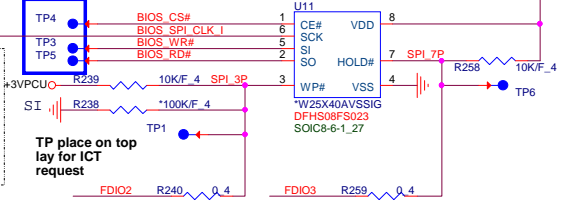
4M SPI EC ROM



DGPU Thermal protect



128K byte SPI EC ROM



Adapter select

+3VPCU - R321 - 10K/F_4 - GPIO42 - R320 - 10K/F_4	
Hi ==> DIS/SG Low ==> UMA	
Platform model	GPIO42
N/A	High
DIS/SG/UMA	Low
	65W

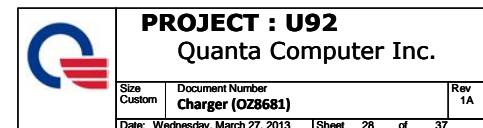
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Custom	EC (IT8528E)/ROM	1A

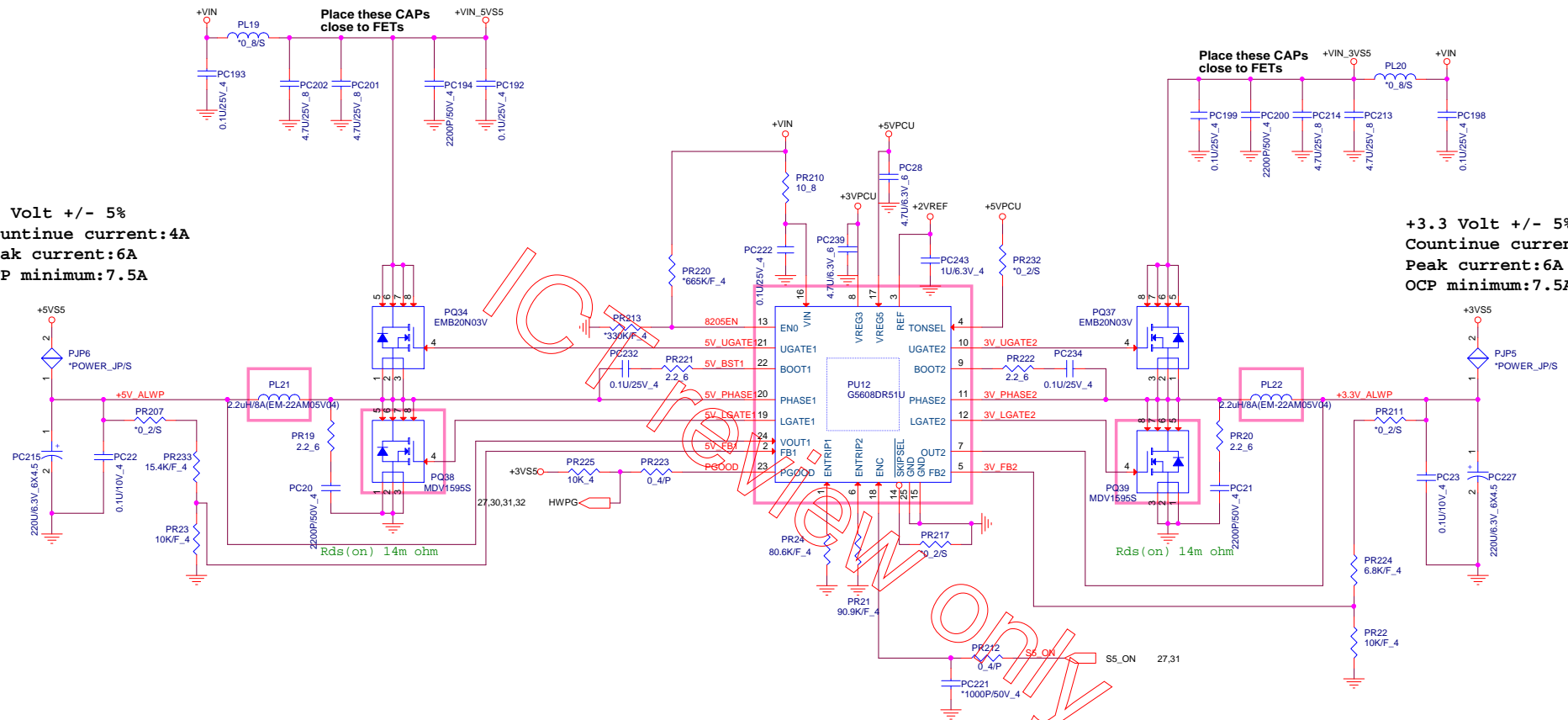
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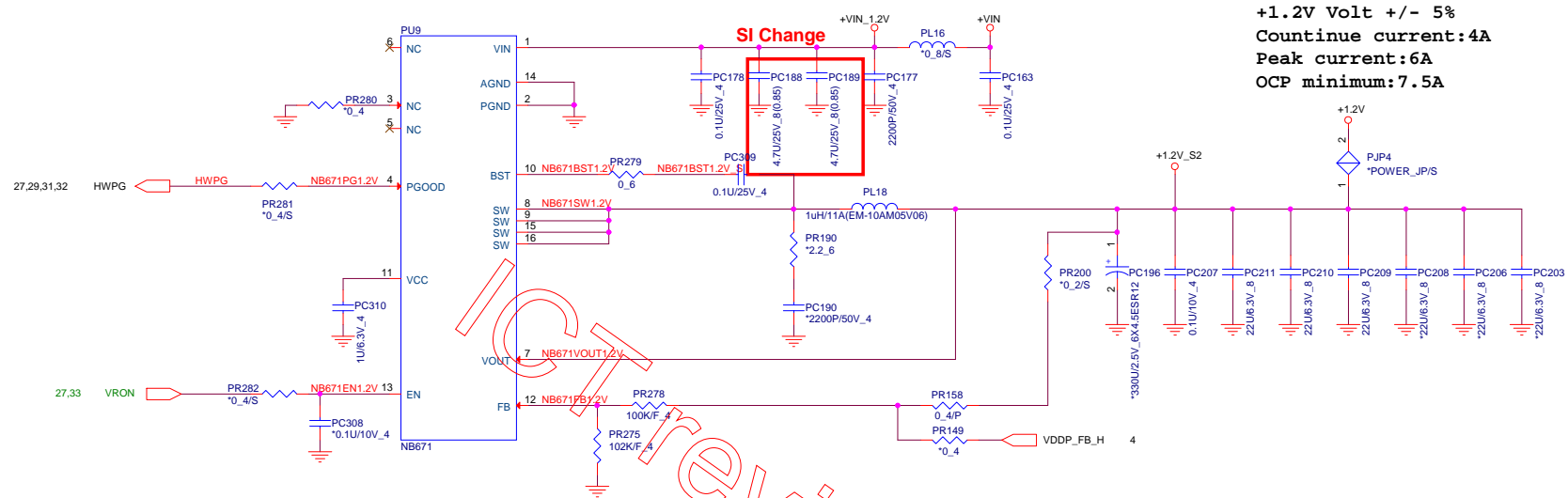
ADD VGA TEMP_FAIL function is active Hi

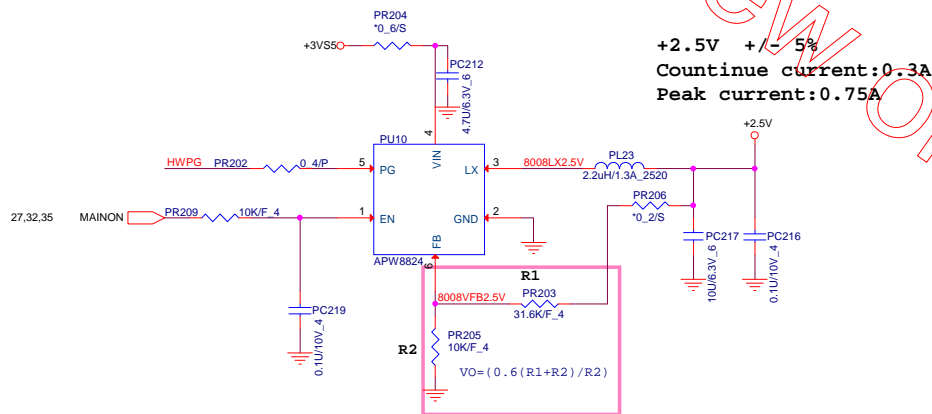
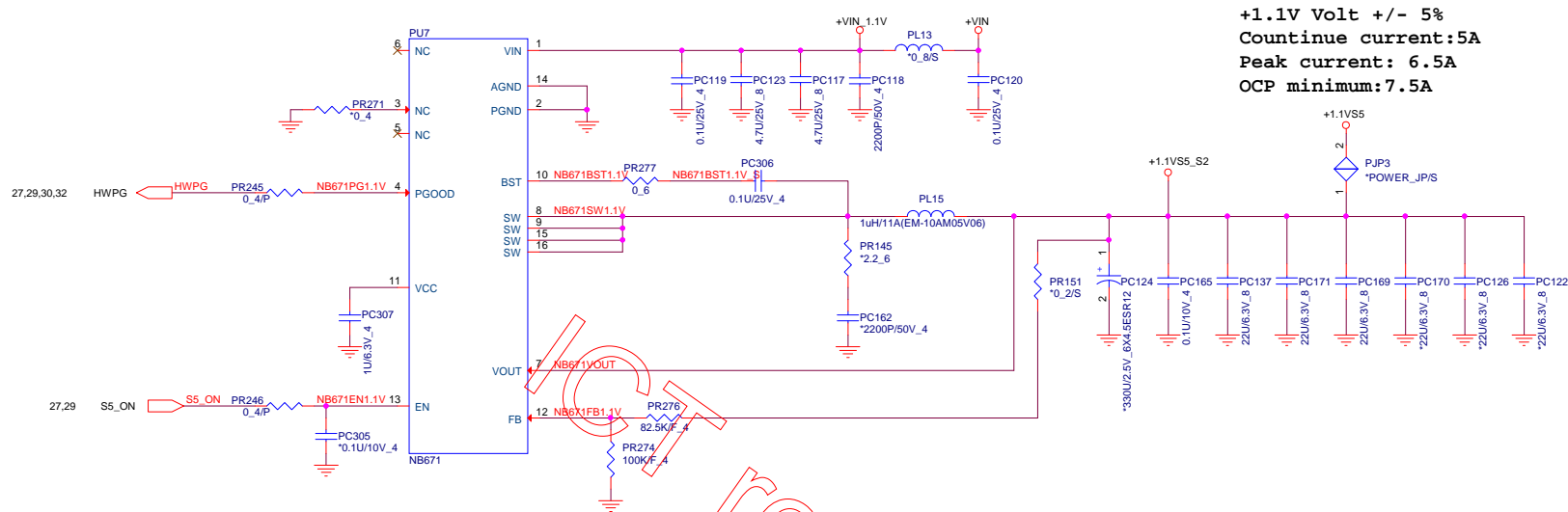


+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

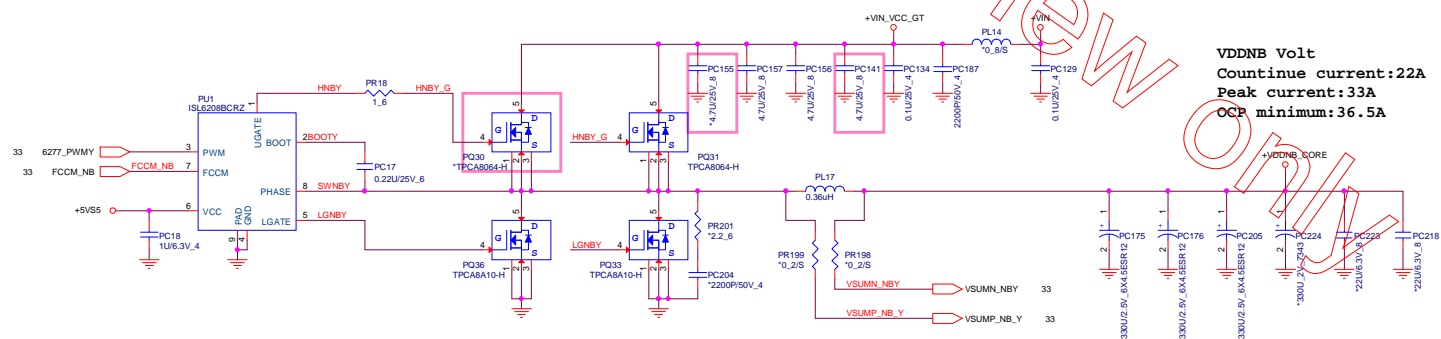
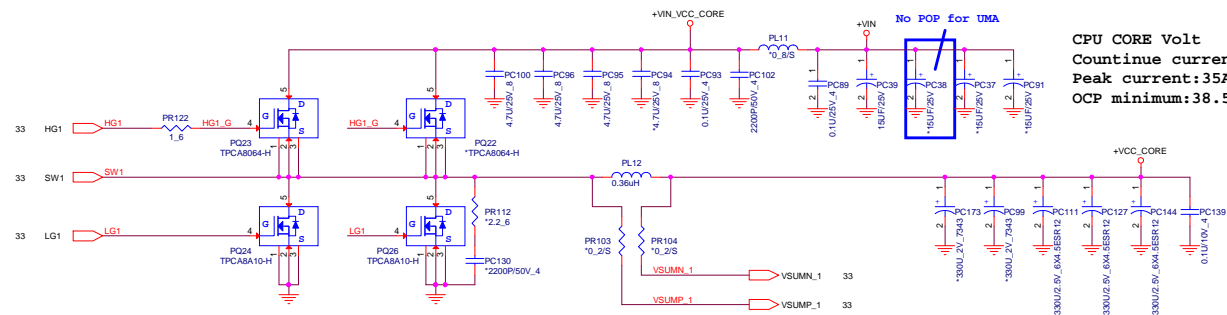
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A





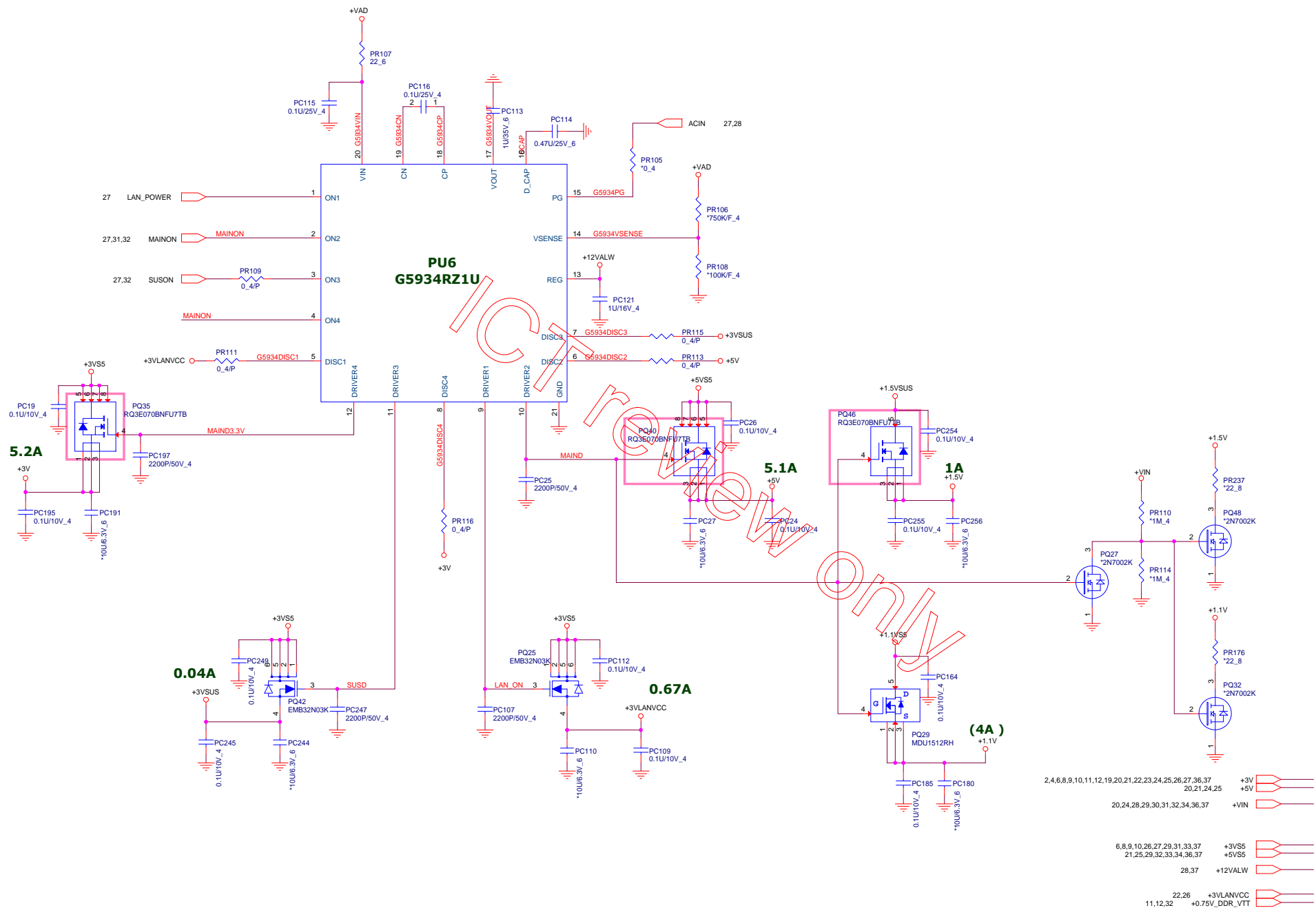


+VIN	20,24,28,29,30,32,34,35,36,37
+2.5V	5
+3VSS	6,8,9,10,26,27,29,33,35,37
+5VSS	21,25,29,32,33,34,35,36,37
+1.1VS5	9,35
+5VPCU	28,29

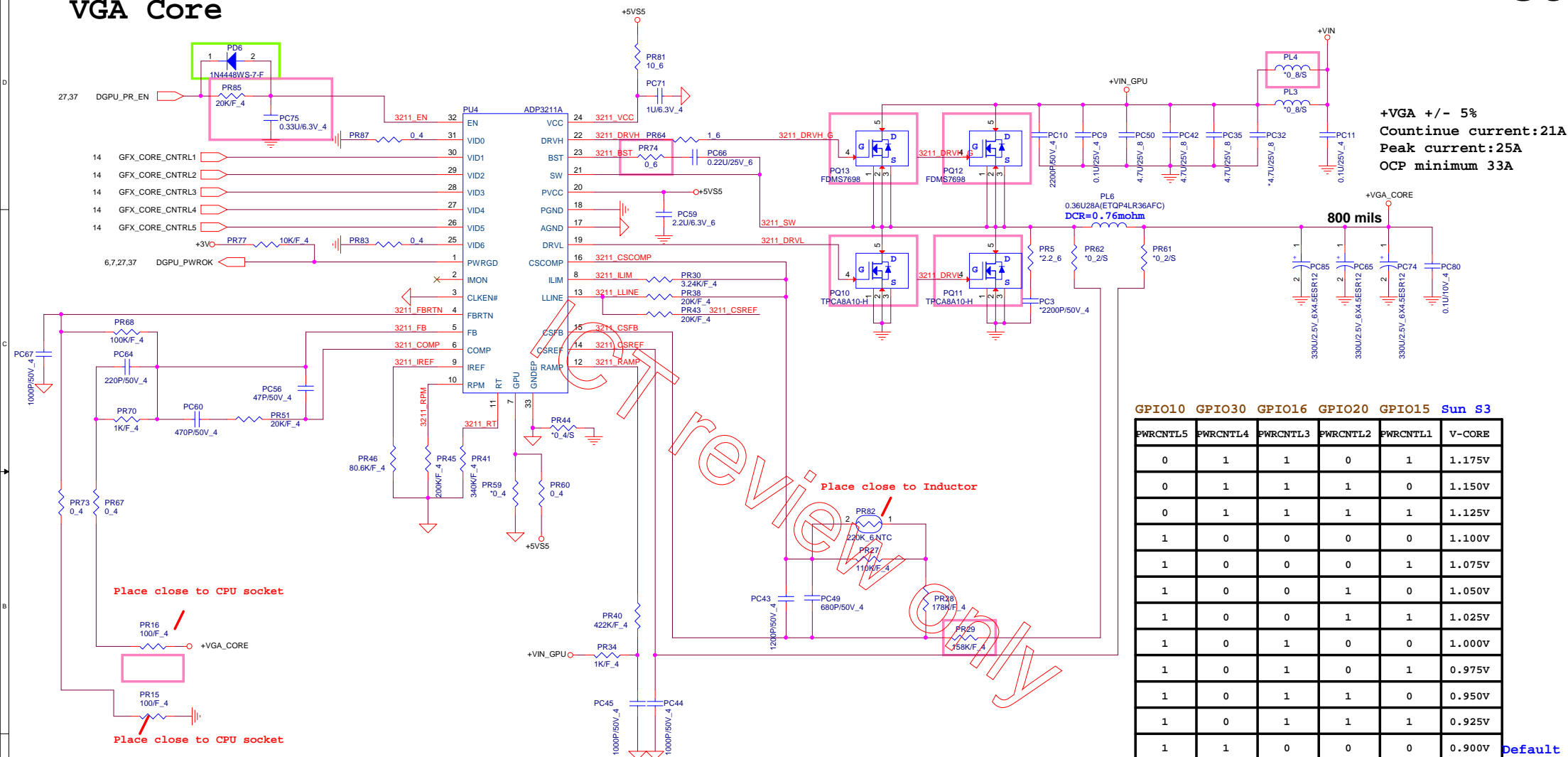


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VGA Core



GPIO10 GPIO30 GPIO16 GPIO20 GPIO15 Sun S3

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	0	1	1.175V
0	1	1	1	0	1.150V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

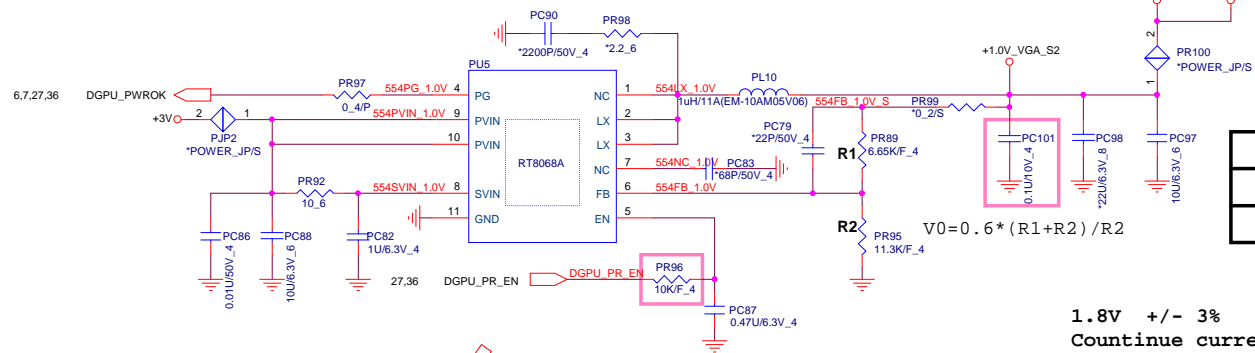
Default



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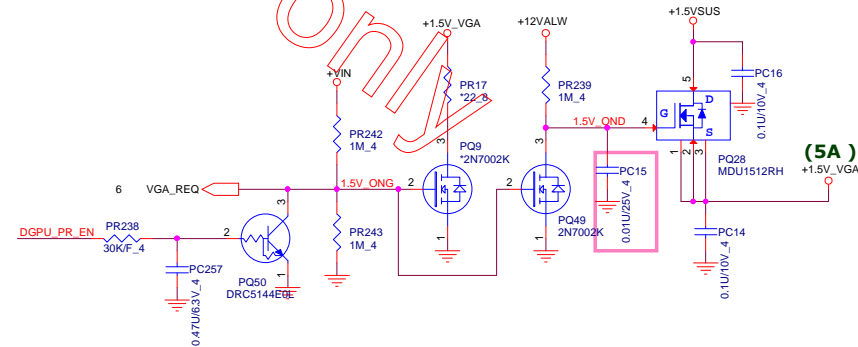
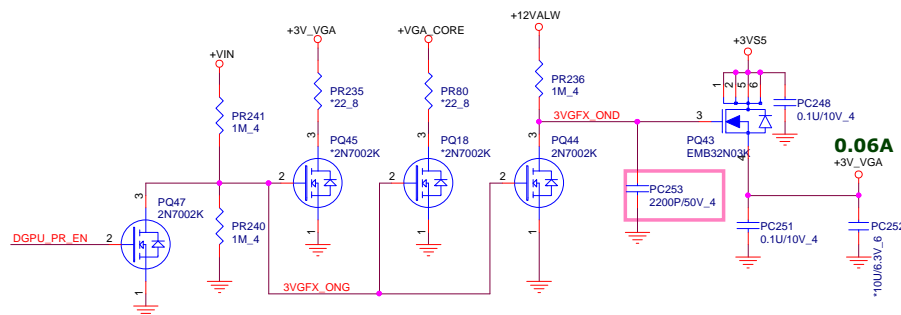
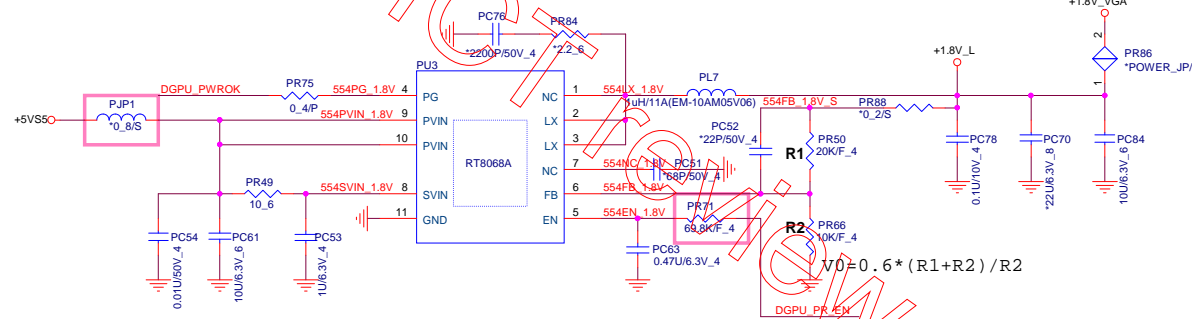
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+0.95V +/- 3%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4A



R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V

1.8V +/- 3%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4A



+3V_VGA 16
 +1.0V_VGA 13,14,16
 +12VALW 28,35
 +1.8V_VGA 13,14,16,26