R 3254

B.E/B.TECH.DEGREE EXAMINATION, NOV/DEC 2007.
Fifth Semester
Computer Science and Engineering
CS1304 – MICROPROCESSORS AND MICROCONTROLLERS
(Regulation 2004)
Time: Three hours Maximum: 100 marks
Answer ALL questions

PART A – (10 ´ 2 = 20 marks)

1. S, Cy, AxCY, P and Z flags.

2. SP stands for stack pointer. SP is a 8- bit wide register. It is incremented before data is stored during PUSH and CALL instructions. The stack array can reside anywhere in on-chip RAM.

3. STD: Set Direction flag
IRET: Returns from the ISR.

4. Macro is a group of instruction. The macro assembler generates the code in the program each time where the macro is called. Macros are defined by MACRO & ENDM directives. Creating macro is similar to creating new opcodes that can be used in the program.

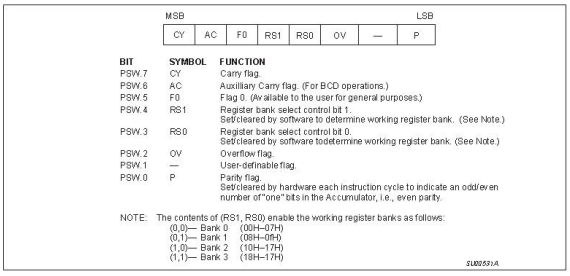
5. 8085 Microprocessor → 8255 PA0-PA7→ Water level indicating circuit

6. The numeric processor 8087 is a coprocessor which has been designed to work under the control of the processor 8086 and offer it additional numeric processing capabilities.

7. The device which can be programmed to perform Synchronous or Asynchronous serial communication is called USART (Universal Synchronous Asynchronous Receiver Transmitter). The INTEL 8251A is an example of USART

8. 64K I/O devices can be addressed.

9.



MSB							LSB
CY	AC	F0	RS1	RS0	OV	—	P

BIT	SYMBOL	FUNCTION
PSW.7	CY	Carry flag.
PSW.6	AC	Auxilliary Carry flag. (For BCD operations.)
PSW.5	F0	Flag 0. (Available to the user for general purposes.)
PSW.4	RS1	Register bank select control bit 1. Set/cleared by software to determine working register bank. (See Note.)
PSW.3	RS0	Register bank select control bit 0. Set/cleared by software todetermine working register bank. (See Note.)
PSW.2	OV	Overflow flag.
PSW.1	—	User-definable flag.
PSW.0	P	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of "one" bits in the Accumulator, i.e., even parity.

NOTE: The contents of (RS1, RS0) enable the working register banks as follows:
(0,0)— Bank 0 (00H–07H)
(0,1)— Bank 1 (08H–0fH)
(1,0)— Bank 2 (10H–17H)
(1,1)— Bank 3 (18H–17H)

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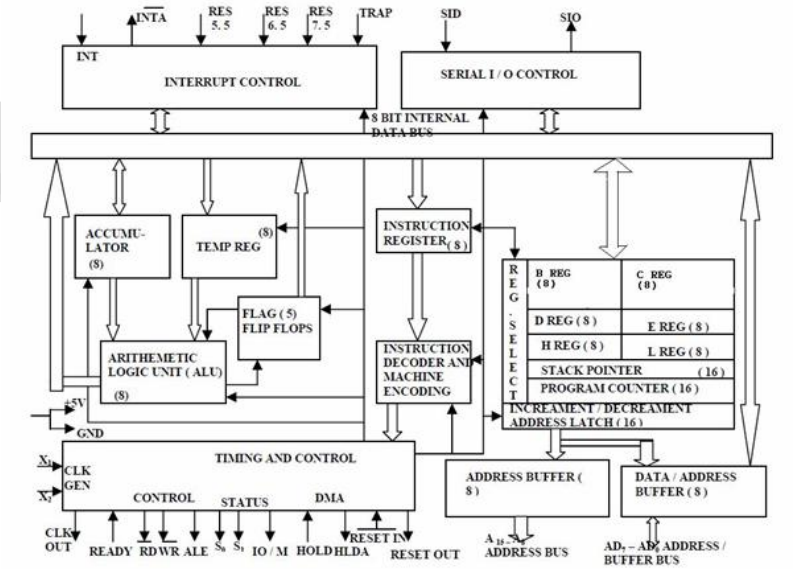
10. There are a number of addressing modes available to the 8051 instruction set, as follows:

Immediate Addressing
Register Addressing
Direct Addressing
Indirect Addressing
Relative Addressing
Absolute addressing
Long Addressing
Indexed Addressing

Part B

11. a)
Data transfer group – MOV, MVI, LXI.
Arithmetic group – ADD, SUB, INR.
Logical group –ANA, XRA, CMP.
Branch group – JMP, JNZ, CALL.
Stack I/O and Machine control group – PUSH, POP, IN, HLT.

(b) (i)



Registers
Accumulator or A register is an 8-bit register used for arithmetic, logic, I/O and load/store operations.

Flag is an 8-bit register containing 5 1-bit flags:

Sign - set if the most significant bit of the result is set.
Zero - set if the result is zero.
Auxiliary carry - set if there was a carry out from bit 3 to bit 4 of the result.
Parity - set if the parity (the number of set bits in the result) is even.
Carry - set if there was a carry during addition, or borrow during subtraction/comparison.
General registers:

8-bit B and 8-bit C registers can be used as one 16-bit BC register pair. When used as a pair the C register contains low-order byte. Some instructions may use BC register as a data pointer.
8-bit D and 8-bit E registers can be used as one 16-bit DE register pair. When used as a pair the E register contains low-order byte. Some instructions may use DE register as a data pointer.
8-bit H and 8-bit L registers can be used as one 16-bit HL register pair. When used as a pair the L register contains low-order byte. HL register usually contains a data pointer used to reference memory addresses.
Stack pointer is a 16 bit register. This register is always incremented/decremented by 2.
Program counter is a 16-bit register.

Interrupts

The processor has 5 interrupts. They are presented below in the order of their priority (from lowest to highest):

INTR is maskable 8080A compatible interrupt. When the interrupt occurs the processor fetches from the bus one instruction, usually one of these instructions:

One of the 8 RST instructions (RST0 - RST7). The processor saves current program counter into stack and branches to memory location N * 8 (where N is a 3-bit number from 0 to 7 supplied with the RST instruction).
CALL instruction (3 byte instruction). The processor calls the subroutine, address of which is specified in the second and third bytes of the instruction.
RST5.5 is a maskable interrupt. When this interrupt is received the processor saves the contents of the PC register into stack and branches to 2Ch (hexadecimal) address.

RST6.5 is a maskable interrupt. When this interrupt is received the processor saves the contents of the PC register into stack and branches to 34h (hexadecimal) address.

RST7.5 is a maskable interrupt. When this interrupt is received the processor saves the contents of the PC register into stack and branches to 3Ch (hexadecimal) address.

Trap is a non-maskable interrupt. When this interrupt is received the processor saves the contents of the PC register into stack and branches to 24h (hexadecimal) address.

All maskable interrupts can be enabled or disabled using EI and DI instructions. RST 5.5, RST6.5 and RST7.5 interrupts can be enabled or disabled individually using SIM instruction.
I/O ports
256 Input ports
256 Output ports

(ii)
```
LXI D, 4160
LXI H, 4150
MVI C, #05
MVI B, #00
L1:MOV A,M
RLC
JC L1
MOV A,M
STAX D
INR B
L1:DCR C
INX H
JNZ L1
LXI H,4160
MVI A, #00
L1: MOV C,M
ADD C
DCR B
INX H
JNZ L1
STA 4180
HLT
```

12. (a)

Stack structure: 8 marks

Explanation: 8 marks
The stack is a group of memory locations in the R/W memory that is used for the temporary storage of binary information during the execution of the program. The stack related instructions are PUSH & POP

(b) (i) Immediate addressing MOV BL, 26

Register addressing	MOV AL, BL
Direct addressing	MOV CL, [9823H]
Indirect addressing	MOV [DI], BX
Based addressing	MOV AL, LAST[BX]
Based Indexed addressing	MOV TOT[SI] [BX], CL
Relative addressing	JNZ BACK
Implied addressing	STC

(ii) The base address and the effective address or offset address are 16 bit wide. Using these 2 components 20 bit physical address can be calculated and can be used to access 1MB of memory space.

13. (a) The different interconnection topologies in multiprocessor systems:

1. Star topology
2. Bus Topology
3. Ring Topology 6 marks

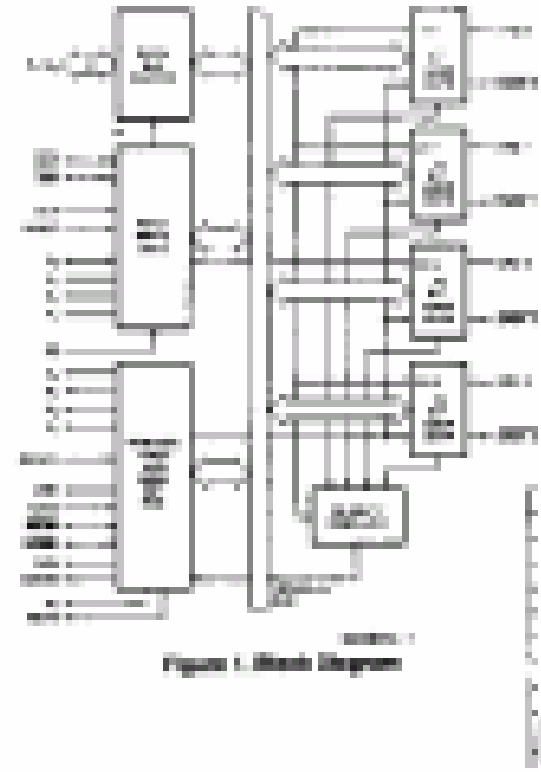
Explanation of above topologies 10 marks

(b)

In minimum mode configuration, AD0-AD15, A16/S3-A19/S6 and BHE/S7 signals are multiplexed. These signals are de multiplexed by external latches and ALE signal generated by the processor. This is done by 3 latch ICs (8282/8283). For interfacing memory module to 8086, it is necessary to have odd and even memory banks. This is implemented by using 2 EPROMs and 2 RAMs. D8-D15 are connected to odd bank and D0-D7 are connected to even bank.
Address lines are connected as per the capacity. RD' is connected to OE' signal of EPROM and RAM. WR' signal is connected to WR' signal of RAM.

In maximum mode configuration, the interfacing of memory and I/O deviceds are shown with the basic maximum mode configuration. The connections for memory and I/O devices are similar to that of minimum mode configuration. But the generation of control signals from 8086 is done by external bus controller 8288.

14. (a) Block diagram of 8257



Data Bus Buffer 8 marks

This three-state bi-directional, 8-bit buffer interfaces the 8257 to the system data bus. When the 8257 is being programmed by the CPU, eight bits of data for a DMA address register, a terminal count register, or the mode set register are received on the data bus. When the CPU reads the DMA address register, a terminal count, or the status register, the data is sent to the CPU over the data bus.

Read/Write Logic

When the CPU is programming or reading one of the 8257's registers (when 8257 is a slave device on the system bus), the read/write logic accepts the (I/OR) or (I/OW) signals and decodes the least significant four address bits, (A0-A3).

During DMA cycle the read/write logic generates the I/O read and memory write or I/O write and memory read signals which controls the data link with the peripheral that has been granted DMA cycle.

The different signals from the block are:

I/OR (I/O Read): It is active low bi-directional three-state line. In the slave mode, it is an input, which allows the 8-bit status register or upper/lower byte of a 16-bit DMA address register or terminal count register to be read. In the master mode, I/OR is a control output, which is used to access data from a peripheral during the DMA write cycle.

I/OW (I/O Write):

It is an active low bi-directional three-state line. In slave mode, it is an input, which

allows microprocessor to write. In the master mode, I/OW is a control output, which allows data to be output in the peripheral during DMA read cycle.
CLK (Clock Input):
This clock will be the clock output of the microprocessor. The complete operation depends on the cycle speed.
RESET: It is an asynchronous input. It disables all DMA channels by clearing the mode register and tri-states all control lines.
A0-A3 (Address Lines): These least significant four address lines are bi-directional. In the "slave" mode they are inputs, which select one of the registers to be read or programmed. In the 'master' mode, they are outputs, which constitute the most significant 4 bits of the 16-bit memory address generated in the 8257.
CS (Chip Select): It is an active low input, which enables the I/O, read or I/O write input when the 8257 is being read or programmed in the "slave" mode. In the master mode, CS is automatically disabled to prevent the chip from selecting while performing the DMA function.
Control Logic Block
This block controls contents of the sequence of operations during all DMA cycles by generating the appropriate control signals and 16-bit address that specifies the memory relations to be accessed.
A4-A7 (Address Lines): These four address lines are tri-stated outputs which contains 4 to 7 of the 16-bit memory address generated by the 8257 during all DMA cycles.

8 marks

(b) Block diagram of 8279 8 marks

- IC 8279 provides a scanned interface to a 64 contact key matrix, with two more keys CONTROL and SHIFT.
- It provides three input modes for keyboard interface.

1. Scanned keyboard mode
2. scanned sensor matrix mode
3. strobed input mode.

- It has built in hardware to provide key debounce.
- It allows in key depression in 2 key lockout or N key rollover mode, which eliminates software required to implement 2 key lockout.
- The interrupt output of 8279 can be used to tell CPU that the key press is detected, this eliminates the need of software polling.
- It provides multiplexed display interface with blanking and inhibit options.

8 marks

15. (a) 8-bit CPU
128 bytes of RAM
4K bytes of ROM
5 Interrupt sources
Two 16-bit Timers/Counters
One Full duplex serial port
Special Function Registers (SFR)
4 Parallel Ports (P0-P3)
The architecture or functional block diagram of 8051 is shown below:

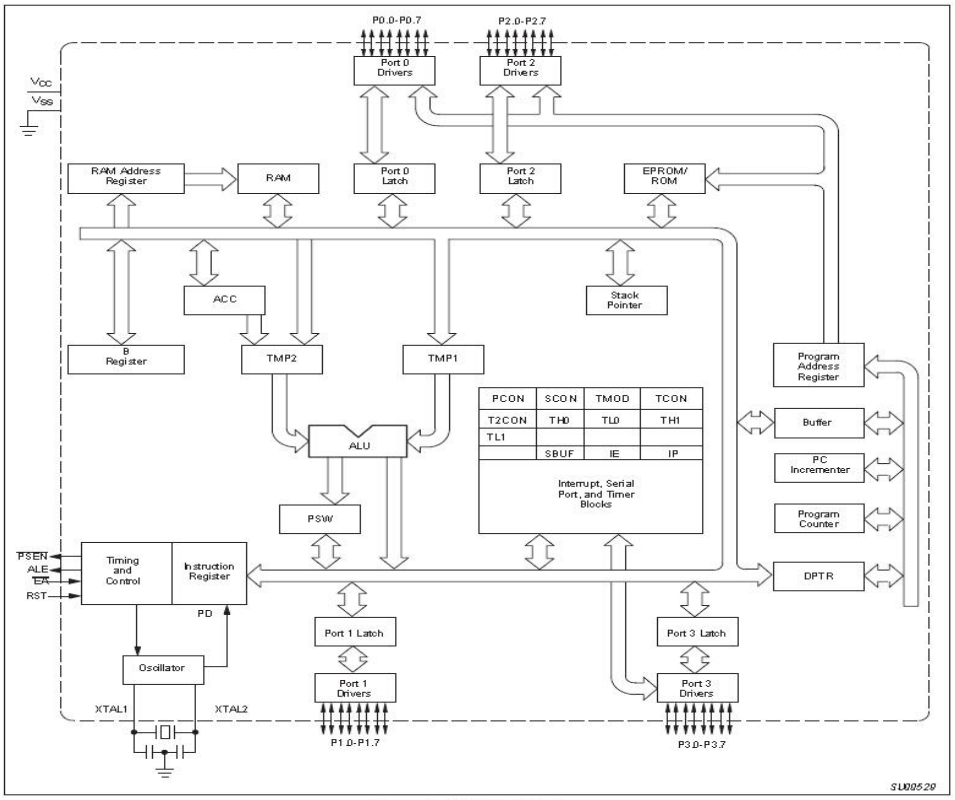


Figure 1. 80C51 Architecture

(b) (i) Memory addressing

Instructions to access external ROM
MOVC A, @A+DPTR
MOVC A, @A+PC

Instructions to access external data memory
MOVX A, @Rp
MOVX A, @DPTR
MOVX @Rp, A
MOVX @DPTR, A

5 marks

(ii) External I/O addressing

5 marks

(iii) The interrupts are:

Vector address

External interrupt 0 : IE0 : 0003H

Timer interrupt 0 : TF0 : 000BH

External interrupt 1 : IE1 : 0013H

Timer Interrupt 1 : TF1 : 001BH

Serial Interrupt

Receive interrupt : RI : 0023H

Transmit interrupt: TI : 0023H