1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

FINO M23

PROTO2

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
08		381734	ENGINEERING RELEASED	05/19/05	?

5/19/05

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10	12	1.5V Vreg	FINO-PC	05/18/2005
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18	24	Shasta Serial / Misc	FINO-ME	05/18/2005
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20	26	PULSAR2 CLOCKS	FINO-ME	05/18/2005
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23	29	SMU SUPPLEMENTAL (2)	FINO-MS	05/18/2005
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29	41	KODIAK EI PWR & CAPS	Q63	05/18/2005
30	42	KODIAK EI A	Q63	05/18/2005
31	43	CPU EI AND IO	FINO-MS	05/18/2005
32	44	KODIAK EI B	Q63	05/18/2005
33	47	CPU STRAPS	FINO-MS	05/18/2005
34	48	CPU POWER AND BYPASS	FINO-MS	05/18/2005
35	49	PROC DECOUPLING	FINO-MS	05/18/2005
36	50	CPU VCORE VREG	M23-MS	05/18/2005
37	52	CPU VCORE MORE BYPASS	FINO-MS	05/18/2005
38	54	CPU AVDD VREG	FINO-MS	05/18/2005
39	55	T,V,I SENSORS	FINO-MS	05/18/2005
40	56	CPU ALIASES & MISC	FINO-MS	05/18/2005
41	58	KODIAC NBMEM PWR & CAPS	Q63	05/18/2005
42	59	Kodiak Memory Dq/Ctl	FINO-RT	05/18/2005
43	61	Parallel Term	FINO-RT	05/18/2005
44	62	Main Memory Clock Buffer	FINO-RT	05/18/2005
45	63	MEMORY ADDR BRANCHING	FINO-EG	05/18/2005
46	67	Memory Dimm A	FINO-RT	05/18/2005
47	68	MLB Mem Series Term	FINO-RT	05/18/2005
48	69	On-Board DDR SDRAM	FINO-RT	05/18/2005
49	70	On-Board DDR SDRAM	FINO-RT	05/18/2005
50	82	KODIAK PCI-E X16	Q63	05/18/2005
51	84	GPU PCIe	FINO-DD	MASTER
52	85	Graphics Vregs	M23-DD	MASTER
53	86	GPU Core Power	FINO-DD	MASTER
54	87	GPU Frame Buffer	FINO-DD	MASTER
55	88	FB Series Termination	FINO-DD	MASTER
56	89	GPU GDDR SDRAM A	FINO-DD	MASTER
57	90	GPU GDDR SDRAM B	FINO-DD	MASTER
58	92	GPU Straps	FINO-DD	MASTER
59	93	GPU DVI & DACs	FINO-DD	MASTER
60	96	TMDS/Inverter/ExtVGA	M23-DD	MASTER
61	97	KODIAK PCI-E CONST	FINO-DD	MASTER
62	98	KODIAK HT16	Q63	05/18/2005
63	101	HT ALIASES	FINO-EG	05/18/2005
64	103	Shasta HyperTransport	Q63	05/18/2005
65	119	Shasta PCI Interface	Q63	05/18/2005
66	120	PCI SERIES TERMINATION	FINO-EG	05/18/2005
67	121	AIRPORT & BLUETOOTH	FINO-EG	05/18/2005
68	122	USB 2.0 PCI Interface	Q63	05/18/2005
69	125	BootROM	Q63	05/18/2005
70	127	Shasta Disk	M23-MB	05/18/2005
71	129	Disk Connectors	M23-MB	05/18/2005
72	130	ENET SERIES TERM	FINO-HC	05/18/2005
73	131	Shasta Ethernet	Q63	05/18/2005
74	132	Vesta Ethernet PHY	Q63	05/18/2005
75	136	ETHERNET CONNECTOR	FINO-HC	05/18/2005
76	138	Shasta FireWire	Q63	05/18/2005
77	139	Vesta FireWire PHY	Q63	05/18/2005
78	140	FIREWIRE CONNECTORS	FINO-HC	05/18/2005
79	142	USB Host Interfaces	Q63	05/18/2005
80	143	USB Device Interfaces	FINO-MB	05/18/2005
81	144	Flash Media Ctrl	FINO-PC	05/18/2005
82	145	Flash Connector	FINO-PC	05/18/2005
83	147	AUDIO: CODEC	FINO-SO	05/18/2005
84	148	AUDIO: LINE INPUT AMP	FINO-SO	05/18/2005
85	150	AUDIO: LINE OUT AMP	FINO-SO	05/18/2005
86	152	AUDIO: SPEAKER AMP	FINO-SO	05/18/2005
87	153	AUDIO: CONNECTORS	FINO-SO	05/18/2005
88	154	AUDIO: POWER SUPPLIES	FINO-SO	05/18/2005

PRELIMINARY

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER / DESIGN CK / ENG APPD / MFG APPD / QA APPD / DESIGNER / RELEASE / SCALE NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

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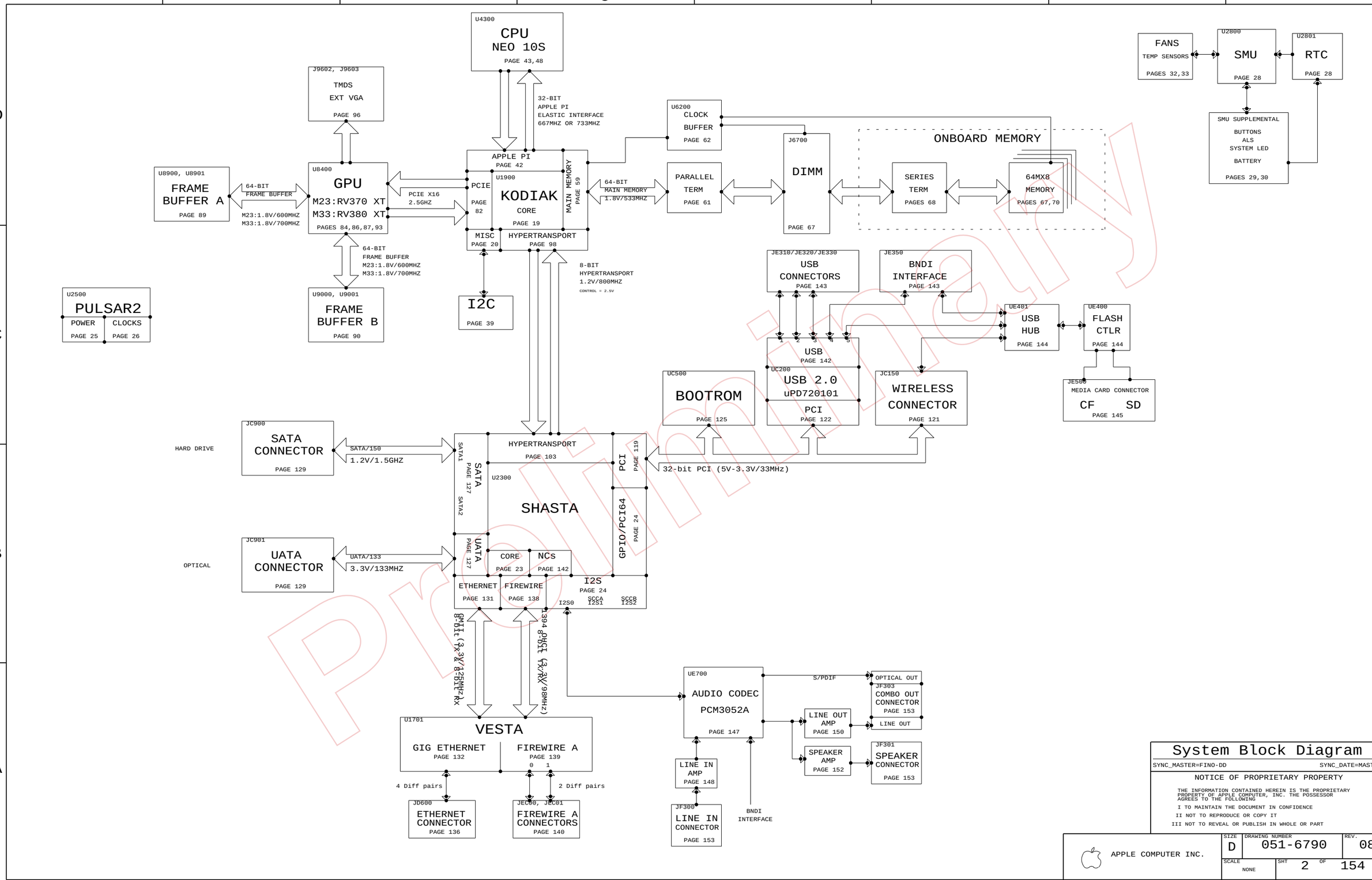
TITLE
SCH,MLB,FINO,M23

DRAWING NUMBER 051-6790 REV. 08



System Block Diagram

SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

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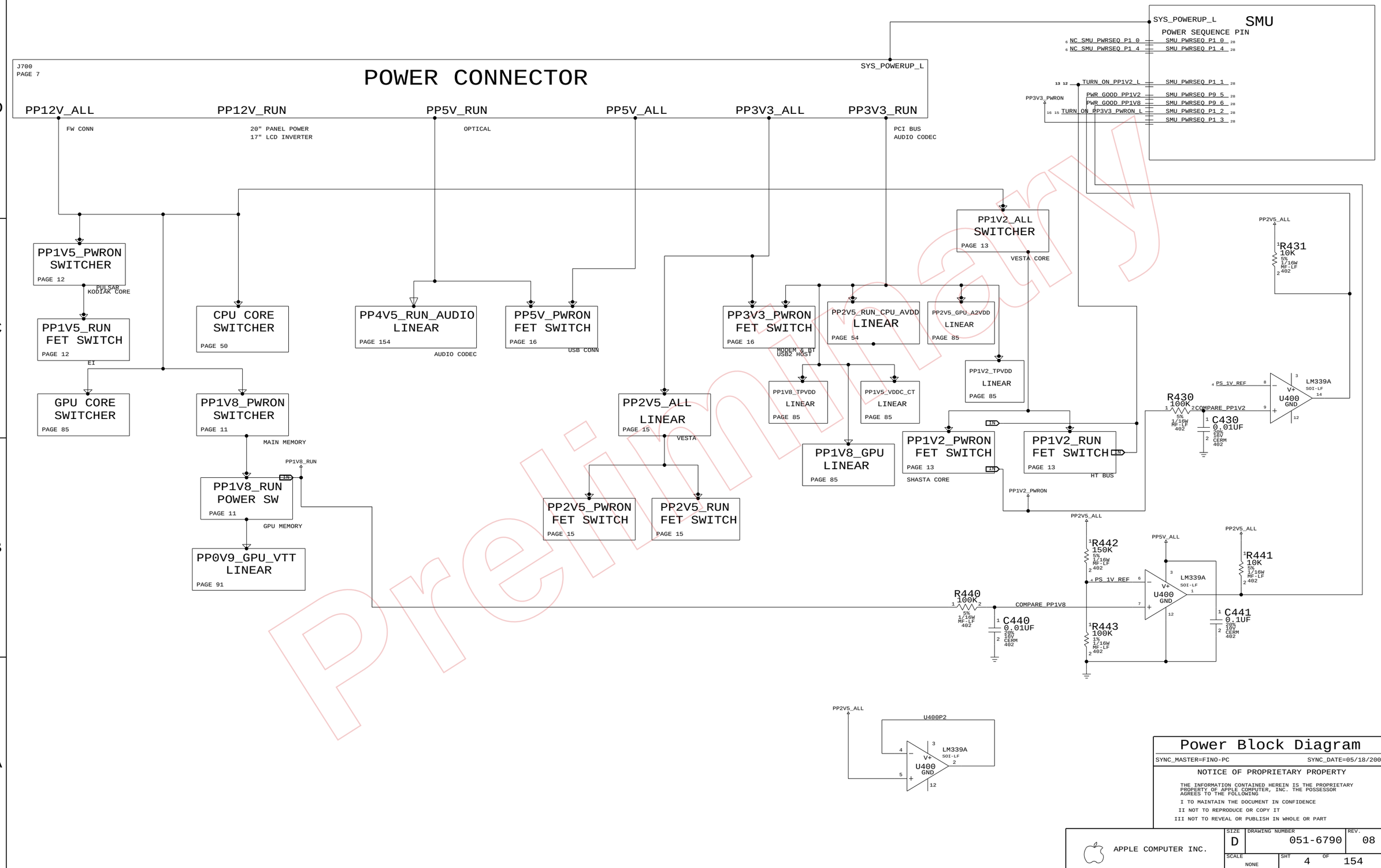
SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE NONE SHT 2 OF 154

Proprietary



Power Block Diagram

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D	051-6790	08
SCALE NONE	SHT 4 OF 154	

Preliminary

PROCESSORS

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3158	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.0G,85C,CQA	2.0GHZ	1.15V	46W	50MV	U4300	CPU_2_0GHZ
337S3157	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.2G,85C,FQA	2.2GHZ	1.15V	51W	50MV	U4300	CPU_2_2GHZ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	VOLTAGE
337S3165	337S3158	CPU_2_0GHZ	U4300	IC,DD3.1,2.0G,CJA	1.20V
337S3164	337S3157	CPU_2_2GHZ	U4300	IC,DD3.1,2.0G,FJA	1.20V

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0371	1	IC,KODIAK,V1.1,PBGA,200MM	U1900	
343S0283	1	IC,ASIC,SHASTA,V1.1,PBGA	U2300	
343S0324	1	IC,ASIC,VESTA,V1.3	U1701	
343S0319	1	IC,PULSAR2,100P,P8MM,BGA	U2500	

MISC PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6790	1	PCB,SCHEM,MLB,M23	SCH1	17_INCH_LCD
051-6863	1	PCB,SCHEM,MLB,M33	SCH1	20_INCH_LCD
820-1783	1	PCB,FAB,MLB,M23	MLB1	17_INCH_LCD
820-1766	1	PCB,FAB,MLB,M33	MLB1	20_INCH_LCD
062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VPP1	
825-6447	1	BARCODE LABEL, MLB	LBL1	
341T1751	1	IC,FLASH,1MX8,3.3V,90NS	UC500	
341T1752	1	PURCH ASSY, SMU BIG	U2800	
603-7318	1	M23 CPU HEATSINK	MECH1	17_INCH_LCD
603-7321	1	M33 CPU HEATSINK	MECH1	20_INCH_LCD
603-7322	1	M33 GPU HEATSINK	MECH2	20_INCH_LCD
875-1614	1	CPU GAP FILLER	GAP1	

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0119	378S0114		LED700,LED702	KINGBRIGHT LED
376S0204	376S0130		Q5010,Q5020	MOSFET,N-CH,VISHAY
376S0207	376S0146		Q5011,Q5021	MOSFET,N-CH,VISHAY

Preliminary

Table Items

SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

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SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 5 OF 154	

NO TEST XW NETS

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NO_TEST=YES PP_3V3PWRONSBPCI64 23
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NO_TEST=YES PP_1V2PWRONSBPLL45VDD 24
NO_TEST=YES PP_OVDD_PULSAR1 25
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NO_TEST=YES PP_3V3ALLSMUAVCC 28
NO_TEST=YES PP_3V3ALLSMU 28
NO_TEST=YES PP_VEINB 41
NO_TEST=YES GND_CPU_AVDD 48
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NO_TEST=YES VC_OUTSEN_R 50
NO_TEST=YES KPVDD2_FMAX 55
NO_TEST=YES GND_GPU_PVSS 86
NO_TEST=YES GND_GPU_MPVSS 87
NO_TEST=YES GND_AUDIO_MIC 153 154

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NO_TEST=YES PP2V5_VESTA_XTALVDD1 132
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NO_TEST=YES PCI_CLK66M_SB_INT_R 26
NO_TEST=YES Q800_D 8
NO_TEST=YES Q800_G 8
NO_TEST=YES Q801_B 8
NO_TEST=YES Q802_B 8
NO_TEST=YES Q802_E 8
NO_TEST=YES Q803_B 8
NO_TEST=YES TP_USB2_PWREN<0> 143
NO_TEST=YES TP_USB2_PWREN<1> 143
NO_TEST=YES TP_SB_FSTEST 24
NO_TEST=YES TP_SB_PLLTEST 24
NO_TEST=YES TP_USB2_PWREN<2> 143
NO_TEST=YES TP_USB2_PWREN<3> 143
NO_TEST=YES TP_USB2_PWREN<4> 143
NO_TEST=YES TP_NEC_NTEST1 122
NO_TEST=YES TP_NEC_SMC 122
NO_TEST=YES TP_NEC_SMI_L 122
NO_TEST=YES TP_NEC_SRCLK 122
NO_TEST=YES TP_NEC_SRMOD 122
NO_TEST=YES TP_NEC_TEST 122
NO_TEST=YES UATA_DASP_L_DS 129

NO_TEST=YES RFBD<19> 88 89
NO_TEST=YES RFBD<18> 88 89

NO_TEST=YES RFBD<16> 88 89
NO_TEST=YES RFBD<15> 88 89
NO_TEST=YES RFBD<14> 88 89
NO_TEST=YES RFBD<13> 88 89

NO_TEST=YES RFBD<11> 88 89
NO_TEST=YES RFBD<10> 88 89

NO_TEST=YES RFBD<8> 88 89
NO_TEST=YES RFBD<7> 88 89
NO_TEST=YES RFBD<6> 88 89
NO_TEST=YES RFBD<5> 88 89

NO_TEST=YES RFBD<3> 88 89
NO_TEST=YES RFBD<2> 88 89
NO_TEST=YES RFBD<1> 88 89
NO_TEST=YES RAM_DQ_R<63> 61 68 70

NO_TEST=YES RAM_DQ_R<60> 61 68 70
NO_TEST=YES RAM_DQ_R<59> 61 68 70
NO_TEST=YES RAM_DQ_R<58> 61 68 70
NO_TEST=YES RAM_DQ_R<57> 61 68 70
NO_TEST=YES RAM_DQ_R<56> 61 68 70

NO_TEST=YES RAM_DQ_R<54> 61 68 70
NO_TEST=YES RAM_DQ_R<53> 61 68 70
NO_TEST=YES RAM_DQ_R<52> 61 68 70

NO_TEST=YES RAM_DQ_R<50> 61 68 70
NO_TEST=YES RAM_DQ_R<49> 61 68 70
NO_TEST=YES RAM_DQ_R<48> 61 68 70

NO_TEST=YES RAM_DQ_R<46> 61 68 70
NO_TEST=YES RAM_DQ_R<45> 61 68 70
NO_TEST=YES RAM_DQ_R<44> 61 68 70
NO_TEST=YES RAM_DQ_R<43> 61 68 70

NO_TEST=YES RAM_DQ_R<41> 61 68 70
NO_TEST=YES RAM_DQ_R<40> 61 68 70
NO_TEST=YES RAM_DQ_R<39> 61 68 70
NO_TEST=YES RAM_DQ_R<38> 61 68 70

NO_TEST=YES RAM_DQ_R<36> 61 68 70

NO_TEST=YES RAM_DQ_R<34> 61 68 70
NO_TEST=YES RAM_DQ_R<33> 61 68 70
NO_TEST=YES RAM_DQ_R<32> 61 68 70

NO_TEST=YES RAM_DQ_R<30> 61 68 69
NO_TEST=YES RAM_DQ_R<29> 61 68 69
NO_TEST=YES RAM_DQ_R<28> 61 68 69

NO_TEST=YES RAM_DQ_R<26> 61 68 69
NO_TEST=YES RAM_DQ_R<25> 61 68 69
NO_TEST=YES RAM_DQ_R<24> 61 68 69

NO_TEST=YES RAM_DQ_R<22> 61 68 69
NO_TEST=YES RAM_DQ_R<21> 61 68 69
NO_TEST=YES RAM_DQ_R<20> 61 68 69
NO_TEST=YES RAM_DQ_R<19> 61 68 69

NO_TEST=YES RAM_DQ_R<17> 61 68 69
NO_TEST=YES RAM_DQ_R<16> 61 68 69

NO_TEST=YES RAM_DQ_R<14> 61 68 69
NO_TEST=YES RAM_DQ_R<13> 61 68 69
NO_TEST=YES RAM_DQ_R<12> 61 68 69
NO_TEST=YES RAM_DQ_R<11> 61 68 69

FUNC TEST NETS

NOTES FROM TOM FUSSELMAN

PLACE TWO TEST POINTS ON TOP SIDE
FOR PP3V3_ALL AND GND
PLACE WITHIN 1 INCH OF EACH OTHER
USE FAT TRACES

FUNC_TEST=TRUE PPVCORE_CPU 50
FUNC_TEST=TRUE =PP3V3_ALL_SMU 7 28 29
FUNC_TEST=TRUE =PP5V_RUN_CPU 7 8

FUNC_TEST=TRUE SYS_POWER_BUTTON_L 28 29
FUNC_TEST=TRUE POWER_BUTTON_L 29
FUNC_TEST=TRUE RESET_BUTTON_L 29
FUNC_TEST=TRUE SMU_RESET_L 28 29
FUNC_TEST=TRUE SYS_POWERUP_L 7 12 28 50 85

TOP SIDE ONLY

FUNC_TEST=TRUE SMU_BOOT_SCLK 28 29
FUNC_TEST=TRUE SMU_BOOT_RXD 28 29
FUNC_TEST=TRUE SMU_BOOT_CE 28 29
FUNC_TEST=TRUE SMU_BOOT_CNVSS 28 29
FUNC_TEST=TRUE SMU_BOOT_TXD 28 29
FUNC_TEST=TRUE SMU_BOOT_BUSY 28 29
FUNC_TEST=TRUE SMU_MANUAL_RESET_L 29

PP1V2_ALL PP3V3_ALL PP5V_ALL
7 PP1V2_ALL FUNC_TEST=TRUE
7 PP3V3_ALL FUNC_TEST=TRUE
7 PP5V_ALL FUNC_TEST=TRUE

PP1V8_RUN PP2V5_RUN PP3V3_RUN PP12V_RUN
7 PP1V8_RUN FUNC_TEST=TRUE
7 PP2V5_RUN FUNC_TEST=TRUE
7 PP3V3_RUN FUNC_TEST=TRUE
7 PP12V_RUN FUNC_TEST=TRUE

PP1V5_PWRON
7 PP1V5_PWRON FUNC_TEST=TRUE

GND FUNC_TEST=TRUE

NO_TEST=YES RAM_DQ_R<10> 61 68 69

NO_TEST=YES RAM_DQ_R<8> 61 68 69
NO_TEST=YES RAM_DQ_R<7> 61 68 69
NO_TEST=YES RAM_DQ_R<6> 61 68 69
NO_TEST=YES RAM_DQ_R<5> 61 68 69

NO_TEST=YES RAM_DQ_R<3> 61 68 69
NO_TEST=YES RAM_DQ_R<2> 61 68 69
NO_TEST=YES RAM_DQ_R<1> 61 68 69

FUNC TEST 1 OF 2

SYNC_MASTER=FINO-ME SYNC_DATE=05/18/2005

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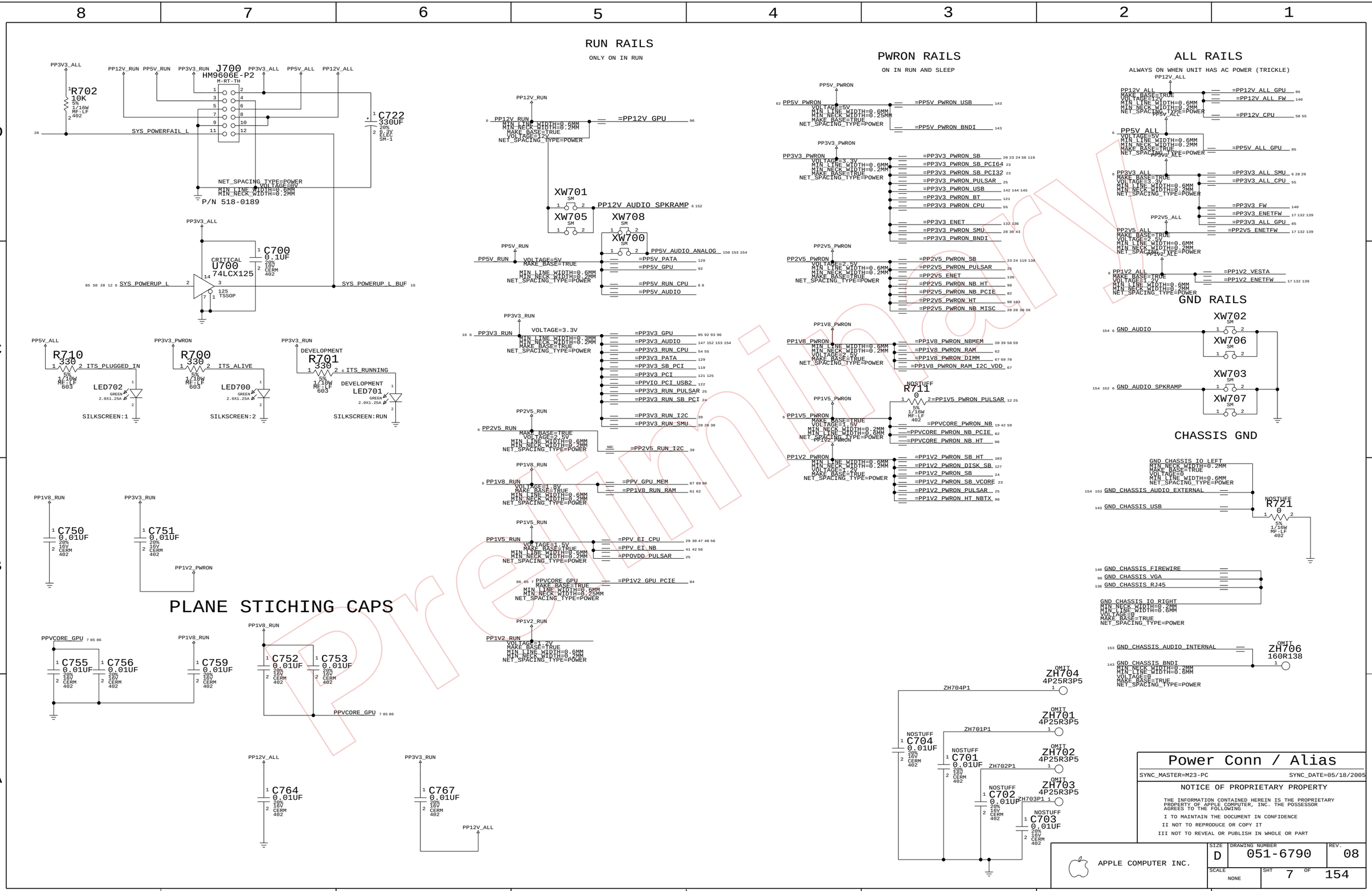
APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6790 | REV. 08
SCALE NONE | SHT 6 OF 154

preliminary


RUN RAILS
ONLY ON IN RUN
PWRON RAILS
ON IN RUN AND SLEEP
ALL RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)
GND RAILS
CHASSIS GND
PLANE STICHING CAPS
J700 HM9606E-P2
R702 10K
C722 330UF
P/N 518-0189
C700 0.1UF
U700 74LCX125
R710 330 ITS_PLUGGED_IN
LED702
SILKSCREEN:1
R700 330 ITS_ALIVE
LED700
SILKSCREEN:2
R701 330 ITS_RUNNING
LED701
SILKSCREEN:RUN
XW701
XW705
XW708
XW700
XW702
XW706
XW703
XW707
R711 0
R721 0
ZH704 4P25R3P5
ZH701 4P25R3P5
ZH702 4P25R3P5
ZH703 4P25R3P5
ZH706 160R138
C704 0.01UF
C701 0.01UF
C702 0.01UF
C703 0.01UF
C750 0.01UF
C751 0.01UF
C755 0.01UF
C756 0.01UF
C759 0.01UF
C752 0.01UF
C753 0.01UF
C764 0.01UF
C767 0.01UF
Power Conn / Alias
SYNC_MASTER=M23-PC
SYNC_DATE=05/18/2005
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REV. 08
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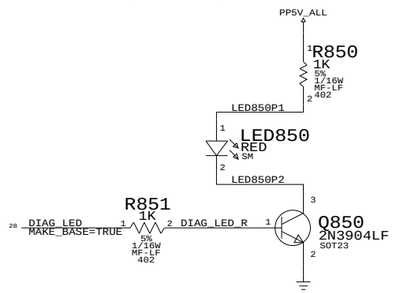
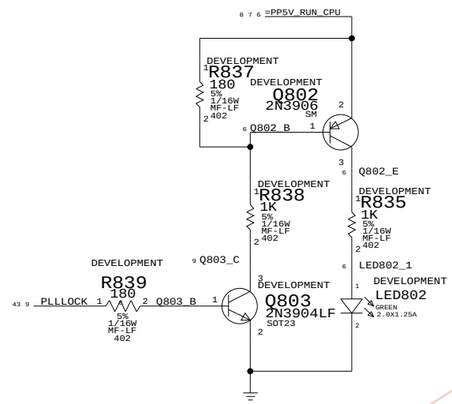
SHT 7 OF 154

DIAG LED

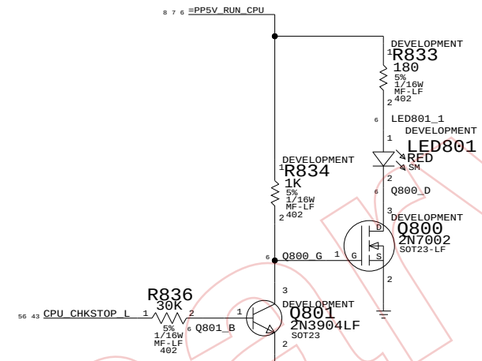
(OVERTEMP LED)



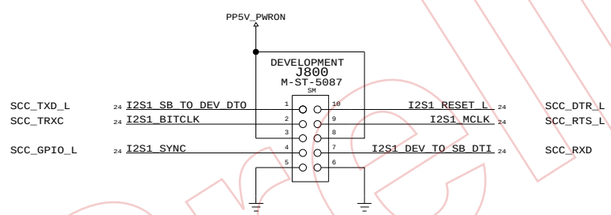
PLL LOCK LED



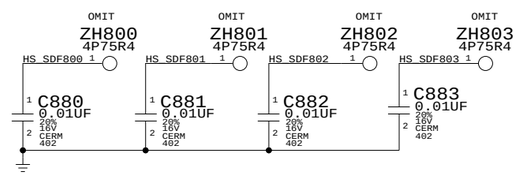
CHKSTOP LED



SERIAL DEBUG



CPU HEATSINK MOUNTING HOLES



Preliminary

Signal Alias

SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 8 OF 154	

I1	NO_TEST=YES	ENET_TXD_R<7>	130 131
I2	NO_TEST=YES	ENET_TXD_R<6>	130 131
I3	NO_TEST=YES	ENET_TXD_R<5>	130 131
I4	NO_TEST=YES	ENET_TXD_R<4>	130 131
I5	NO_TEST=YES	ENET_TXD_R<3>	130 131
I6	NO_TEST=YES	ENET_TXD_R<2>	130 131
I7	NO_TEST=YES	ENET_TXD_R<1>	130 131
I8	NO_TEST=YES	ENET_TXD_R<0>	130 131
I9	NO_TEST=YES	ENET_TXD<7>	130 131 132
I10	NO_TEST=YES	ENET_TXD<6>	130 131 132
I12	NO_TEST=YES	ENET_TXD<5>	130 131 132
I11	NO_TEST=YES	ENET_TXD<4>	130 131 132
I13	NO_TEST=YES	ENET_TXD<3>	130 131 132
I14	NO_TEST=YES	ENET_TXD<2>	130 131 132
I15	NO_TEST=YES	ENET_TXD<1>	130 131 132
I16	NO_TEST=YES	ENET_TXD<0>	130 131 132
I18	NO_TEST=YES	ENET_RXD_R<7>	130 131 132
I17	NO_TEST=YES	ENET_RXD_R<6>	130 131 132
I19	NO_TEST=YES	ENET_RXD_R<5>	130 131 132
I20	NO_TEST=YES	ENET_RXD_R<4>	130 131 132
I21	NO_TEST=YES	ENET_RXD_R<3>	130 131 132
I22	NO_TEST=YES	ENET_RXD_R<2>	130 131 132
I24	NO_TEST=YES	ENET_RXD_R<1>	130 131 132
I23	NO_TEST=YES	ENET_RXD_R<0>	130 131 132
I25	NO_TEST=YES	ENET_RXD<7>	130 131
I26	NO_TEST=YES	ENET_RXD<6>	130 131
I27	NO_TEST=YES	ENET_RXD<5>	130 131
I28	NO_TEST=YES	ENET_RXD<4>	130 131
I30	NO_TEST=YES	ENET_RXD<3>	130 131
I29	NO_TEST=YES	ENET_RXD<2>	130 131
I31	NO_TEST=YES	ENET_RXD<1>	130 131
I32	NO_TEST=YES	ENET_RXD<0>	130 131
I33	NO_TEST=YES	ENET_TX_EN_R	130 131
I34	NO_TEST=YES	ENET_TX_ER_R	130 131
I36	NO_TEST=YES	ENET_TX_EN	130 131 132
I35	NO_TEST=YES	ENET_TX_ER	130 131 132
I37	NO_TEST=YES	TP_HT_MB_TO_NB_CLK_N<1>	101
I38	NO_TEST=YES	TP_HT_MB_TO_NB_CLK_P<1>	101
I39	NO_TEST=YES	NC_CPU_AFN	56
I40	NO_TEST=YES	NC_I2C_SMU_CPU_SCL_IN	31
I42	NO_TEST=YES	NC_PSRO	56
I41	NO_TEST=YES	NC_PSRO_ENABLE	56
I43	NO_TEST=YES	NC_SLOT_TOTAL_PWR	31
I44	NO_TEST=YES	NC_SMU_CPU_VID_LE0	31
I45	NO_TEST=YES	NC_SMU_CPU_VID_LE1	31
I46	NO_TEST=YES	NC_SMU_FAN_RPM3	31
I48	NO_TEST=YES	NC_SMU_FAN_RPM4	31
I47	NO_TEST=YES	NC_SMU_FAN_RPM5	31
I49	NO_TEST=YES	NC_SMU_FAN_TACH3	31
I50	NO_TEST=YES	NC_SMU_FAN_TACH4	31
I51	NO_TEST=YES	NC_SMU_FAN_TACH5	31
I52	NO_TEST=YES	NC_SMU_FAN_TACH7	31
I54	NO_TEST=YES	NC_SMU_SER_SEL	31
I53	NO_TEST=YES	NC_SYS_DOOR_AJAR_L	31
I55	NO_TEST=YES	TP_VESTA_2_5V_EN	17
I56	NO_TEST=YES	TP_VESTA_AN_EN	132
I57	NO_TEST=YES	TP_VESTA_DNC_C9	17
I58	NO_TEST=YES	TP_VESTA_DNC_E9	17
I60	NO_TEST=YES	TP_VESTA_EN_10B	132
I59	NO_TEST=YES	TP_VESTA_ER	132
I61	NO_TEST=YES	TP_VESTA_F1000	132
I62	NO_TEST=YES	TP_VESTA_FDX	132
I63	NO_TEST=YES	TP_VESTA_FDXLED_L	132
I64	NO_TEST=YES	TP_VESTA_HUB	132
I66	NO_TEST=YES	TP_VESTA_LINK1_L	132
I65	NO_TEST=YES	TP_VESTA_LINK2_L	132
I67	NO_TEST=YES	TP_VESTA_MANMS	132
I68	NO_TEST=YES	TP_VESTA_PHYA<0>	132
I69	NO_TEST=YES	TP_VESTA_PHYA<1>	132
I70	NO_TEST=YES	TP_VESTA_PHYA<2>	132
I72	NO_TEST=YES	TP_VESTA_PHYA<3>	132
I71	NO_TEST=YES	TP_VESTA_PHYA<4>	132
I73	NO_TEST=YES	TP_VESTA_RBC0	132
I74	NO_TEST=YES	TP_VESTA_RBC1	132
I75	NO_TEST=YES	TP_VESTA_REGCTL1	17
I76	NO_TEST=YES	TP_VESTA_REGCTL2	17
I78	NO_TEST=YES	TP_VESTA_REGSEN1	17
I77	NO_TEST=YES	TP_VESTA_REGSEN2	17
I79	NO_TEST=YES	TP_VESTA_REGSUP1	17
I80	NO_TEST=YES	TP_VESTA_REGSUP2	17
I81	NO_TEST=YES	TP_VESTA_RGMIIEN	132
I82	NO_TEST=YES	TP_VESTA_SPD0	132
I84	NO_TEST=YES	TP_VESTA_TDBL<0>	139
I83	NO_TEST=YES	TP_VESTA_TDBL<1>	139
I85	NO_TEST=YES	TP_VESTA_TDBL<2>	139
I86	NO_TEST=YES	TP_VESTA_TEST<0>	132
I87	NO_TEST=YES	TP_VESTA_TEST<1>	132
I88	NO_TEST=YES	TP_VESTA_TEST_1394<0>	139
I90	NO_TEST=YES	TP_VESTA_TEST_1394<1>	139
I89	NO_TEST=YES	TP_VESTA_TVCO	132
I222	NO_TEST=YES	CARD_READER_ACTIVITY_R	144
I223	NO_TEST=YES	TP_VESTA_FAVDDL	139
I223	NO_TEST=YES	TP_NB_A_TRIGGER_OUT	56
I223	NO_TEST=YES	TP_NB_B_TRIGGER_OUT	56

I91	NO_TEST=YES	TP_VESTA_TVCO_24	139
I92	NO_TEST=YES	TP_VESTA_TXC_RXC_DELAY	132
I93	NO_TEST=YES	TP_I2S2_SB_TO_DEV_DTO	154
I94	NO_TEST=YES	TP_NB_APSYNC	44
I95	NO_TEST=YES	TP_SB_WATCHDOG	24
I96	NO_TEST=YES	NC_CPU_TBEN_CLK	27
I97	NO_TEST=YES	NC_J3108_10	31
I98	NO_TEST=YES	NC_J3108_11	31
I99	NO_TEST=YES	NC_J3108_12	31
I100	NO_TEST=YES	NC_J3108_8	31
I101	NO_TEST=YES	NC_J3108_9	31
I102	NO_TEST=YES	NC_JTAGMUX_3	30
I103	NO_TEST=YES	NC_PP1V5_PULSAR	12

THE FOLLOWING NETS ARE USED ONLY
WHEN THE DEVELOPMENT BOM OPTION IS ENABLED

I108	NO_TEST=YES	Q803_C	8
I109	NO_TEST=YES	PLLLOCK	8 43
I110	NO_TEST=YES	LED_PP1V8_RUN_P	11
I111	NO_TEST=YES	LED_PP1V8_RUN_N	11
I112	NO_TEST=YES	PP1V5_RUN_FOR_LED	12
I113	NO_TEST=YES	LED_PP1V5_RUN_N	12
I114	NO_TEST=YES	LED_PP1V5_RUN_P	12
I115	NO_TEST=YES	PULSAR_1V5_RUN_SWITCH	12
I120	NO_TEST=YES	PP1V2_RUN_FOR_LED	13
I121	NO_TEST=YES	LED_PP1V2_RUN_N	13
I122	NO_TEST=YES	LED_PP1V2_RUN_P	13
I123	NO_TEST=YES	KP_V<1>	55
I124	NO_TEST=YES	KP_V<2>	55
I125	NO_TEST=YES	CPU_SENSE_KP_V	55
I126	NO_TEST=YES	NB_PLL_OUT_TRG_R	
I127	NO_TEST=YES	NB_PLL_OUT_TRG	59
I128	NO_TEST=YES	PP5V_T555	92
I131	NO_TEST=YES	T555_DISC	92
I132	NO_TEST=YES	T555_THRES	92
I129	NO_TEST=YES	T555_OUT	92
I130	NO_TEST=YES	T555_PWM	92
I133	NO_TEST=YES	PP3V3_GPU_TSENSE	
I134	NO_TEST=YES	TSENSE_GPU_OVERTEMP_L	93
I135	NO_TEST=YES	TSENSE_GPU_ADD0	93
I136	NO_TEST=YES	TSENSE_GPU_ADD1	93
I137	NO_TEST=YES	GPU_DIODE_PLUS	93
I138	NO_TEST=YES	GPU_DIODE_MINUS	93
I139	NO_TEST=YES	LED8700_P	136
I140	NO_TEST=YES	LED8701_P	136

THE FOLLOWING PULSAR NETS WILL BE
TESTED VIA TEST JET

I143	NO_TEST=YES	CPU_A_TBEN_CLK_R	26
I144	NO_TEST=YES	CPU_B_TBEN_CLK_R	26
I145	NO_TEST=YES	CPU_A_APSYNC_R	26
I146	NO_TEST=YES	CPU_B_APSYNC_R	26
I148	NO_TEST=YES	NB_APSYNC_R	26
I149	NO_TEST=YES	HT_SB_REFCLK_R	26
I147	NO_TEST=YES	HT_NB_REFCLK_H0_R	26
I150	NO_TEST=YES	HT_NB_REFCLK_L0_R	26
I151	NO_TEST=YES	CLK_RAIREF_200M_P_R	26
I152	NO_TEST=YES	CLK_RAIREF_200M_N_R	26
I153	NO_TEST=YES	NB_PMR_CLK_P_R	26
I154	NO_TEST=YES	NB_PMR_CLK_N_R	26
I155	NO_TEST=YES	NB_PCIE_REFCLK_P_C	26
I156	NO_TEST=YES	NB_PCIE_REFCLK_N_C	26
I158	NO_TEST=YES	GFX_SLOT_PCIE_REFCLK_P_C	26
I159	NO_TEST=YES	GFX_SLOT_PCIE_REFCLK_N_C	26
I157	NO_TEST=YES	PCIE_A_REFCLKIN_P_C	26
I160	NO_TEST=YES	PCIE_A_REFCLKIN_N_C	26
I159	NO_TEST=YES	PCIE_B_REFCLKIN_P_C	26
I161	NO_TEST=YES	PCIE_B_REFCLKIN_N_C	26
I162	NO_TEST=YES	PCIE_C_REFCLKIN_P_C	26
I163	NO_TEST=YES	PCIE_C_REFCLKIN_N_C	26
I164	NO_TEST=YES	NB_DDR_REFCLK_P_R	26
I165	NO_TEST=YES	NB_DDR_REFCLK_N_R	26
I166	NO_TEST=YES	CLK_RAI_GIGE_25MHZ_R	26
I168	NO_TEST=YES	QUA0_REF_25MHZ_R	26
I167	NO_TEST=YES	SB_CLK25M_SATA_R	26
I169	NO_TEST=YES	QUA1_REF_25MHZ_R	26
I170	NO_TEST=YES	PCI_CLK33M_SB_EXT_R	26
I172	NO_TEST=YES	SB_AIRPRT_CLK_33MHZ_R	26
I173	NO_TEST=YES	CLK_RAI_REFCLK_66M_R	26
I171	NO_TEST=YES	SB_USB2_CLK_33MHZ_R	26

THE FOLLOWING NETS DO NOT HAVE
TEST POINT BECAUSE OF ROUTING DENSITY
AND SIGNAL INTEGRITY.
TEST COVERAGE WILL BE BY FCT
NOTE FOR SHARING: DO NOT INCLUDE THIS LIST UNTIL
PCB LAYOUT ADDS TEST POINTS. THIS LIST IS A RESULT OF PCB
LAYOUT HAVING DIFFICULTY PLACING TEST POINTS ON THESE NETS

I175	NO_TEST=YES	100M_N<0>	82 97
I176	NO_TEST=YES	100M_P<0>	82 97
I178	NO_TEST=YES	CKA_N<0>	84 97
I179	NO_TEST=YES	CKA_P<0>	84 97
I177	NO_TEST=YES	HT_NB_N<0>	98 101
I179	NO_TEST=YES	HT_NB_P<0>	98 101
I179	NO_TEST=YES	HT_NB_REFCLK_NF<0>	98 101
I180	NO_TEST=YES	HT_NB_REFCLK_PF<0>	98 101
I181	NO_TEST=YES	HT_NB_TO_SB_CAD_N<0..7>	101
I182	NO_TEST=YES	HT_NB_TO_SB_CAD_P<0..7>	101
I183	NO_TEST=YES	HT_NB_TO_SB_CLK_P<0>	101
I184	NO_TEST=YES	HT_NB_TO_SB_CLK_N<0>	101
I185	NO_TEST=YES	HT_SB_TO_NB_CAD_N<0..7>	101
I186	NO_TEST=YES	HT_SB_TO_NB_CAD_P<0..7>	101
I187	NO_TEST=YES	HT_SB_TO_NB_CLK_P<0>	101
I188	NO_TEST=YES	HT_SB_TO_NB_CLK_N<0>	101
I189	NO_TEST=YES	PCIE_SLOTA_TO_NB_N<0..15>	82 84 97
I190	NO_TEST=YES	PCIE_SLOTA_TO_NB_P<0..15>	82 84 97
I191	NO_TEST=YES	UATA_DA<0>	127 129
I192	NO_TEST=YES	UATA_DD<1>	127 129
I193	NO_TEST=YES	UATA_DD<14>	127 129
I194	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<0>	82 84 97
I195	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<3>	82 84 97
I197	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<13>	82 97
I198	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<7>	82 97
I199	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<1>	82 84 97
I200	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<10>	82 84 97
I201	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<13>	82 97
I202	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<14>	82 97
I203	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<12>	82 97
I205	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<10>	82 97
I206	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<4>	82 97
I208	NO_TEST=YES	HT_MB_TO_NB_CTL_N<1>	98
I209	NO_TEST=YES	HT_MB_TO_NB_CTL_P<1>	98
I207	NO_TEST=YES	HT_NB_TO_MB_CTL_N<1>	98
I211	NO_TEST=YES	HT_NB_TO_MB_CTL_P<1>	98
I210	NO_TEST=YES	HT_NB_TO_SB_CTL_N<0>	101
I213	NO_TEST=YES	HT_SB_TO_NB_CTL_P<0>	101
I215	NO_TEST=YES	CLK_KOD_100M_NF<0>	82 97
I212	NO_TEST=YES	CLK_KOD_100M_PF<0>	82 97
I216	NO_TEST=YES	EI_CPU_TO_NB_CLK_N	43 56
I218	NO_TEST=YES	EI_CPU_TO_NB_CLK_P	43 56
I219	NO_TEST=YES	EI_CPU_TO_NB_SR_N<1>	43 56
I221	NO_TEST=YES	EI_CPU_TO_NB_SR_P<1>	43 56
I217	NO_TEST=YES	EI_NB_TO_CPU_CLK_N	43 56
I214	NO_TEST=YES	EI_NB_TO_CPU_CLK_P	43 56
I224	NO_TEST=YES	EI_NB_TO_CPU_SR_N<0>	43 56
I220	NO_TEST=YES	EI_NB_TO_CPU_SR_P<0>	43 56

JTAG TEST POINTS NEED TO BE ON THE BOTTOM
OF THE BOARD
ADDING FUNC_TEST=TRUE TO THESE NETS

I220	FUNC_TEST=TRUE	TP_JTAG_SB_TCK	20
I222	FUNC_TEST=TRUE	TP_JTAG_SB_TDI	20
I222	FUNC_TEST=TRUE	TP_JTAG_SB_TDO	20
I224	FUNC_TEST=TRUE	TP_JTAG_SB_TMS	20
I230	FUNC_TEST=TRUE	JTAG_SB_TRST_L	20 24
I232	FUNC_TEST=TRUE	JTAG_NB_TCK	20 30
I234	FUNC_TEST=TRUE	JTAG_NB_TDI	20 30
I233	FUNC_TEST=TRUE	JTAG_NB_TDO	20 30
I236	FUNC_TEST=TRUE	JTAG_NB_TMS	20 30
I231	FUNC_TEST=TRUE	JTAG_NB_TRST_L	
I238	FUNC_TEST=TRUE	TP_JTAG_VESTA_TDI	
I240	FUNC_TEST=TRUE	TP_JTAG_VESTA_TDO	
I239	FUNC_TEST=TRUE	TP_JTAG_VESTA_TCK	
I242	FUNC_TEST=TRUE	TP_JTAG_VESTA_TMS	
I241	FUNC_TEST=TRUE	TP_JTAG_VESTA_TRST_L	
I244	FUNC_TEST=TRUE	JTAG_CPU_TCK	30 43
I246	FUNC_TEST=TRUE	JTAG_CPU_TDI	30 43
I245	FUNC_TEST=TRUE	JTAG_CPU_TDO	30 43 47
I248	FUNC_TEST=TRUE	JTAG_CPU_TMS	30 43
I247	FUNC_TEST=TRUE	JTAG_CPU_TRST_L	43 47

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FUNC TEST 2 OF 2

SYNC_MASTER=FINO-ME SYNC_DATE=05/18/2005

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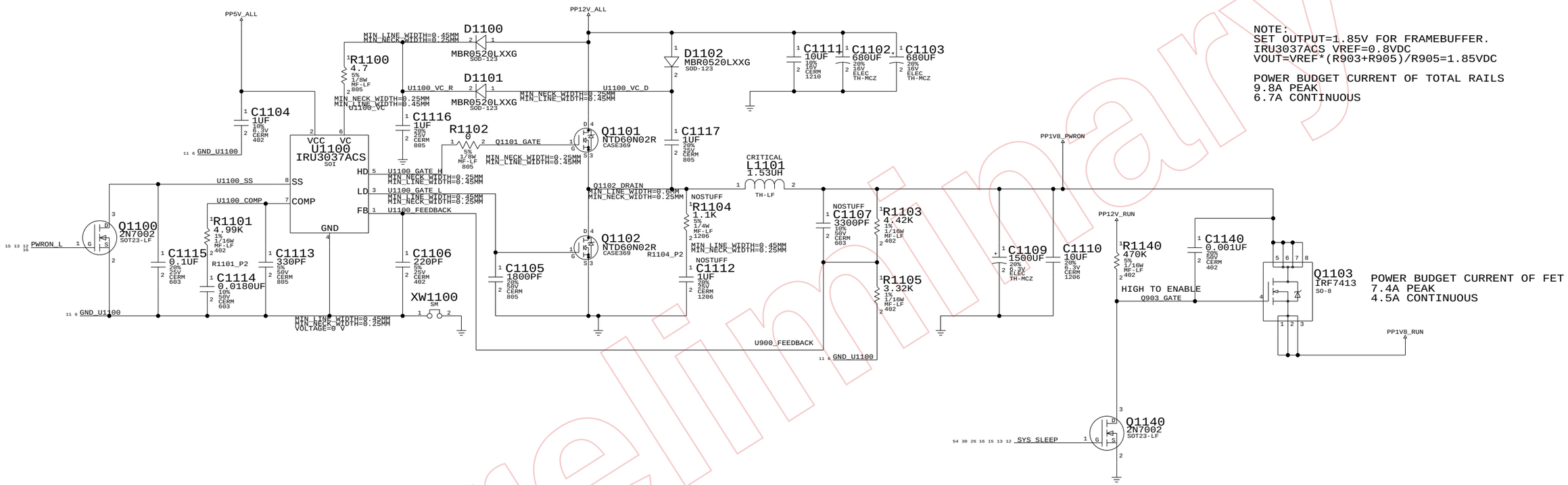
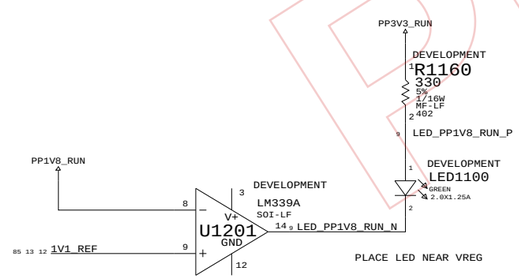
1.8V VOLTAGE REGULATOR



NOTE:
SET OUTPUT=1.85V FOR FRAMEBUFFER.
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R903+R905)/R905=1.85VDC

POWER BUDGET CURRENT OF TOTAL RAILS
9.8A PEAK
6.7A CONTINUOUS

POWER BUDGET CURRENT OF FET
7.4A PEAK
4.5A CONTINUOUS



PLACE LED NEAR VREG

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1.8V Vreg	
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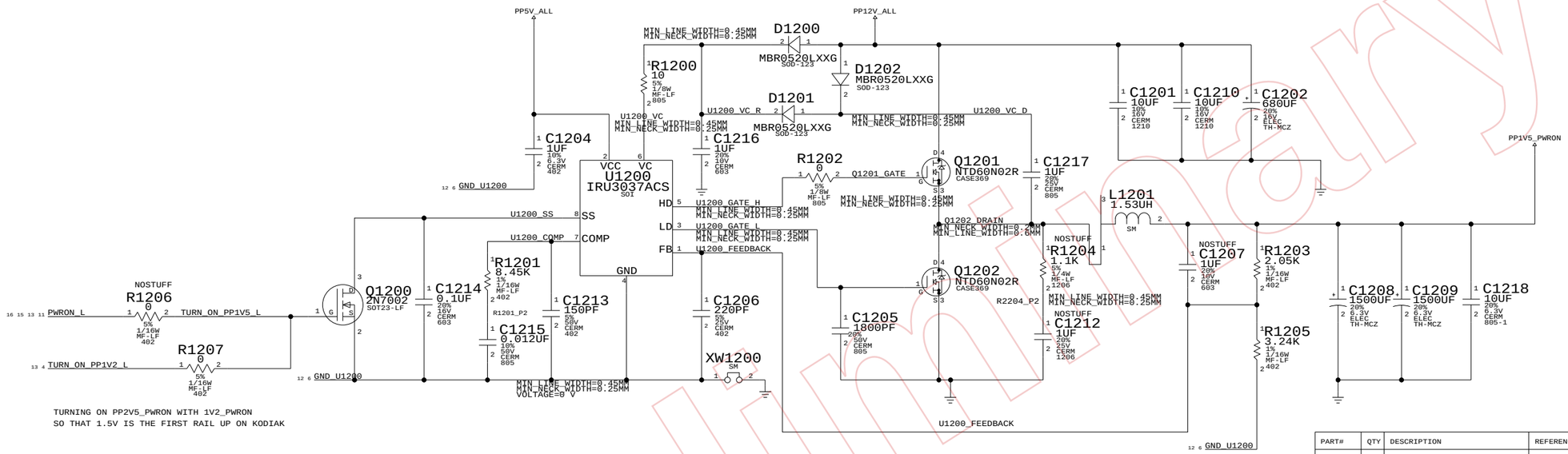
KODIAK CORE VOLTAGE REGULATOR

NOTE:

IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1203+R1205)/R1205=1.30VDC

LOAD FROM POWER BUDGET
8.5A PEAK CURRENT DRAW
7.2A CONTINUOUS CURRENT DRAW

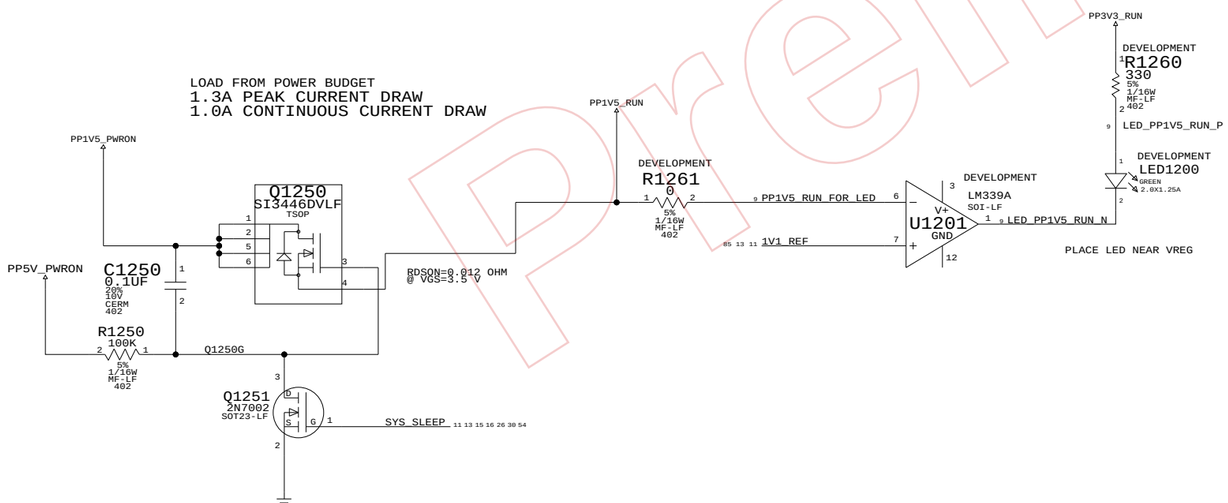
1.35V	R1205=2.87K
1.30V	R1205=3.24K
1.25V	R1205=4.02K



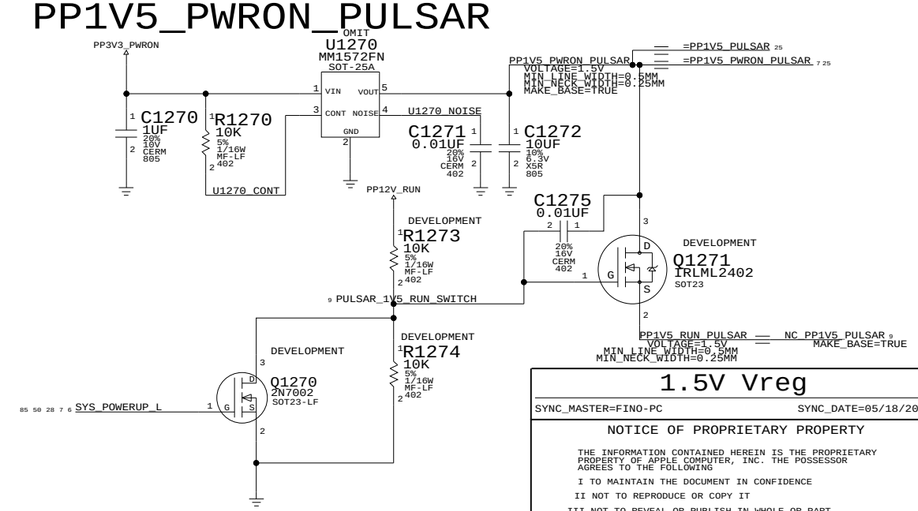
TURNING ON PP2V5_PWRON WITH 1V2_PWRON
SO THAT 1.5V IS THE FIRST RAIL UP ON KODIAK

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1145	1	MM1571FN	U1270	CRITICAL	

LOAD FROM POWER BUDGET
1.3A PEAK CURRENT DRAW
1.0A CONTINUOUS CURRENT DRAW



PP1V5_PWRON_PULSAR



1.5V Vreg

SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

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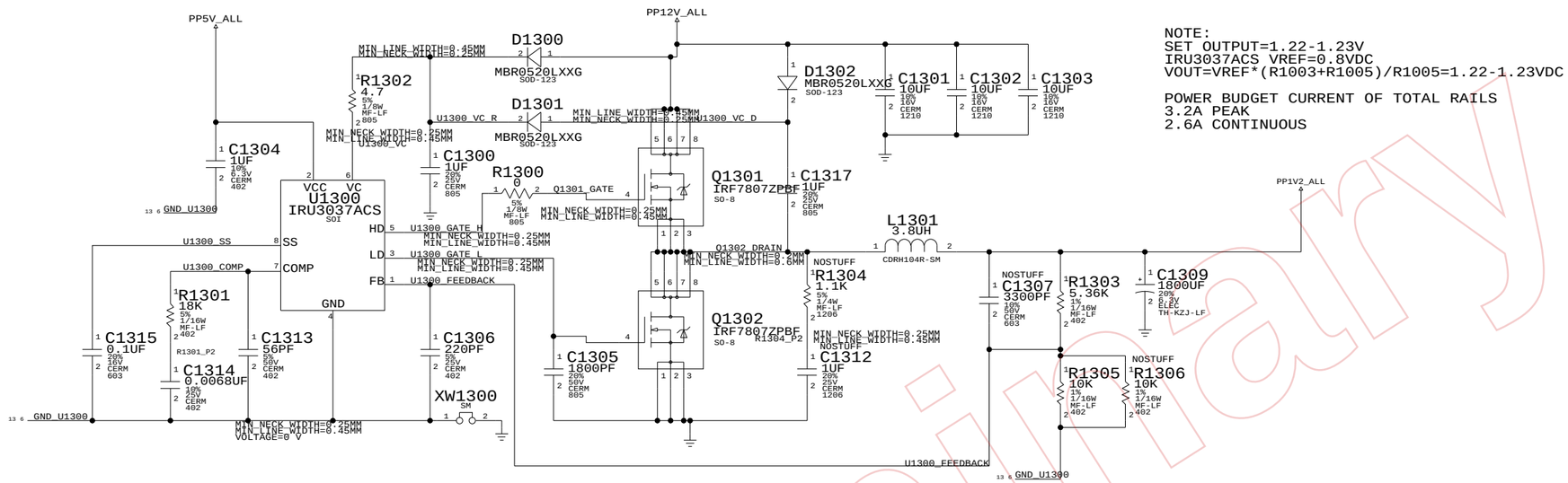
PP1V2_ALL VOLTAGE REGULATOR

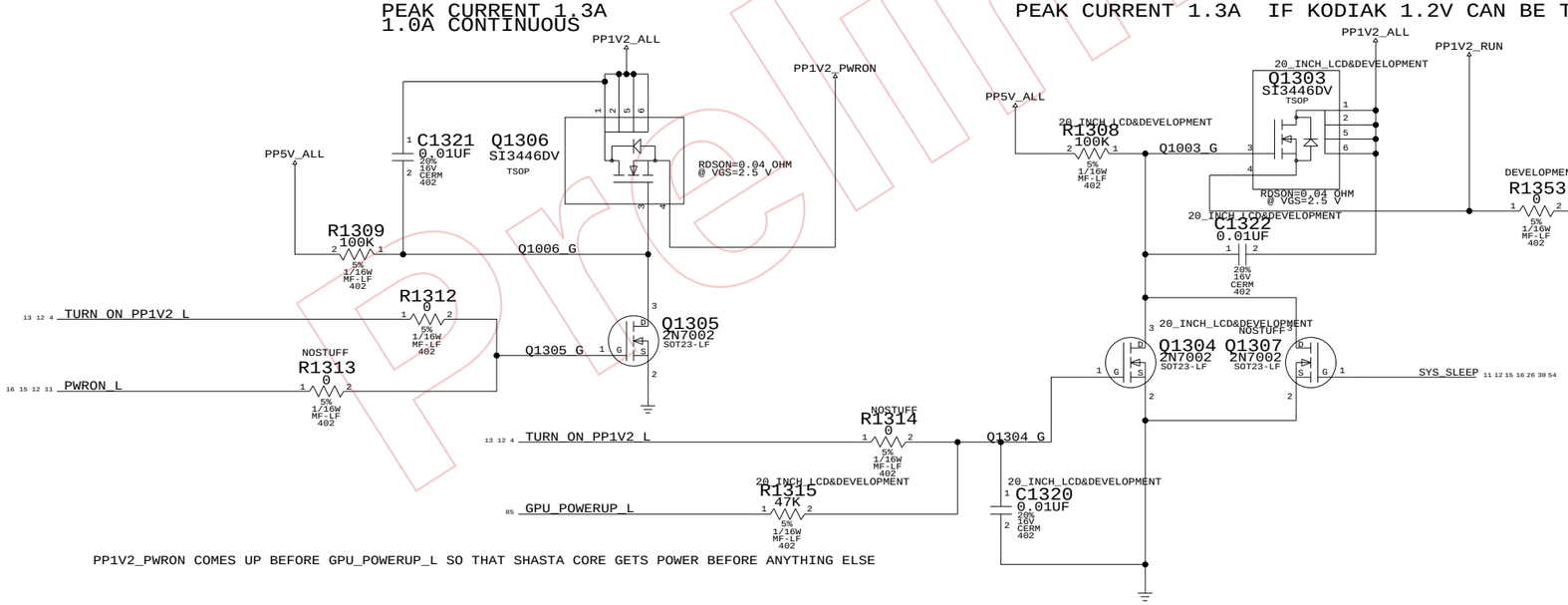


NOTE:
SET OUTPUT=1.22-1.23V
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1003+R1005)/R1005=1.22-1.23VDC

POWER BUDGET CURRENT OF TOTAL RAILS
3.2A PEAK
2.6A CONTINUOUS

PP1V2_PWRON FET SWITCH

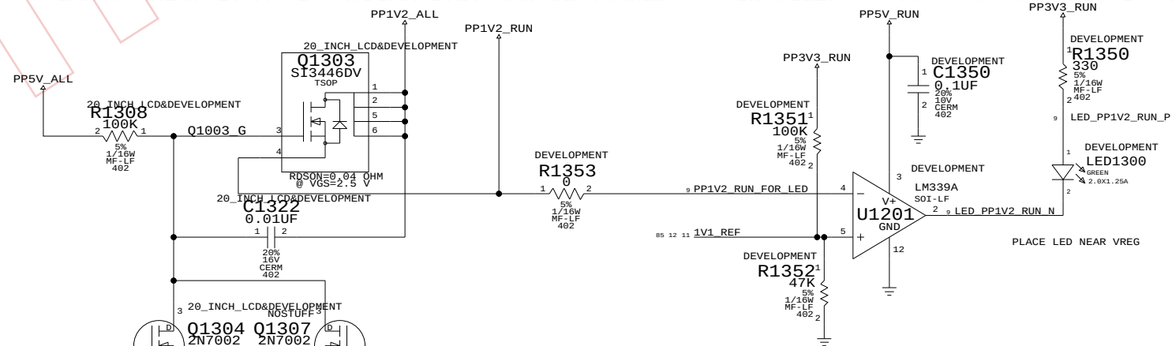
PEAK CURRENT 1.3A
1.0A CONTINUOUS



PP1V2_PWRON COMES UP BEFORE GPU_POWERUP_L SO THAT SHASTA CORE GETS POWER BEFORE ANYTHING ELSE

PP1V2_RUN FET SWITCH

PEAK CURRENT 1.3A IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.0A/M23 IF NOT



1.2V Vreg	
SYNC_MASTER=FINO-PC	SYNC_DATE=05/18/2005

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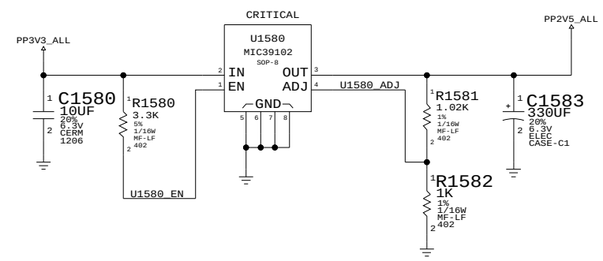
PP2V5_ALL VOLTAGE REGULATOR

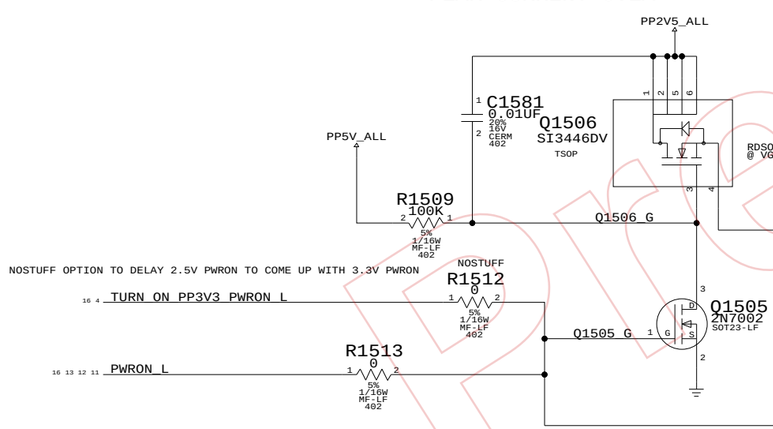


NOTE:
SET OUTPUT=2.5V
IRU3037CS VREF=1.24VDC
VOUT=VREF*(R1581+R1582)+1=5.505VDC

POWER BUDGET CURRENT OF TOTAL RAILS
0.2A PEAK
0.1A CONTINUOUS

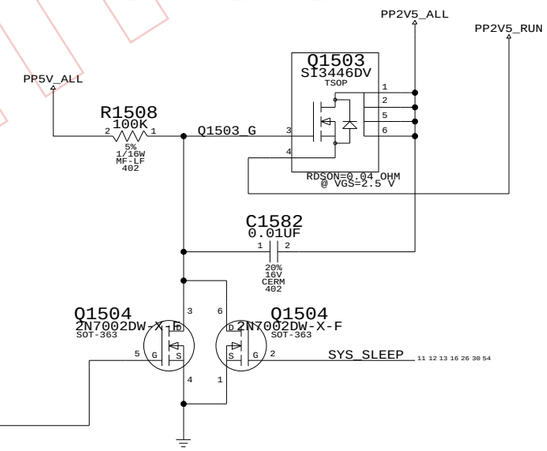
PP2V5_PWRON FET SWITCH

PEAK CURRENT 0.1A



PP2V5_RUN FET SWITCH

PEAK CURRENT 0.1A



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2.5V Vreg

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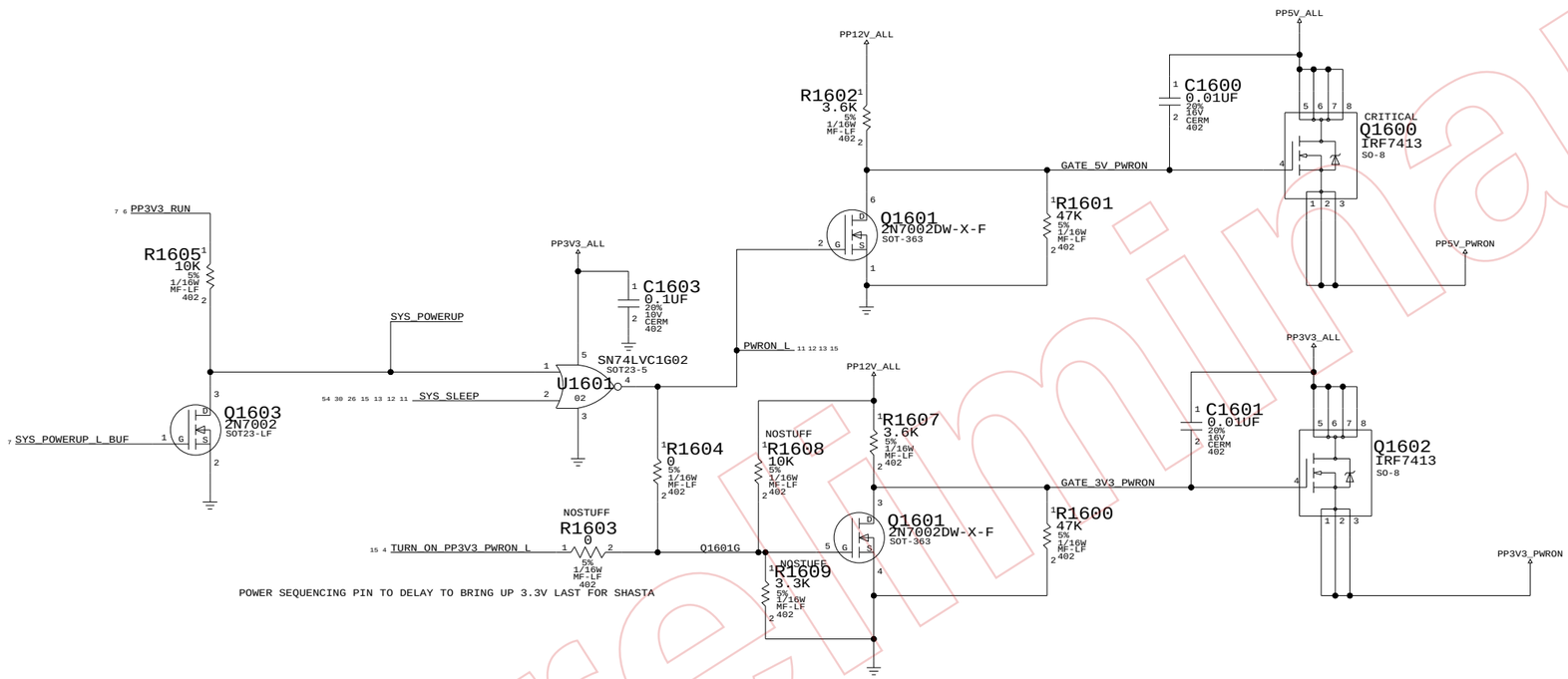

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5V & 3.3V Fets

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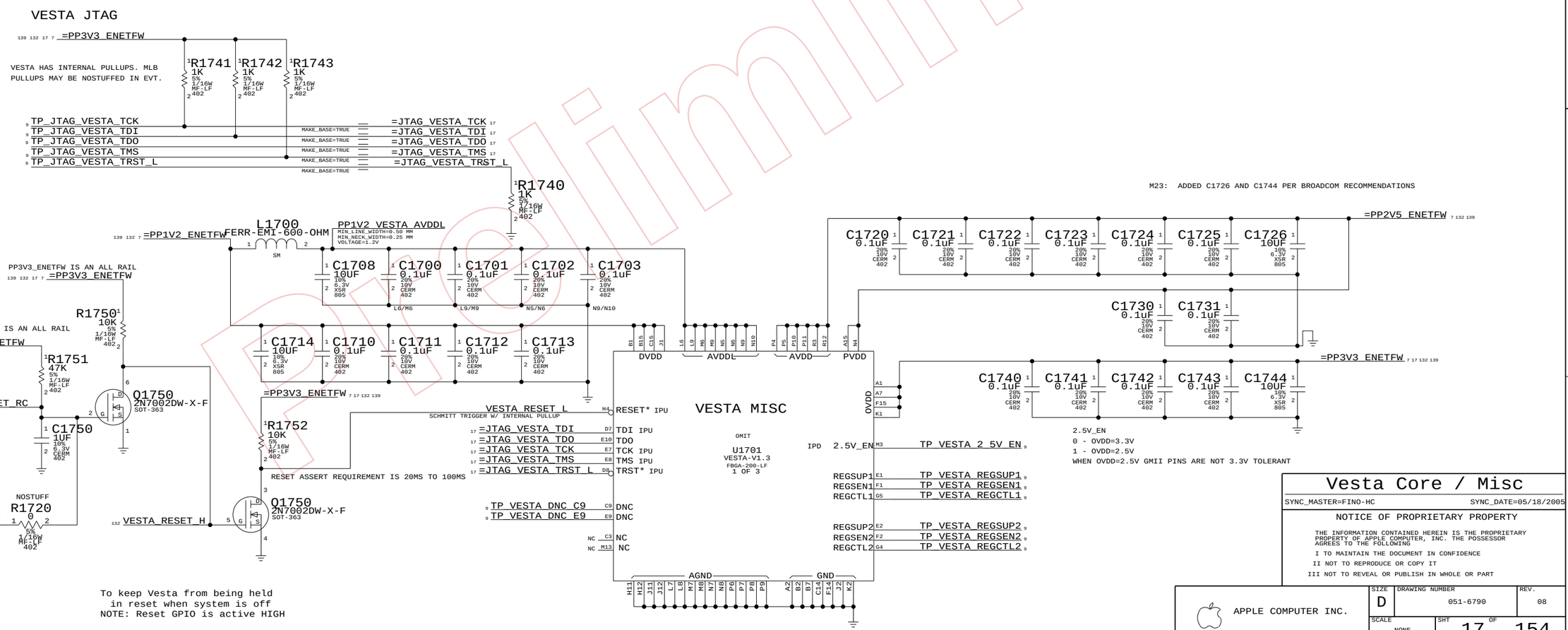
Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.



Vesta Core / Misc

SYNC_MASTER=FINO-HC SYNC_DATE=05/18/2005

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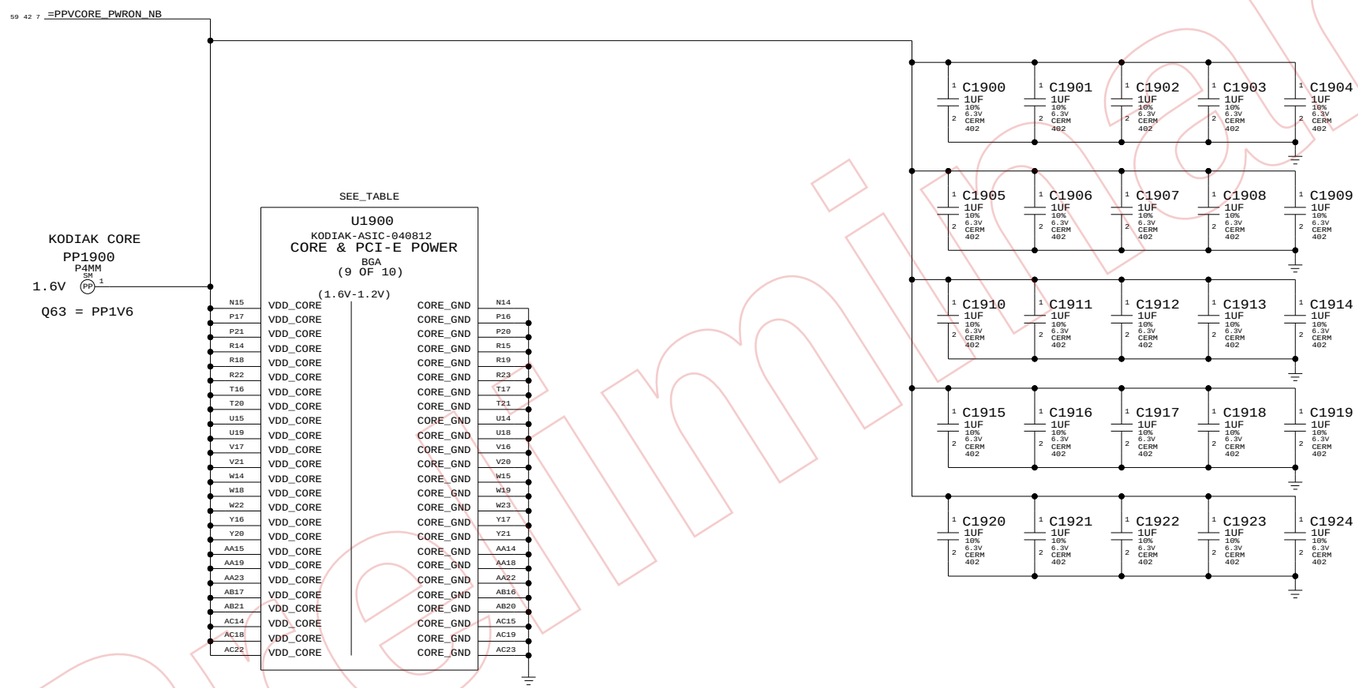

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KODIAK CORE & BYPASS

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

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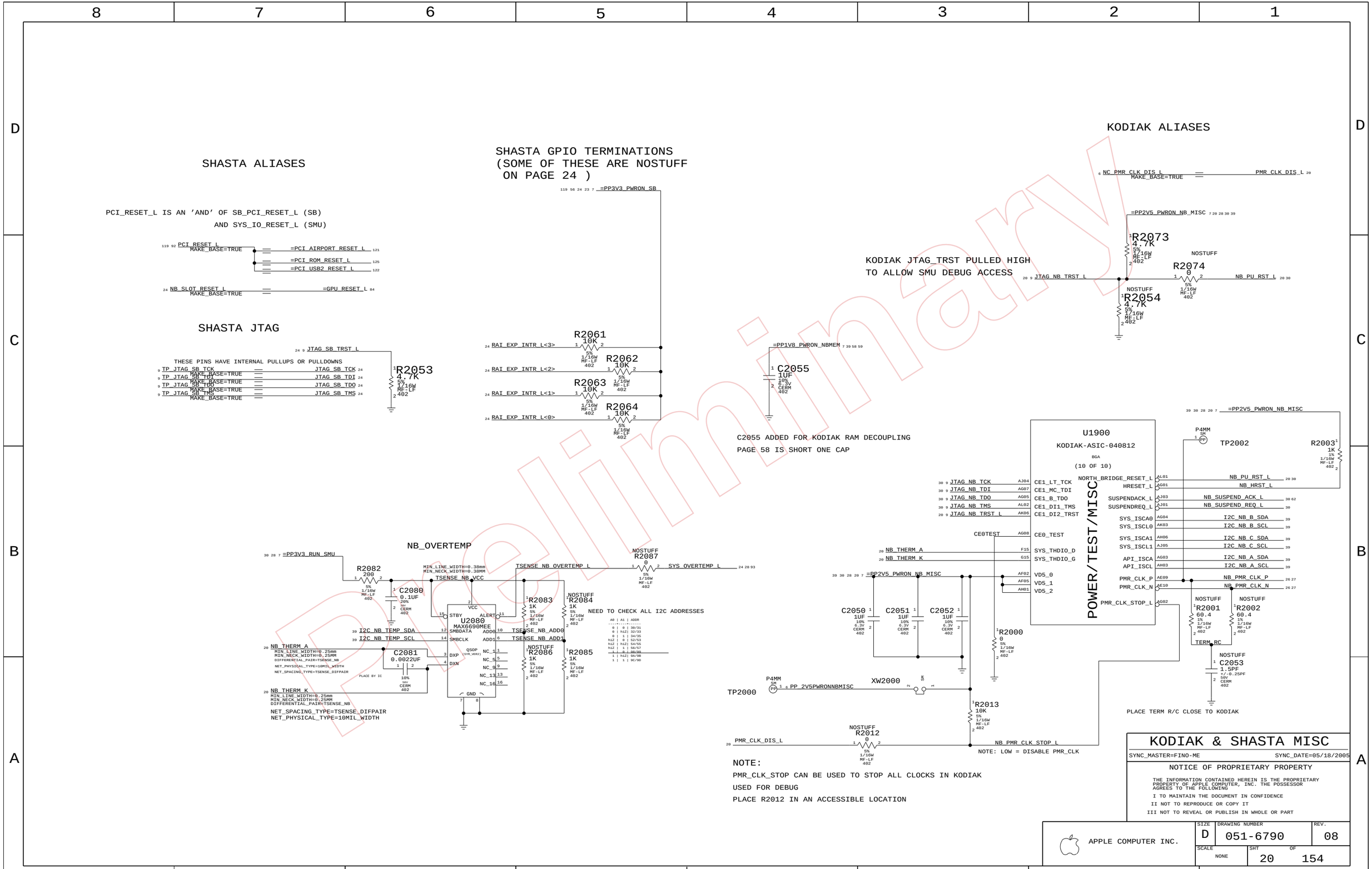


Preliminary

Page Notes

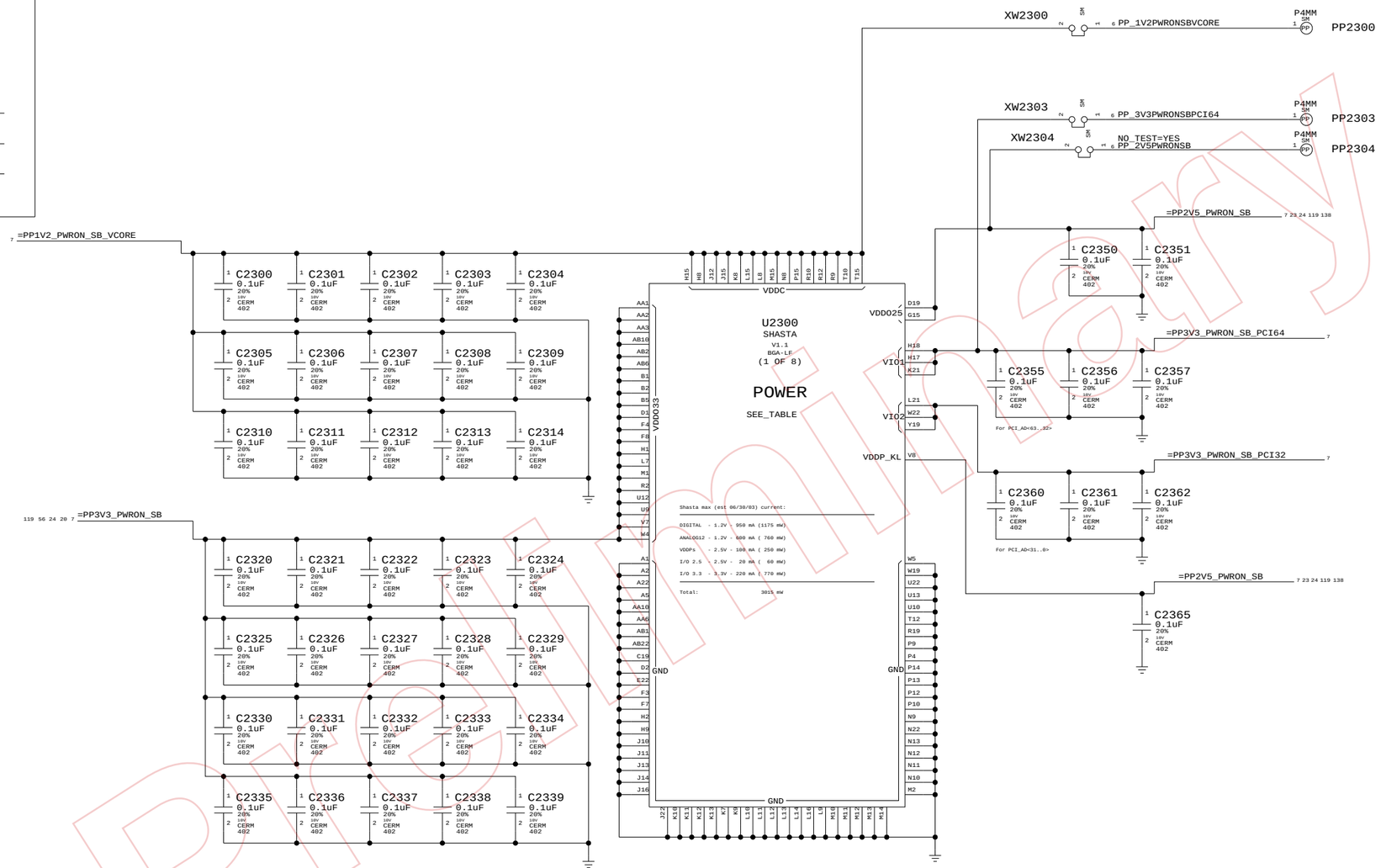
Power aliases required by this page:
- =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB_PCI32 (VIO2) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB
- =PP1V2_PWRON_SB_VCORE

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. CONNECT VIO2 TO appropriate PCI bus voltage and VIO1 TO SAME IF 64-BIT PCI, otherwise 3.3V.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Power Sequencing:
Must power Shasta VCore rail before any other Shasta supplies.



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Shasta Core Power

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

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LAST_MODIFIED=Thu May 19 14:08:56 2005

DRAWING
TITLE=Z13MHBA
NAME=SDRAWING

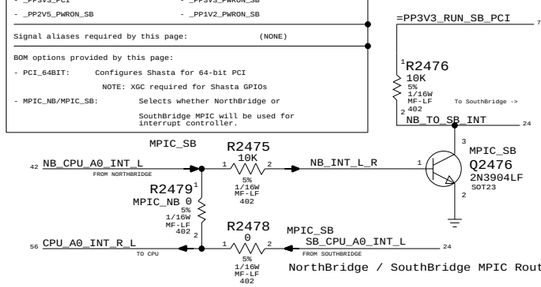
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
I2S0_TO_SB		I2S0_DEV_TO_SB_DTI
I2S0_TO_DEV		I2S0_SB_TO_DEV_DTO
I2S0_TO_DEV	AUDIO	I2S0_MCLK
I2S0_BIDIR		I2S0_BITCLK
I2S0_BIDIR		I2S0_SYNC
I2S1_TO_SB		I2S1_DEV_TO_SB_DTI
I2S1_TO_DEV		I2S1_SB_TO_DEV_DTO
I2S1_TO_DEV	0.25mm SPACING	I2S1_MCLK
I2S1_BIDIR		I2S1_BITCLK
I2S1_BIDIR		I2S1_SYNC
I2S2_TO_SB		I2S2_DEV_TO_SB_DTI
I2S2_TO_DEV		I2S2_SB_TO_DEV_DTO
I2S2_TO_DEV	0.25mm SPACING	I2S2_MCLK
I2S2_BIDIR		I2S2_BITCLK
I2S2_BIDIR		I2S2_SYNC
SB_CLK18M_XTAL	0.38mm SPACING	SB_CLK18M_XTALI
	0.38mm SPACING	SB_CLK18M_XTALO
	0.38mm SPACING	SB_CLK18M_XTALO_R
SB_CLK25M_ATA	0.38mm SPACING	SB_CLK25M_SATA
	P3MM SPACING	NB_TO_SB_INT
	P3MM SPACING	SB_CPU_A0_INT_L
	P3MM SPACING	SB_CPU_A1_INT_L
	P3MM SPACING	SB_CPU_B0_INT_L
	P3MM SPACING	SB_CPU_B1_INT_L
	P3MM SPACING	PCI_AIRPORT_INT_L
	P3MM SPACING	PCI_USB2_INT_L
	P3MM SPACING	I2S0_RESET_L
	P3MM SPACING	I2S1_RESET_L
	P3MM SPACING	I2S2_RESET_L
	P3MM SPACING	MB_SLOT_RESET_L
	P3MM SPACING	NB_SLOT_RESET_L
	P3MM SPACING	SB_CPU_A0_SRESET_L
	P3MM SPACING	SB_CPU_A1_SRESET_L
	P3MM SPACING	SB_CPU_B0_SRESET_L
	P3MM SPACING	SB_CPU_B1_SRESET_L

Page Notes

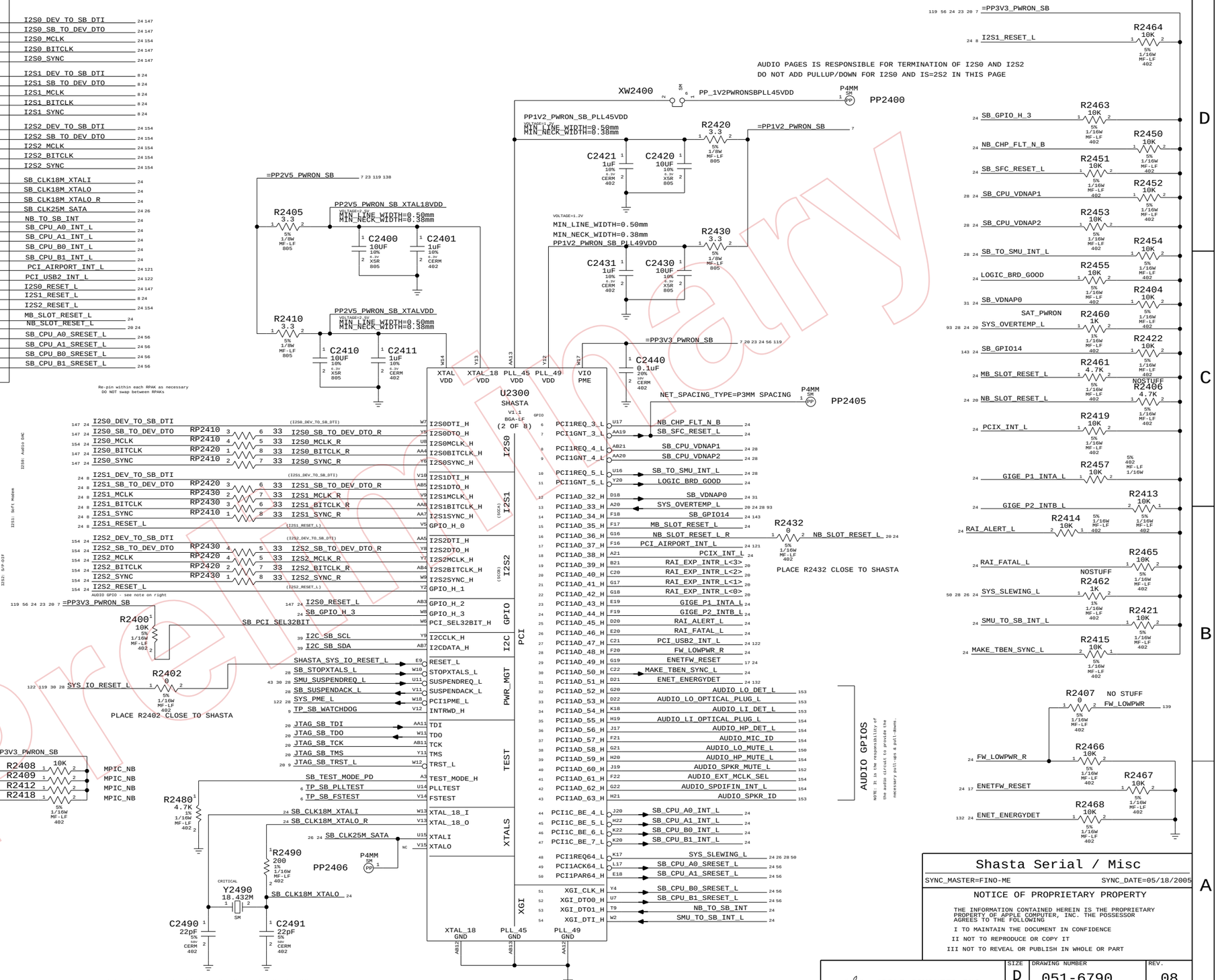
Power aliases required by this page:
- _P3V3/_PCI
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PP1V2_PWRON_SB

Signal aliases required by this page: (NONE)

BOM options provided by this page:
- PCI_64BIT: Configures Shasta for 64-bit PCI
  NOTE: XGC required for Shasta GPIOs
- MPIC_NB/MPIC_SB: Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.



NorthBridge / SouthBridge MPIC Routing



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DRAWING

TITLE=K21LOWMA
ABBREV=YOMAMAG

Shasta Serial / Misc

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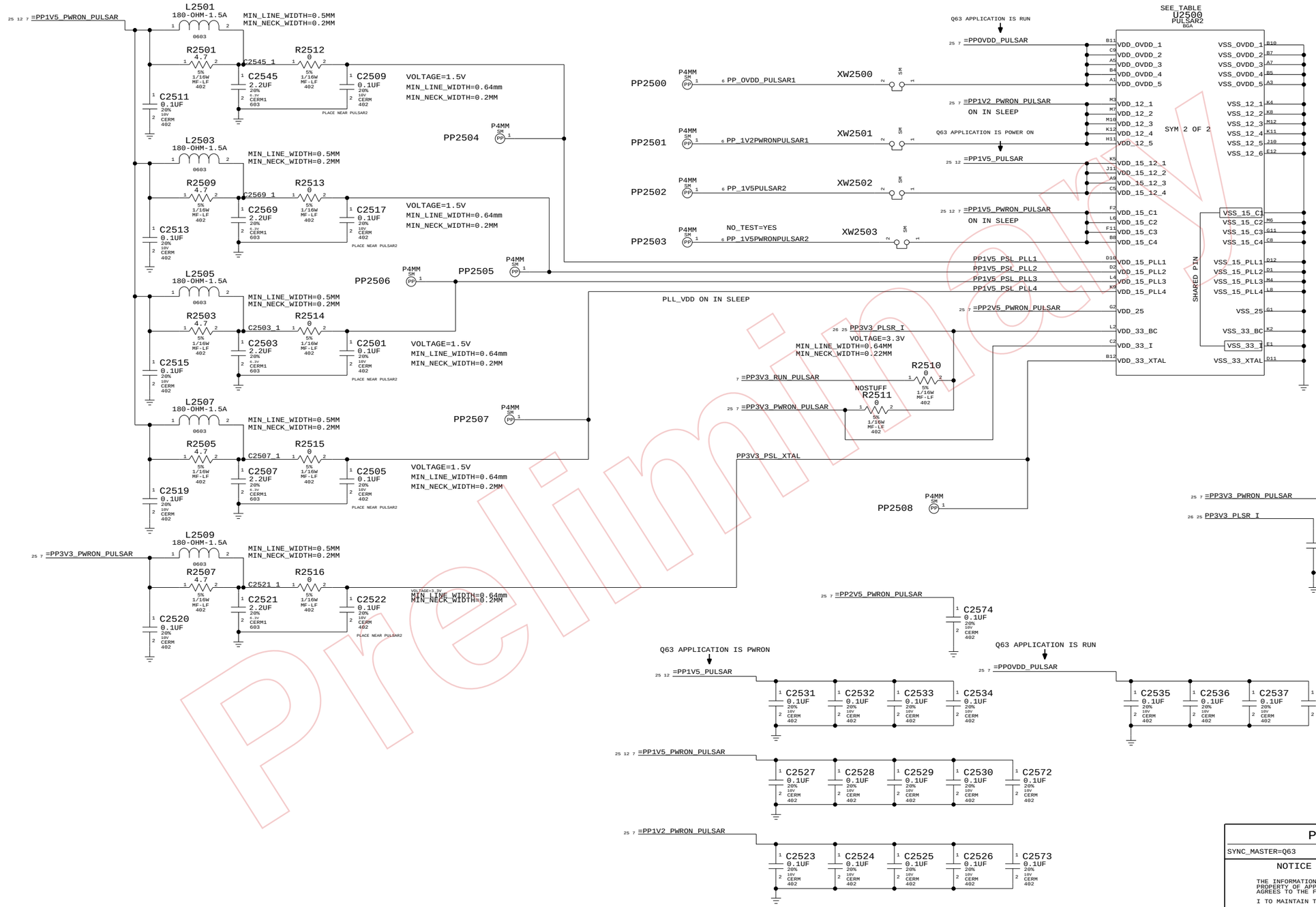

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PULSAR2 POWER

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

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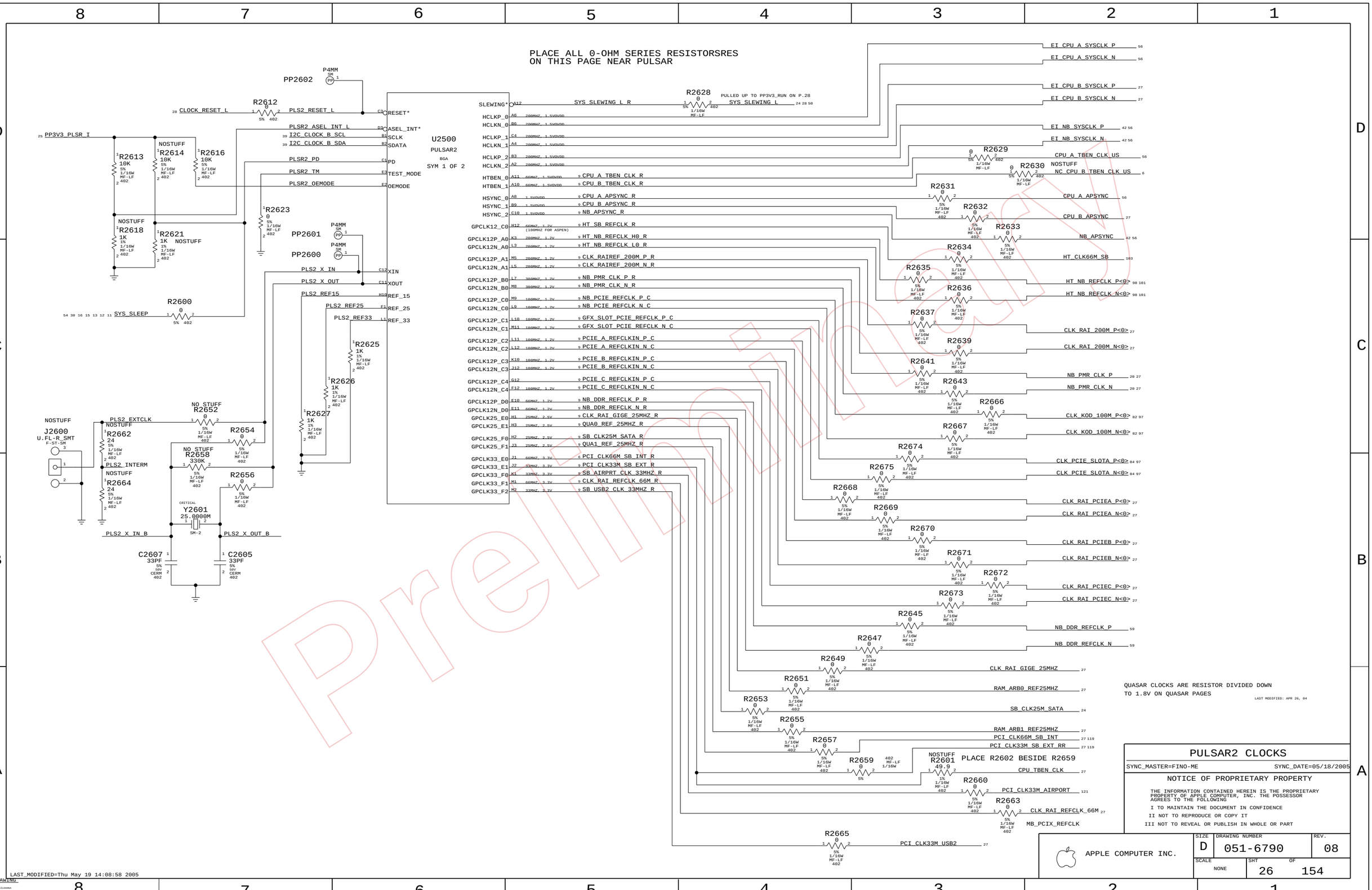
DRAWING


PLACE ALL 0-OHM SERIES RESISTORSRES
ON THIS PAGE NEAR PULSAR
U2500
PULSAR2
BGA
SYM 1 OF 2
PP2602
PP2601
PP2600
R2612
R2628
PULLED UP TO PP3V3_RUN ON P.28
SYS_SLEWING_L
R2600
SYS_SLEEP
J2600
U.FL-R_SMT
F-ST-SM
Y2601
25.0000M
C2607
33PF
C2605
33PF
R2601
49.9
PLACE R2602 BESIDE R2659
QUASAR CLOCKS ARE RESISTOR DIVIDED DOWN
TO 1.8V ON QUASAR PAGES
LAST MODIFIED: APR 26, 04
PULSAR2 CLOCKS
SYNC_MASTER=FINO-ME
SYNC_DATE=05/18/2005
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REV. 08
SCALE NONE
SHT 26 OF 154
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N/C ALIASES

N/C RAINIER CLOCKS

6 NC_CLK_RAI_REFCLK_66M — CLK_RAI_REFCLK_66M 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_GIGE_25MHZ — CLK_RAI_GIGE_25MHZ 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_200M_P<0> — CLK_RAI_200M_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_200M_N<0> — CLK_RAI_200M_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEA_P<0> — CLK_RAI_PCIEA_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEA_N<0> — CLK_RAI_PCIEA_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEB_P<0> — CLK_RAI_PCIEB_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEB_N<0> — CLK_RAI_PCIEB_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEC_P<0> — CLK_RAI_PCIEC_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEC_N<0> — CLK_RAI_PCIEC_N<0> 26
MAKE_BASE=TRUE

N/C CPUB CLOCKS

9 NC_CPU_TBEN_CLK — CPU_TBEN_CLK 26
MAKE_BASE=TRUE

CPU_TBEN_CLK IS FOR Q63 ONLY
IT IS THE INPUT TO THE AND GATE WHICH
GENERATES CPUA AND CPUB TBEN_CLK

6 NC_EI_CPU_B_SYSCLK_P — EI_CPU_B_SYSCLK_P 26
MAKE_BASE=TRUE

6 NC_EI_CPU_B_SYSCLK_N — EI_CPU_B_SYSCLK_N 26
MAKE_BASE=TRUE

6 NC_CPU_B_APSYNC — CPU_B_APSYNC 26
MAKE_BASE=TRUE

N/C QUASAR CLOCKS

6 NC_RAM_ARB0_REF25MHZ — RAM_ARB0_REF25MHZ 26
MAKE_BASE=TRUE

6 NC_RAM_ARB1_REF25MHZ — RAM_ARB1_REF25MHZ 26
MAKE_BASE=TRUE

CLOCK CONSTRAINTS

	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	ELECTRICAL_CONSTAINT_SET	
26 20 NB_PMR_CLK_P	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	167
26 20 NB_PMR_CLK_N	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	168
119 26 PCI_CLK66M_SB_INT		PCI_CLK_SB	P3MM SPACING	PCI_CLK_SB	169
26 PCI_CLK33M_SB_EXT_RR		PCI_CLK_SB	PCI_CLK_SB	PCI_CLK_SB	170

NOTE:
ALL OTHER CLOCK CONTRAINTS ON THEIR
RESPECTIVE BUS PAGES

26 PCI_CLK33M_USB2 — =PCI_CLK33M_USB2 122
MAKE_BASE=TRUE

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Pulsar Aliases

SYNC_MASTER=FINO-ME SYNC_DATE=05/18/2005

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SMU_CLK10M_XTAL	0.38MM SPACING		SMU_CLK10M_XIN 28
	0.38MM SPACING		SMU_CLK10M_XOUT 28
	0.38MM SPACING		SMU_CLK10M_XOUT_R 28
RTC_CLK32K_XTAL	0.38MM SPACING		RTC_CLK32K_X1 28
	0.38MM SPACING		RTC_CLK32K_X2 28
PAT3	P3MM SPACING		SMU_IO_RESET_L 28 30
PAT4	0.25MM SPACING		SYS_NORTH_RESET_L 28 30

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
PAT56 SMU_RESET	0.25MM SPACING		SYS_NORTH_RESET_L 28 30
PAT57 SMU_RESET	0.25MM SPACING		SYS_IO_RESET_L 24 30 119 122
PAT72	P3MM SPACING		CLOCK_RESET_L 26 28
PAT75	P3MM SPACING		SYS_RESET_BUTTON_L 28 29

Page Notes

Power aliases required by this page:
- =PP3V3_ALL_SMU
- =PP3V3_ALL_RTC
- =PP3V3_PWRON_SMU
- =PPVREF_SMU (SMU AVCC OR 2.5V REFERENCE)

Signal aliases required by this page:
(NONE)

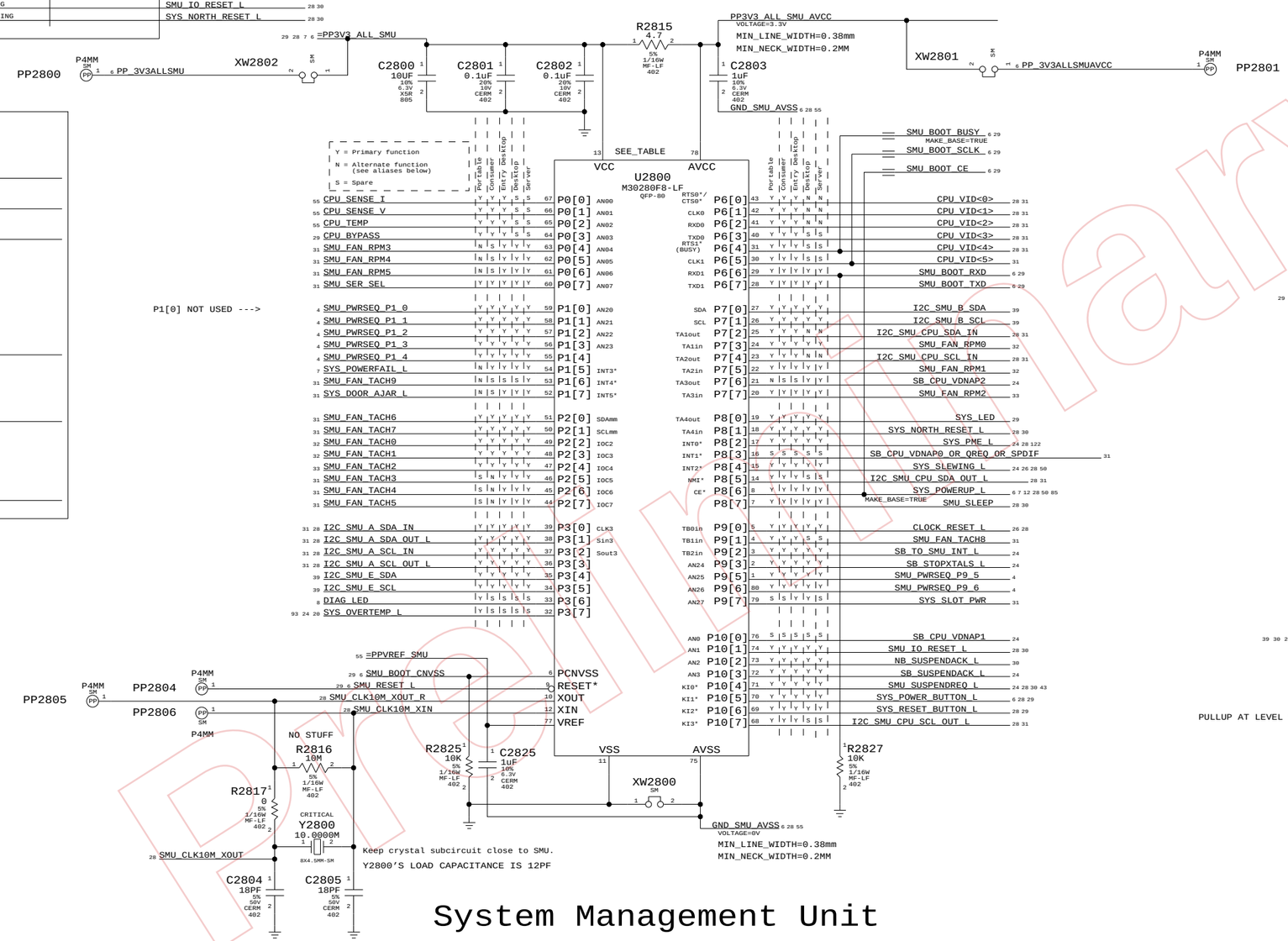
BOM options provided by this page:
(NONE)

NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

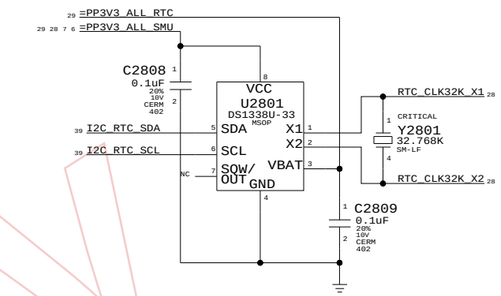
NOTE: Some primary and alternate functions reuire pull-ups that are not. provided on this page. Please. review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

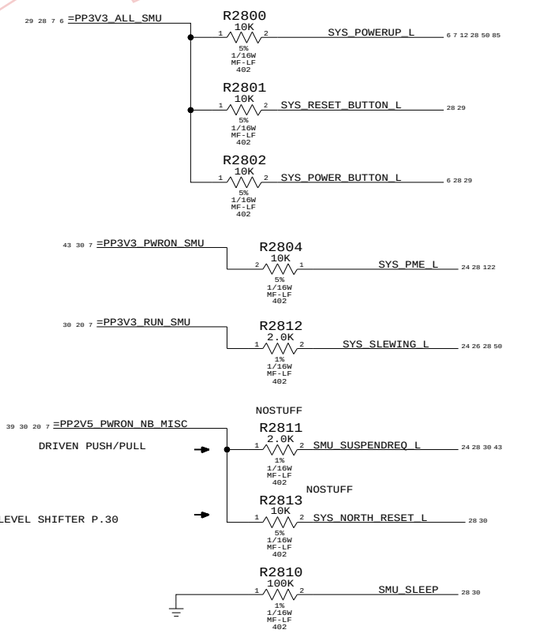


System Management Unit

Real Time Clock



SMU Pull-ups / pull-down



Alternate Functions

Tower & Server

	Port		
CPU_VID<0>	6.0		SAT_MRESET_L
CPU_VID<1>	6.1		CPU_A_INSERTED_L
CPU_VID<2>	6.2		CPU_B_INSERTED_L
I2C_SMU_CPU_SDA_IN	7.2		SMU_FAN_PWM8
I2C_SMU_CPU_SCL_IN	7.4		SMU_FAN_PWM9
I2C_SMU_A_SDA_IN	3.0		I2C_SMU_A_SDA
I2C_SMU_A_SDA_OUT_L	3.1		I2C_SMU_A_SCL

	Port		
CPU_VID<3>	6.3		SMU_FAN_RPM6
CPU_VID<4>	6.4		SMU_FAN_RPM7
I2C_SMU_A_SCL_IN	3.2		NB_TDI
I2C_SMU_A_SCL_OUT_L	3.3		NB_TCK
I2C_SMU_CPU_SDA_OUT_L	8.5		NB_TMS
I2C_SMU_CPU_SCL_OUT_L	10.7		NB_TDO_SMU

System Management Unit

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

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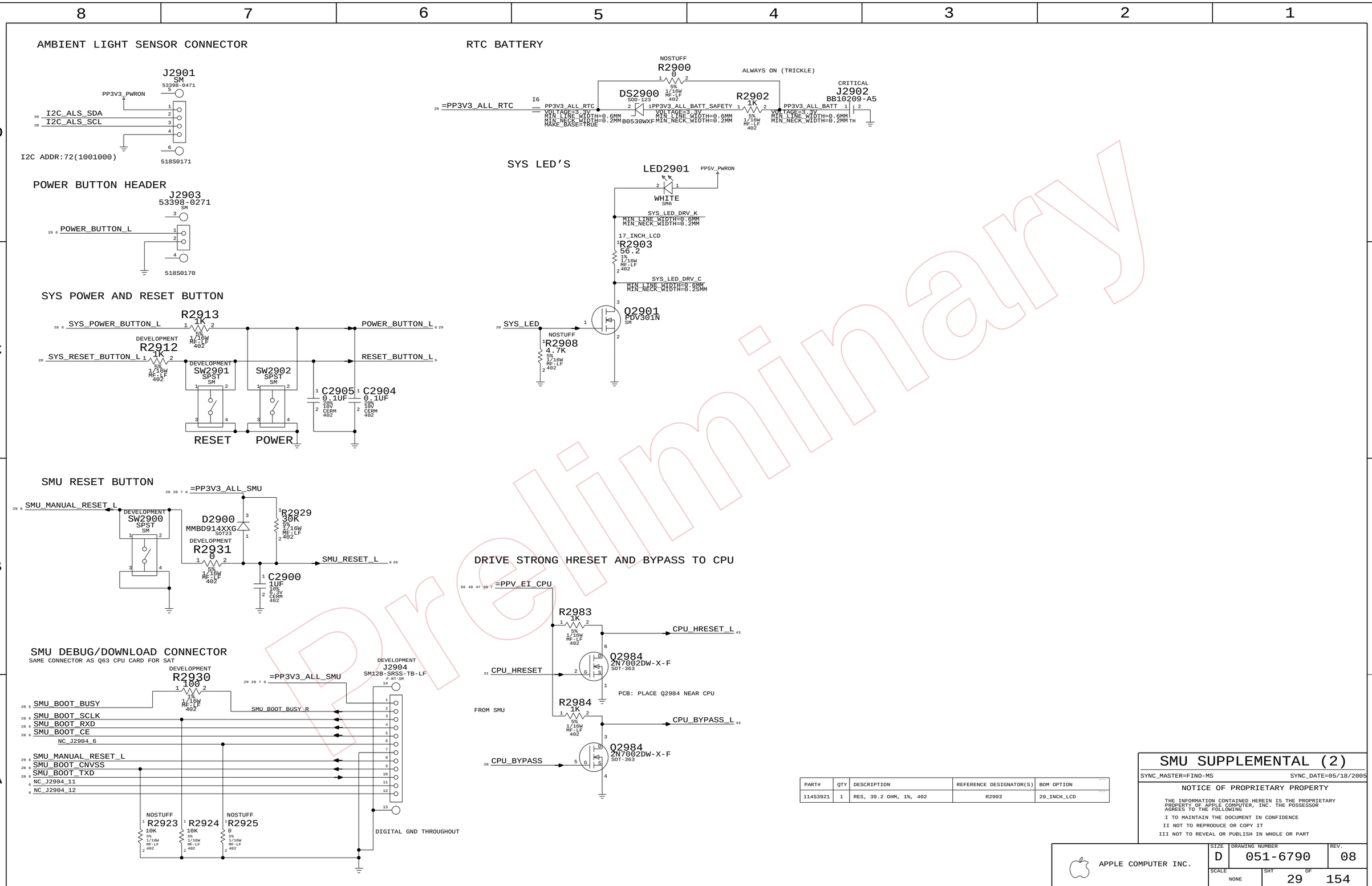

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S3921	1	RES, 39.2 OHM, 1%, 402	R2903	20_INCH_LCD

SMU SUPPLEMENTAL (2)

SYNC_MASTER=FINO-MS SYNC_DATE=05/18/2005

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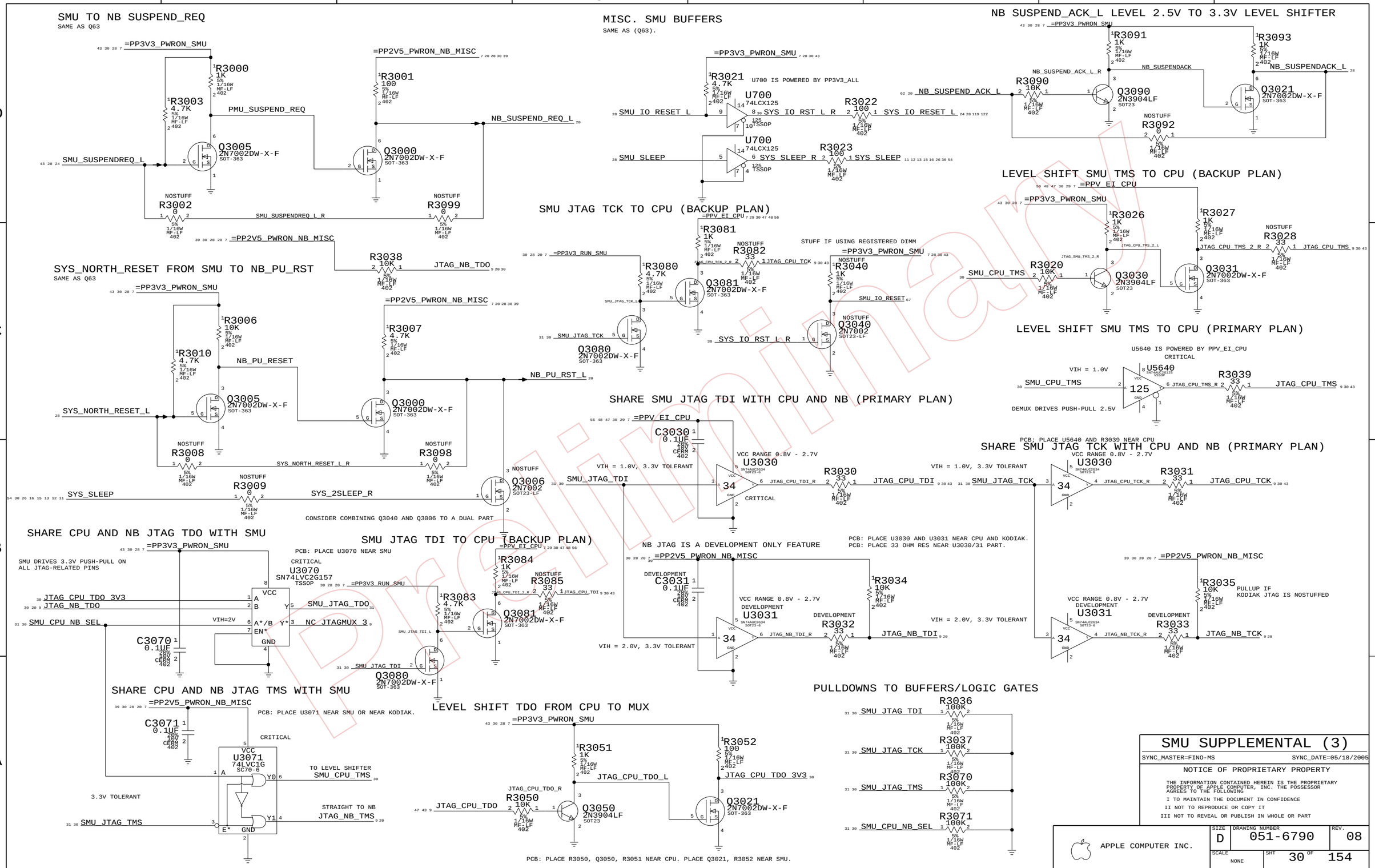
SMU TO NB SUSPEND_REQ
SAME AS Q63
=PP3V3_PWRON_SMU
R3000 1K
R3003 4.7K
PMU_SUSPEND_REQ
=PP2V5_PWRON_NB_MISC
R3001 100
NB_SUSPEND_REQ_L
Q3005 2N7002DW-X-F SOT-363
Q3000 2N7002DW-X-F SOT-363
SMU_SUSPENDREQ_L
NOSTUFF R3002 0
NOSTUFF R3099 0
SMU_SUSPENDREQ_L_R
=PP2V5_PWRON_NB_MISC
R3038 10K
JTAG_NB_TDO
SYS_NORTH_RESET FROM SMU TO NB_PU_RST
SAME AS Q63
=PP3V3_PWRON_SMU
R3006 10K
R3010 4.7K
NB_PU_RESET
=PP2V5_PWRON_NB_MISC
R3007 4.7K
NB_PU_RST_L
Q3005 2N7002DW-X-F SOT-363
Q3000 2N7002DW-X-F SOT-363
SYS_NORTH_RESET_L
NOSTUFF R3008 0
NOSTUFF R3098 0
SYS_NORTH_RESET_L_R
NOSTUFF R3009 0
SYS_SLEEP
SYS_2SLEEP_R
NOSTUFF Q3006 2N7002 SOT23-LF
CONSIDER COMBINING Q3040 AND Q3006 TO A DUAL PART
MISC. SMU BUFFERS
SAME AS (Q63).
=PP3V3_PWRON_SMU
R3021 4.7K
U700 IS POWERED BY PP3V3_ALL
U700 74LCX125 TSSOP
SMU_IO_RESET_L
SYS_IO_RST_L_R
R3022 100
SYS_IO_RESET_L
U700 74LCX125 TSSOP
SMU_SLEEP
SYS_SLEEP_R
R3023 100
SYS_SLEEP
SMU JTAG TCK TO CPU (BACKUP PLAN)
=PPV_EI_CPU
R3081 1K
R3080 4.7K
NOSTUFF R3082 33
JTAG_CPU_TCK
Q3081 2N7002DW-X-F SOT-363
Q3080 2N7002DW-X-F SOT-363
SMU_JTAG_TCK
STUFF IF USING REGISTERED DIMM
=PP3V3_PWRON_SMU
NOSTUFF R3040 1K
SMU_IO_RESET
NOSTUFF Q3040 2N7002 SOT23-LF
SYS_IO_RST_L_R
SHARE SMU JTAG TDI WITH CPU AND NB (PRIMARY PLAN)
=PPV_EI_CPU
C3030 0.1UF
VCC RANGE 0.8V - 2.7V
U3030 SN74AUC2G34 SOT23-6
VIH = 1.0V, 3.3V TOLERANT
SMU_JTAG_TDI
R3030 33
JTAG_CPU_TDI
CRITICAL
CONSIDER COMBINING Q3040 AND Q3006 TO A DUAL PART
NB SUSPEND_ACK_L LEVEL 2.5V TO 3.3V LEVEL SHIFTER
=PP3V3_PWRON_SMU
R3091 1K
R3093 1K
NB_SUSPENDACK
NB_SUSPENDACK_L
NB_SUSPEND_ACK_L_R
R3090 10K
NB_SUSPEND_ACK_L
Q3090 2N3904LF SOT23
Q3021 2N7002DW-X-F SOT-363
NOSTUFF R3092 0
LEVEL SHIFT SMU TMS TO CPU (BACKUP PLAN)
=PPV_EI_CPU
=PP3V3_PWRON_SMU
R3026 1K
R3027 1K
NOSTUFF R3028 33
JTAG_CPU_TMS
SMU_CPU_TMS
R3020 10K
Q3030 2N3904LF SOT23
Q3031 2N7002DW-X-F SOT-363
LEVEL SHIFT SMU TMS TO CPU (PRIMARY PLAN)
U5640 IS POWERED BY PPV_EI_CPU
CRITICAL
VIH = 1.0V
U5640 SN74AUC2G125 VSSOP
SMU_CPU_TMS
R3039 33
JTAG_CPU_TMS
DEMUX DRIVES PUSH-PULL 2.5V
PCB: PLACE U5640 AND R3039 NEAR CPU
SHARE SMU JTAG TCK WITH CPU AND NB (PRIMARY PLAN)
VCC RANGE 0.8V - 2.7V
U3030 SN74AUC2G34 SOT23-6
VIH = 1.0V, 3.3V TOLERANT
SMU_JTAG_TCK
R3031 33
JTAG_CPU_TCK
PCB: PLACE U3030 AND U3031 NEAR CPU AND KODIAK.
PCB: PLACE 33 OHM RES NEAR U3030/31 PART.
SHARE CPU AND NB JTAG TDO WITH SMU
=PP3V3_PWRON_SMU
SMU DRIVES 3.3V PUSH-PULL ON ALL JTAG-RELATED PINS
PCB: PLACE U3070 NEAR SMU
CRITICAL
U3070 SN74LVC2G157 TSSOP
JTAG_CPU_TDO_3V3
JTAG_NB_TDO
SMU_CPU_NB_SEL
VIH=2V
SMU_JTAG_TDO
NC_JTAGMUX_3
C3070 0.1UF
SMU JTAG TDI TO CPU (BACKUP PLAN)
=PPV_EI_CPU
R3084 1K
NOSTUFF R3085 33
JTAG_CPU_TDI
R3083 4.7K
Q3081 2N7002DW-X-F SOT-363
SMU_JTAG_TDI
Q3080 2N7002DW-X-F SOT-363
NB JTAG IS A DEVELOPMENT ONLY FEATURE
=PP2V5_PWRON_NB_MISC
DEVELOPMENT C3031 0.1UF
VCC RANGE 0.8V - 2.7V
DEVELOPMENT U3031 SN74AUC2G34 SOT23-6
R3034 10K
DEVELOPMENT R3032 33
JTAG_NB_TDI
VIH = 2.0V, 3.3V TOLERANT
=PP2V5_PWRON_NB_MISC
R3035 10K
PULLUP IF KODIAK JTAG IS NOSTUFFED
VCC RANGE 0.8V - 2.7V
DEVELOPMENT U3031 SN74AUC2G34 SOT23-6
VIH = 2.0V, 3.3V TOLERANT
DEVELOPMENT R3033 33
JTAG_NB_TCK
SHARE CPU AND NB JTAG TMS WITH SMU
=PP2V5_PWRON_NB_MISC
C3071 0.1UF
PCB: PLACE U3071 NEAR SMU OR NEAR KODIAK.
CRITICAL
U3071 74LVC1G SC70-6
TO LEVEL SHIFTER
SMU_CPU_TMS
3.3V TOLERANT
STRAIGHT TO NB
JTAG_NB_TMS
SMU_JTAG_TMS
LEVEL SHIFT TDO FROM CPU TO MUX
=PP3V3_PWRON_SMU
R3051 1K
R3052 100
JTAG_CPU_TDO_L
JTAG_CPU_TDO_3V3
JTAG_CPU_TDO_R
R3050 10K
JTAGCPU_TDO
Q3050 2N3904LF SOT23
Q3021 2N7002DW-X-F SOT-363
PCB: PLACE R3050, Q3050, R3051 NEAR CPU. PLACE Q3021, R3052 NEAR SMU.
PULLDOWNS TO BUFFERS/LOGIC GATES
R3036 100K SMU_JTAG_TDI
R3037 100K SMU_JTAG_TCK
R3070 100K SMU_JTAG_TMS
R3071 100K SMU_CPU_NB_SEL
SMU SUPPLEMENTAL (3)
SYNC_MASTER=FINO-MS
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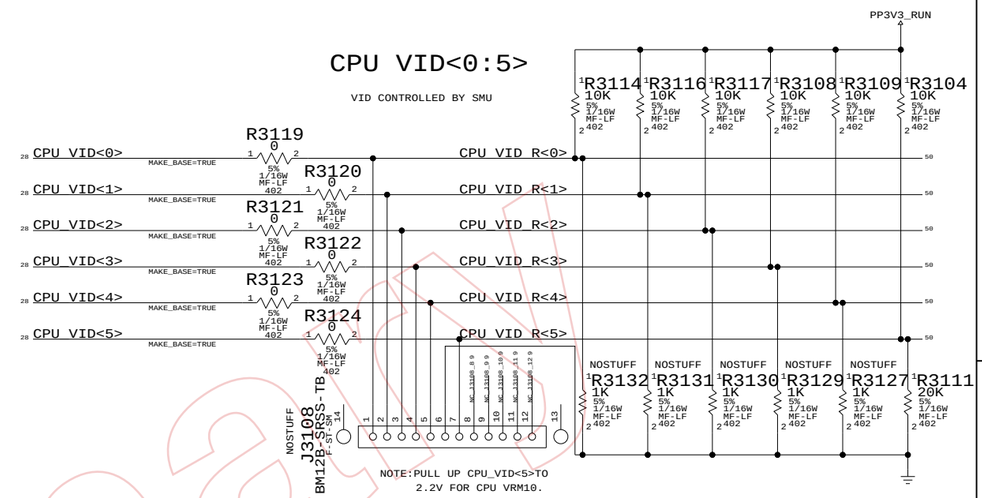
SMU ALIASES

ALIASES ARE ONLY NECESSARY WHERE USE DIFFERS FROM Q63.

COMMENT (ONLY IF USE DIFFERS FROM Q63)	M23 NET NAME	M23 SMU ALLOCATION		Q63 NET NAME (SHARED PAGE)
		CPU_SENSE_I0	P0.0	
		CPU_SENSE_V0	P0.1	
Q63 NC'S THESE AS IT USES A SAT.		CPU_TEMP0	P0.2	
		CPU_BYPASS	P0.3	
M23/M33 DOESN'T HAVE THOSE FANS.	9 NC_SMU_FAN_RPM3	FAN_CNTL0_4	P0.4	SMU_FAN_RPM3 28
	9 NC_SMU_FAN_RPM4	FAN_CNTL0_5	P0.5	SMU_FAN_RPM4 28
	9 NC_SMU_FAN_RPM5	FAN_CNTL0_6	P0.6	SMU_FAN_RPM5 28
Q63 USES SMU_SER_SEL FOR SPDIF-SMU-DEBUG. NOT M23/M33 FEATURE.	9 NC_SMU_SER_SEL	SMU_SCCL_SEL	P0.7	SMU_SER_SEL 28
M23/M33 DOESN'T USE. P1.0 NC ON PG 7.		CPU_SENSE_I1	P1.0	
		CPU_SENSE_V1	P1.1	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		CPU_TEMP1	P1.2	
		PS1_3	P1.3	
M23/M33 DOESN'T USE P1.4. NC ON PG 7.		PS1_4	P1.4	
		POWERFAIL*	P1.5	
CPU_VID_LE0 FOR Q82. NOT M23/M33 FEATURE.	9 NC_SMU_CPU_VID_LE0	CPU_VID_LE0	P1.6	SMU_FAN_TACH9 28
CONSIDER DOOR_AJAR FOR M23/M33 DIMM ACCESS DOOR?	9 NC_SYS_DOOR_AJAR_L	DOOR_AJAR*	P1.7	SYS_DOOR_AJAR_L 28
CPU_VID_LE1 FOR Q82. NOT M23/M33 FEATURE.	9 NC_SMU_CPU_VID_LE1	CPU_VID_LE1	P2.0	SMU_FAN_TACH6 28
M23/M33 DOESN'T HAVE THIS FAN.	9 NC_SMU_FAN_TACH7	FAN_TACH2_1	P2.1	SMU_FAN_TACH7 28
		FAN_TACH2_2	P2.2	
		FAN_TACH2_3	P2.3	
		FAN_TACH2_4	P2.4	
M23/M33 DOESN'T HAVE FAN TACHS P2.5, P2.6, P2.7.	9 NC_SMU_FAN_TACH3	FAN_TACH2_5	P2.5	SMU_FAN_TACH3 28
M23/M33 USES TACH0 (P2.2), TACH1 (P2.3), TACH2 (P2.4) ONLY.	9 NC_SMU_FAN_TACH4	FAN_TACH2_6	P2.6	SMU_FAN_TACH4 28
	9 NC_SMU_FAN_TACH5	FAN_TACH2_7	P2.7	SMU_FAN_TACH5 28
M23/M33 ONLY CONNECTS I2C TO KODIAK NOW; CPU HAS PULLUPS ON ITS PG.	39 28 I2C_SMU_A_SDA	IIC_A_DAT	P3.0	I2C_SMU_A_SDA_IN 28
	39 28 I2C_SMU_A_SCL	IIC_A_CLK	P3.1	I2C_SMU_A_SDA_OUT_L 28
	39 SMU_JTAG_TDI	TDI	P3.2	I2C_SMU_A_SCL_IN 28
	39 SMU_JTAG_TCK	TCK	P3.3	I2C_SMU_A_SCL_OUT_L 28
		IIC_E_DAT	P3.4	
		IIC_E_CLK	P3.5	
		DIAG_LED	P3.6	
		OVERTEMP*	P3.7	
		CPU_VID[0]	P6.0	
		CPU_VID[1]	P6.1	
		CPU_VID[2]	P6.2	
		CPU_VID[3]	P6.3	
		CPU_VID[4]	P6.4	
		CPU_VID[5]	P6.5	
		DEBUG_RXD	P6.6	
		DEBUG_TXD	P6.7	
		IIC_B_DAT	P7.0	
		IIC_B_CLK	P7.1	
Q63 USE OF P7.2 IS PWM FAN SELECT BETWEEN CPU OR NB TMS AND TDO FROM/TO SMU	38 SMU_CPU_NB_SEL	CPU_TMS	P7.2	I2C_SMU_CPU_SDA_IN 28
		FAN_CNTL7_3	P7.3	
M23/M33 DOESN'T HAVE THIS FAN (P7.4)	9 NC_I2C_SMU_CPU_SCL_IN	FAN_CNTL7_4	P7.4	I2C_SMU_CPU_SCL_IN 28
M23/M33 USES FAN_RPM0 (P7.3), FAN_RPM1 (P7.5), FAN_RPM2 (P7.7) ONLY.		FAN_CNTL7_5	P7.5	
		VDNAP2	P7.6	
		FAN_CNTL7_7	P7.7	
		SYSTEM_LED	P8.0	
		NB_RESET*	P8.1	
		PME*	P8.2	
M23/M33 DOESN'T NEED TO MAKE VDNAP0 DO TRIPLE-DUTY.	24 SB_VDNAP0	VDNAP0	P8.3	SB_CPU_VDNAP0_OR_OREQ_OR_SPDIF 28
		SLEWING*	P8.4	
	39 SMU_JTAG_TMS	NB_TMS	P8.5	I2C_SMU_CPU_SDA_OUT_L 28
		POWERUP*	P8.6	
		SLEEP	P8.7	
		CLK_RESET*	P9.0	
Q63 USE OF P9.1 IS TACH 8.	29 CPU_HRESET	CPU_HRESET	P9.1	SMU_FAN_TACH8 28
		SMU_DOORBELL*	P9.2	
		STOP_XTAL*	P9.3	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		PS9_5	P9.5	
		PS9_6	P9.6	
M23/M33 HAS NO SLOTS.	9 NC_SLOT_TOTAL_PWR	SLOT_TOTAL_PWR	P9.7	SYS_SLOT_PWR 28
		VDNAP1	P10.0	
		IO_RESET*	P10.1	
		SUSPEND_ACK*	P10.2	
		SUSPEND_IO_ACK*	P10.3	
		SUSPEND_REQ*	P10.4	
		PWR_BUTTON*	P10.5	
		RST_BUTTON*	P10.6	
	39 SMU_JTAG_TDO	TDO	P10.7	I2C_SMU_CPU_SCL_OUT_L 28



Preliminary

SMU SUPPLEMENTAL (4)

SYNC_MASTER=FINO-MS SYNC_DATE=05/18/2005

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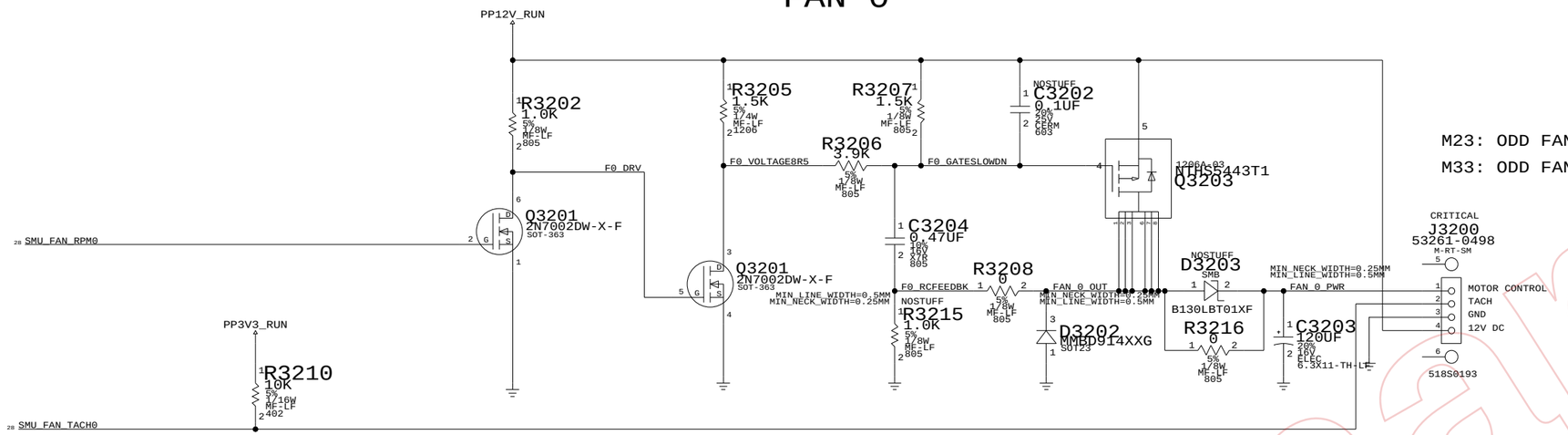
FAN 0



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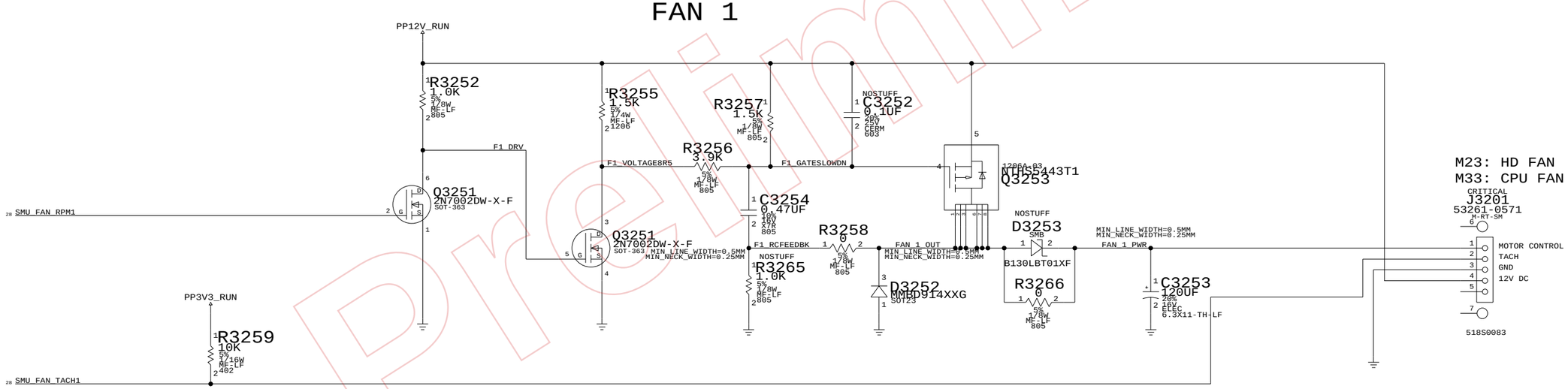

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Fan 0, 1 & System Temp

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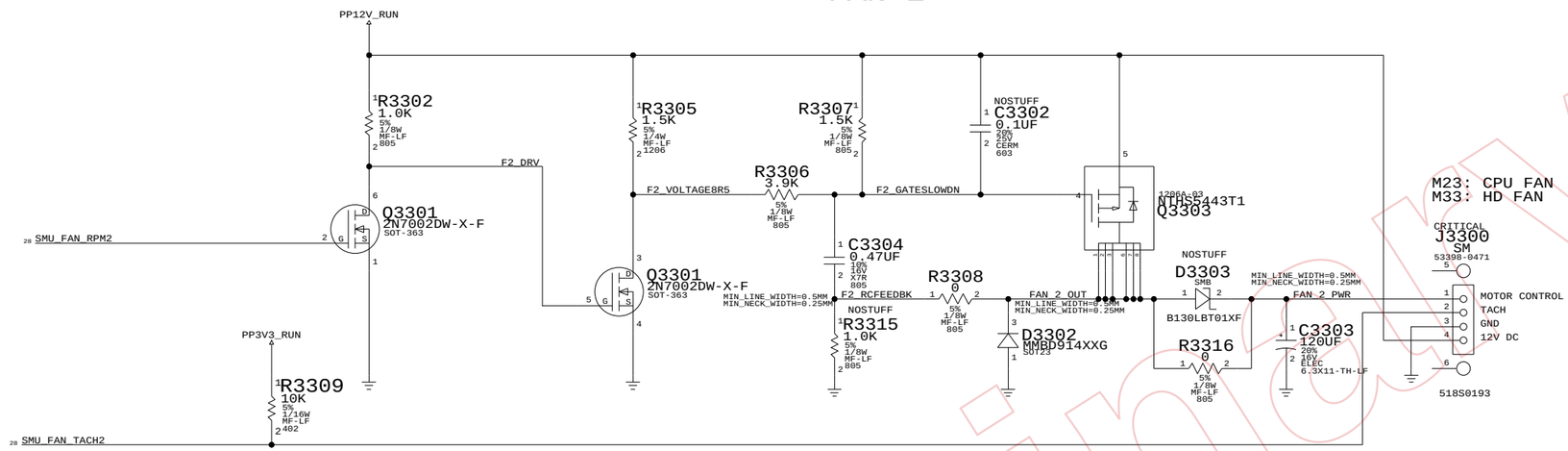
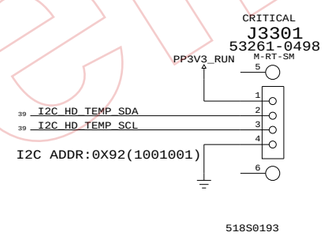
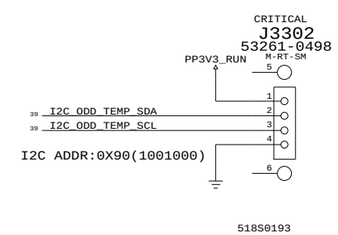
FAN 2



HD TEMP SENSOR



ODD TEMP SENSOR



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Fan 2 & HD Temp		
SYNC_MASTER=FINO-PC	SYNC_DATE=05/18/2005	

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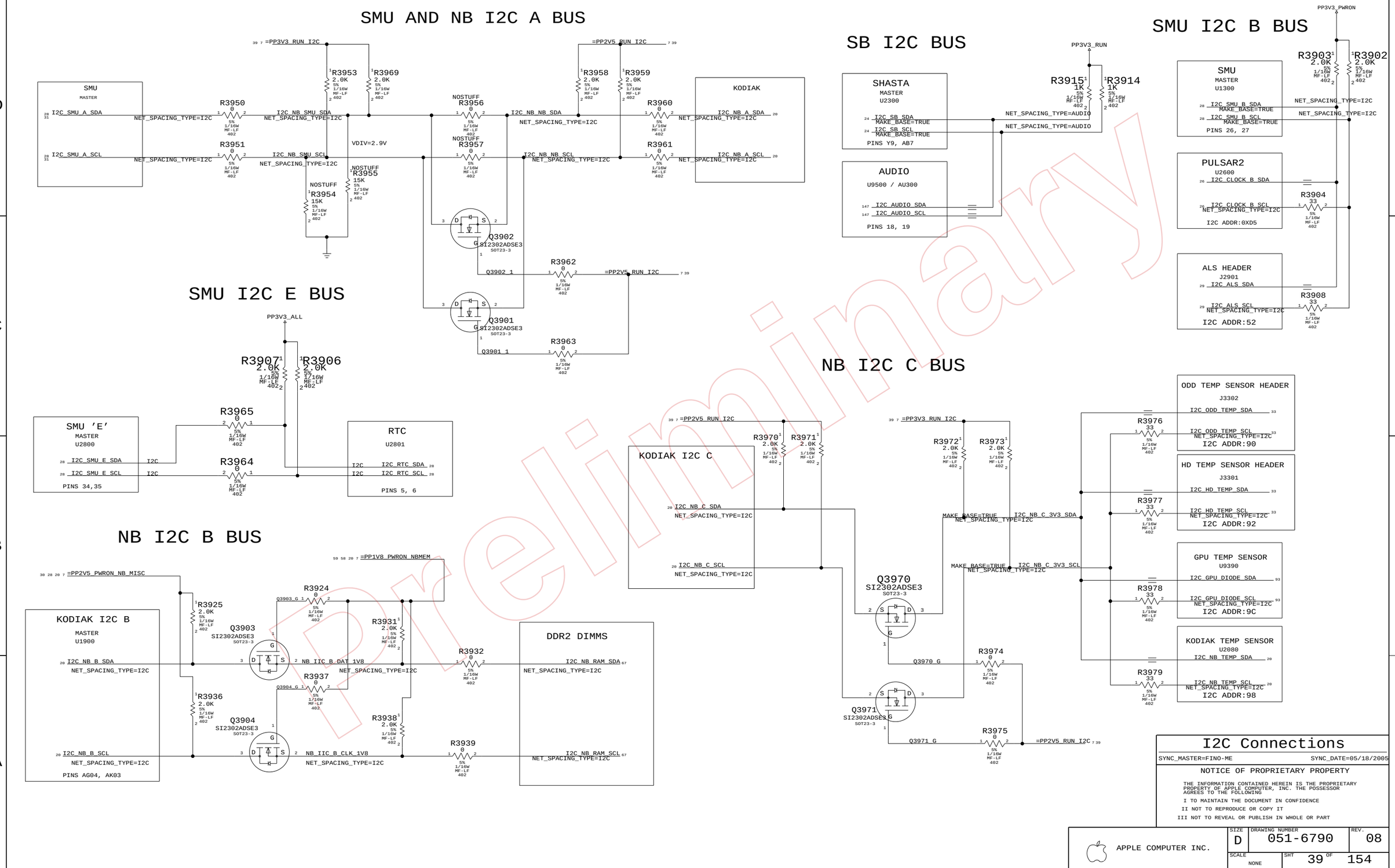

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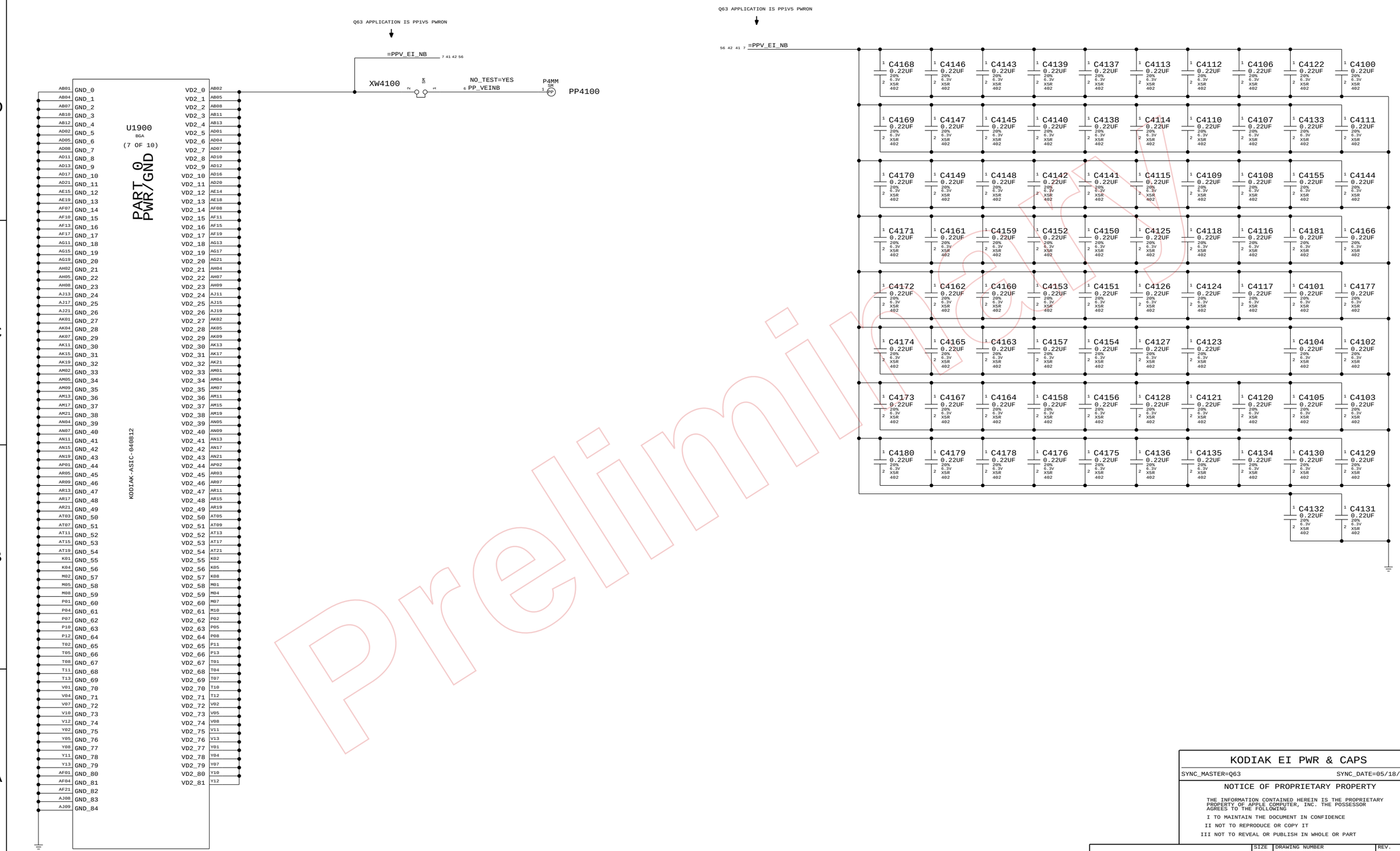

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KODIAK EI PWR & CAPS

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

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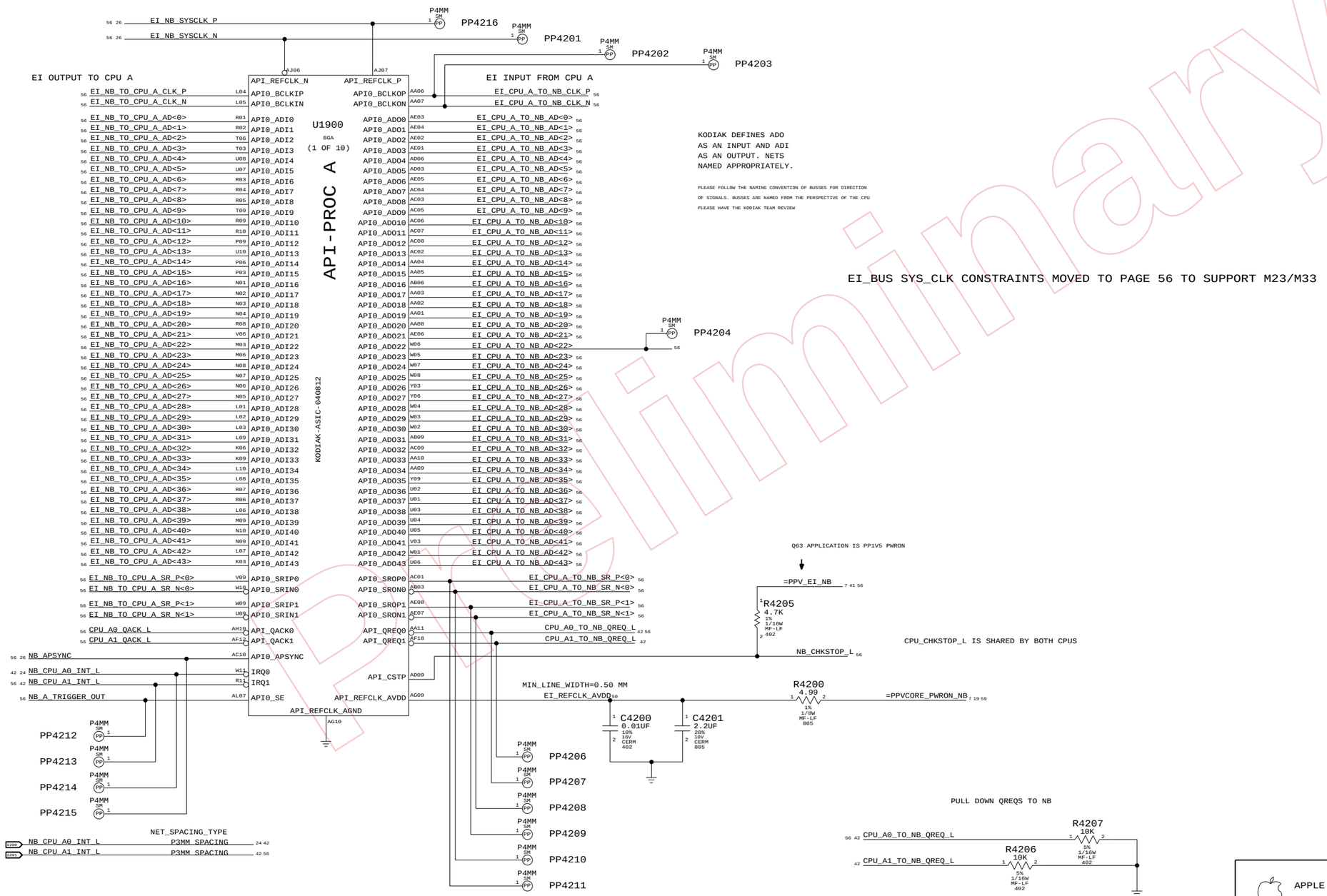

KODIAK DEFINES ADO
AS AN INPUT AND ADI
AS AN OUTPUT. NETS
NAMED APPROPRIATELY.

PLEASE FOLLOW THE NAMING CONVENTION OF BUSSES FOR DIRECTION
OF SIGNALS. BUSSES ARE NAMED FROM THE PERSPECTIVE OF THE CPU
PLEASE HAVE THE KODIAK TEAM REVIEW

EI_BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

Q63 APPLICATION IS PP1V5 PWRON

CPU_CHKSTOP_L IS SHARED BY BOTH CPUS

MIN_LINE_WIDTH=0.50 MM

PULL DOWN QREQS TO NB

Preliminary

KODIAK EI A

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

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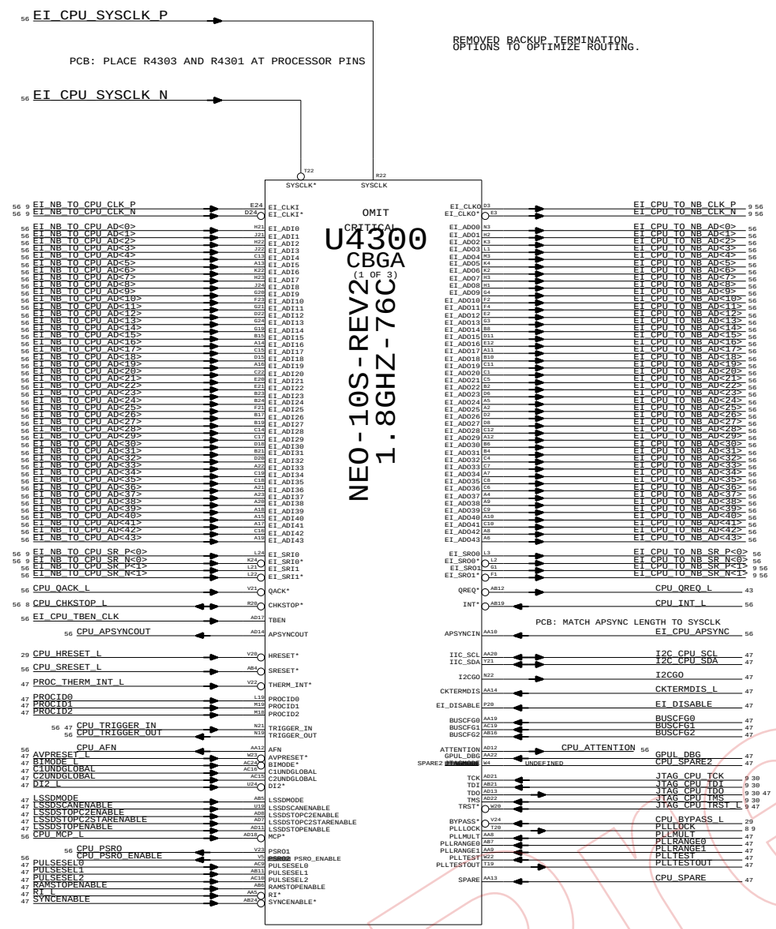
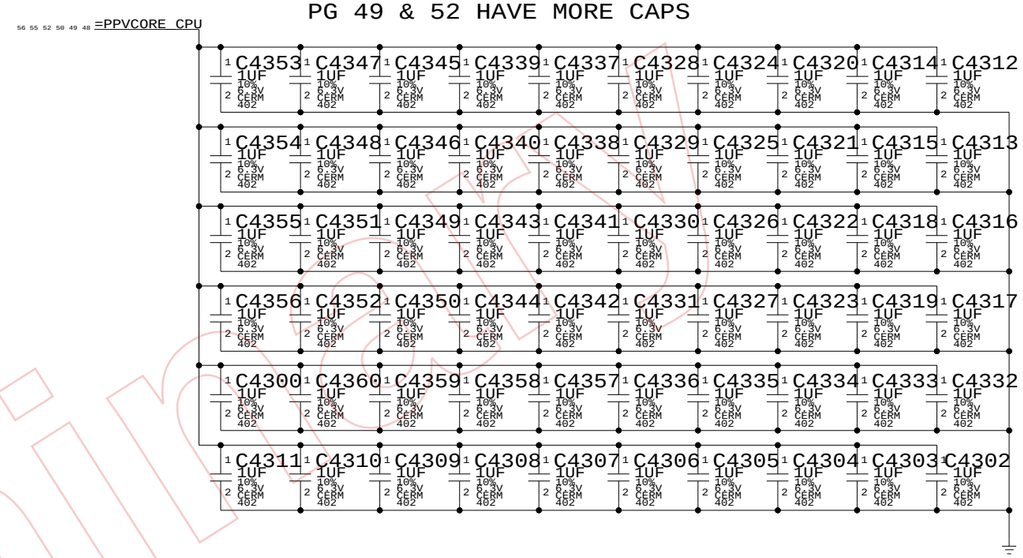
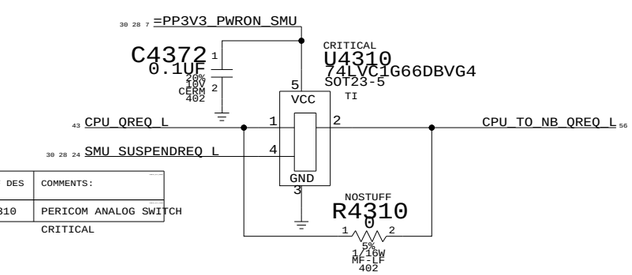


PG 49 & 52 HAVE MORE CAPS



QREQ_L AND SUSPENDREQ_L AND HACK

SAME AS Q45



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0920	353S0867		U4310	PERICOM ANALOG SWITCH CRITICAL

CPU EI AND IO

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PLEASE HAVE THE KODIAK TEAM REVIEW

EI OUTPUT TO CPU B

EI INPUT FROM CPU B

U1900
BGA
(2 OF 10)
API-PROC B
KODIAK-ASIC-040812

Signal	Pin	Pin	Signal
EI_NB_TO_CPU_B_CLK_P	AT08	API1_BCLKIP	API1_BCLKOP AT16
EI_NB_TO_CPU_B_CLK_N	AR08	API1_BCLKIN	API1_BCLKON AR16
EI_NB_TO_CPU_B_AD<0>	AM12	API1_ADI0	API1_AD00 AP20
EI_NB_TO_CPU_B_AD<1>	AN12	API1_ADI1	API1_AD01 AN20
EI_NB_TO_CPU_B_AD<2>	AL12	API1_ADI2	API1_AD02 AR20
EI_NB_TO_CPU_B_AD<3>	AK12	API1_ADI3	API1_AD03 AT20
EI_NB_TO_CPU_B_AD<4>	AP11	API1_ADI4	API1_AD04 AL19
EI_NB_TO_CPU_B_AD<5>	AL11	API1_ADI5	API1_AD05 AP19
EI_NB_TO_CPU_B_AD<6>	AP12	API1_ADI6	API1_AD06 AM20
EI_NB_TO_CPU_B_AD<7>	AR12	API1_ADI7	API1_AD07 AM18
EI_NB_TO_CPU_B_AD<8>	AT12	API1_ADI8	API1_AD08 AL18
EI_NB_TO_CPU_B_AD<9>	AH12	API1_ADI9	API1_AD09 AN18
EI_NB_TO_CPU_B_AD<10>	AG12	API1_ADI10	API1_AD010 AP18
EI_NB_TO_CPU_B_AD<11>	AH13	API1_ADI11	API1_AD011 AR18
EI_NB_TO_CPU_B_AD<12>	AJ12	API1_ADI12	API1_AD012 AT18
EI_NB_TO_CPU_B_AD<13>	AG14	API1_ADI13	API1_AD013 AK18
EI_NB_TO_CPU_B_AD<14>	AM10	API1_ADI14	API1_AD014 AP17
EI_NB_TO_CPU_B_AD<15>	AL10	API1_ADI15	API1_AD015 AL17
EI_NB_TO_CPU_B_AD<16>	AN10	API1_ADI16	API1_AD016 AH20
EI_NB_TO_CPU_B_AD<17>	AP10	API1_ADI17	API1_AD017 AJ20
EI_NB_TO_CPU_B_AD<18>	AR10	API1_ADI18	API1_AD018 AK20
EI_NB_TO_CPU_B_AD<19>	AT10	API1_ADI19	API1_AD019 AH19
EI_NB_TO_CPU_B_AD<20>	AK10	API1_ADI20	API1_AD020 AG20
EI_NB_TO_CPU_B_AD<21>	AJ10	API1_ADI21	API1_AD021 AL20
EI_NB_TO_CPU_B_AD<22>	AM08	API1_ADI22	API1_AD022 AM16
EI_NB_TO_CPU_B_AD<23>	AN08	API1_ADI23	API1_AD023 AN16
EI_NB_TO_CPU_B_AD<24>	AL08	API1_ADI24	API1_AD024 AL16
EI_NB_TO_CPU_B_AD<25>	AP07	API1_ADI25	API1_AD025 AK16
EI_NB_TO_CPU_B_AD<26>	AT06	API1_ADI26	API1_AD026 AP15
EI_NB_TO_CPU_B_AD<27>	AR06	API1_ADI27	API1_AD027 AL15
EI_NB_TO_CPU_B_AD<28>	AP08	API1_ADI28	API1_AD028 AP16
EI_NB_TO_CPU_B_AD<29>	AT04	API1_ADI29	API1_AD029 AM14
EI_NB_TO_CPU_B_AD<30>	AR04	API1_ADI30	API1_AD030 AL14
EI_NB_TO_CPU_B_AD<31>	AP05	API1_ADI31	API1_AD031 AN14
EI_NB_TO_CPU_B_AD<32>	AM06	API1_ADI32	API1_AD032 AP14
EI_NB_TO_CPU_B_AD<33>	AN06	API1_ADI33	API1_AD033 AR14
EI_NB_TO_CPU_B_AD<34>	AP06	API1_ADI34	API1_AD034 AT14
EI_NB_TO_CPU_B_AD<35>	AP04	API1_ADI35	API1_AD035 AK14
EI_NB_TO_CPU_B_AD<36>	AM03	API1_ADI36	API1_AD036 AP13
EI_NB_TO_CPU_B_AD<37>	AN01	API1_ADI37	API1_AD037 AL13
EI_NB_TO_CPU_B_AD<38>	AL06	API1_ADI38	API1_AD038 AG16
EI_NB_TO_CPU_B_AD<39>	AL05	API1_ADI39	API1_AD039 AH15
EI_NB_TO_CPU_B_AD<40>	AL04	API1_ADI40	API1_AD040 AJ14
EI_NB_TO_CPU_B_AD<41>	AL03	API1_ADI41	API1_AD041 AH14
EI_NB_TO_CPU_B_AD<42>	AN02	API1_ADI42	API1_AD042 AH16
EI_NB_TO_CPU_B_AD<43>	AN03	API1_ADI43	API1_AD043 AH17
EI_NB_TO_CPU_B_SR_P<0>	AP09	API1_SRIP0	API1_SROP0 AG18
EI_NB_TO_CPU_B_SR_N<0>	AL09	API1_SRIN0	API1_SRON0 AJ16
EI_NB_TO_CPU_B_SR_P<1>	AR02	API1_SRIP1	API1_SROP1 AJ18
EI_NB_TO_CPU_B_SR_N<1>	AP02	API1_SRIN1	API1_SRON1 AH18
CPU_B0_QACK_L	AF12	API_QACK2	API_QREQ2 AF16
CPU_B1_QACK_L	AC12	API_QACK3	API_QREQ3 AF20
NB_CPU_B0_INT_L	N12	IRQ2	
NB_CPU_B1_INT_L	U12	IRQ3	
TP_NB_APSYNC	AH11	API1_APSYNC	
NB_B_TRIGGER_OUT	AK08	API1_SE	

Signal	Pin	Pin	Signal
EI_CPU_B_TO_NB_CLK_P			EI_CPU_B_TO_NB_CLK_P
EI_CPU_B_TO_NB_CLK_N			EI_CPU_B_TO_NB_CLK_N
EI_CPU_B_TO_NB_AD<0>			EI_CPU_B_TO_NB_AD<0>
EI_CPU_B_TO_NB_AD<1>			EI_CPU_B_TO_NB_AD<1>
EI_CPU_B_TO_NB_AD<2>			EI_CPU_B_TO_NB_AD<2>
EI_CPU_B_TO_NB_AD<3>			EI_CPU_B_TO_NB_AD<3>
EI_CPU_B_TO_NB_AD<4>			EI_CPU_B_TO_NB_AD<4>
EI_CPU_B_TO_NB_AD<5>			EI_CPU_B_TO_NB_AD<5>
EI_CPU_B_TO_NB_AD<6>			EI_CPU_B_TO_NB_AD<6>
EI_CPU_B_TO_NB_AD<7>			EI_CPU_B_TO_NB_AD<7>
EI_CPU_B_TO_NB_AD<8>			EI_CPU_B_TO_NB_AD<8>
EI_CPU_B_TO_NB_AD<9>			EI_CPU_B_TO_NB_AD<9>
EI_CPU_B_TO_NB_AD<10>			EI_CPU_B_TO_NB_AD<10>
EI_CPU_B_TO_NB_AD<11>			EI_CPU_B_TO_NB_AD<11>
EI_CPU_B_TO_NB_AD<12>			EI_CPU_B_TO_NB_AD<12>
EI_CPU_B_TO_NB_AD<13>			EI_CPU_B_TO_NB_AD<13>
EI_CPU_B_TO_NB_AD<14>			EI_CPU_B_TO_NB_AD<14>
EI_CPU_B_TO_NB_AD<15>			EI_CPU_B_TO_NB_AD<15>
EI_CPU_B_TO_NB_AD<16>			EI_CPU_B_TO_NB_AD<16>
EI_CPU_B_TO_NB_AD<17>			EI_CPU_B_TO_NB_AD<17>
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EI_CPU_B_TO_NB_AD<21>			EI_CPU_B_TO_NB_AD<21>
EI_CPU_B_TO_NB_AD<22>			EI_CPU_B_TO_NB_AD<22>
EI_CPU_B_TO_NB_AD<23>			EI_CPU_B_TO_NB_AD<23>
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EI_CPU_B_TO_NB_AD<39>			EI_CPU_B_TO_NB_AD<39>
EI_CPU_B_TO_NB_AD<40>			EI_CPU_B_TO_NB_AD<40>
EI_CPU_B_TO_NB_AD<41>			EI_CPU_B_TO_NB_AD<41>
EI_CPU_B_TO_NB_AD<42>			EI_CPU_B_TO_NB_AD<42>
EI_CPU_B_TO_NB_AD<43>			EI_CPU_B_TO_NB_AD<43>
			EI_CPU_B_TO_NB_SR_P<0>
			EI_CPU_B_TO_NB_SR_N<0>
			EI_CPU_B_TO_NB_SR_P<1>
			EI_CPU_B_TO_NB_SR_N<1>
			CPU_B0_TO_NB_QREQ_L
			CPU_B1_TO_NB_QREQ_L

KODIAK DEFINES ADO
AS AN INPUT AND ADI
AS AN OUTPUT. NETS
NAMED APPROPRIATELY.

WE MAY NEED A DIFFERENT
ELECTRICAL_CONSTRAINT_SET
FOR CPU_A AND CPU_B.

EI_BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

WIRE TP_NB_APSYNC TO A TEST POINT

NET_SPACING_TYPE
NB_CPU_B0_INT_L P3MM_SPACING
NB_CPU_B1_INT_L P3MM_SPACING

PULL DOWN QREQS TO NB

CPU_B0_TO_NB_QREQ_L — R4407 10K 5% 1/16W MF-LF 402
CPU_B1_TO_NB_QREQ_L — R4406 10K 5% 1/16W MF-LF 402

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KODIAK EI B	
SYNC_MASTER=Q63	SYNC_DATE=05/18/2005

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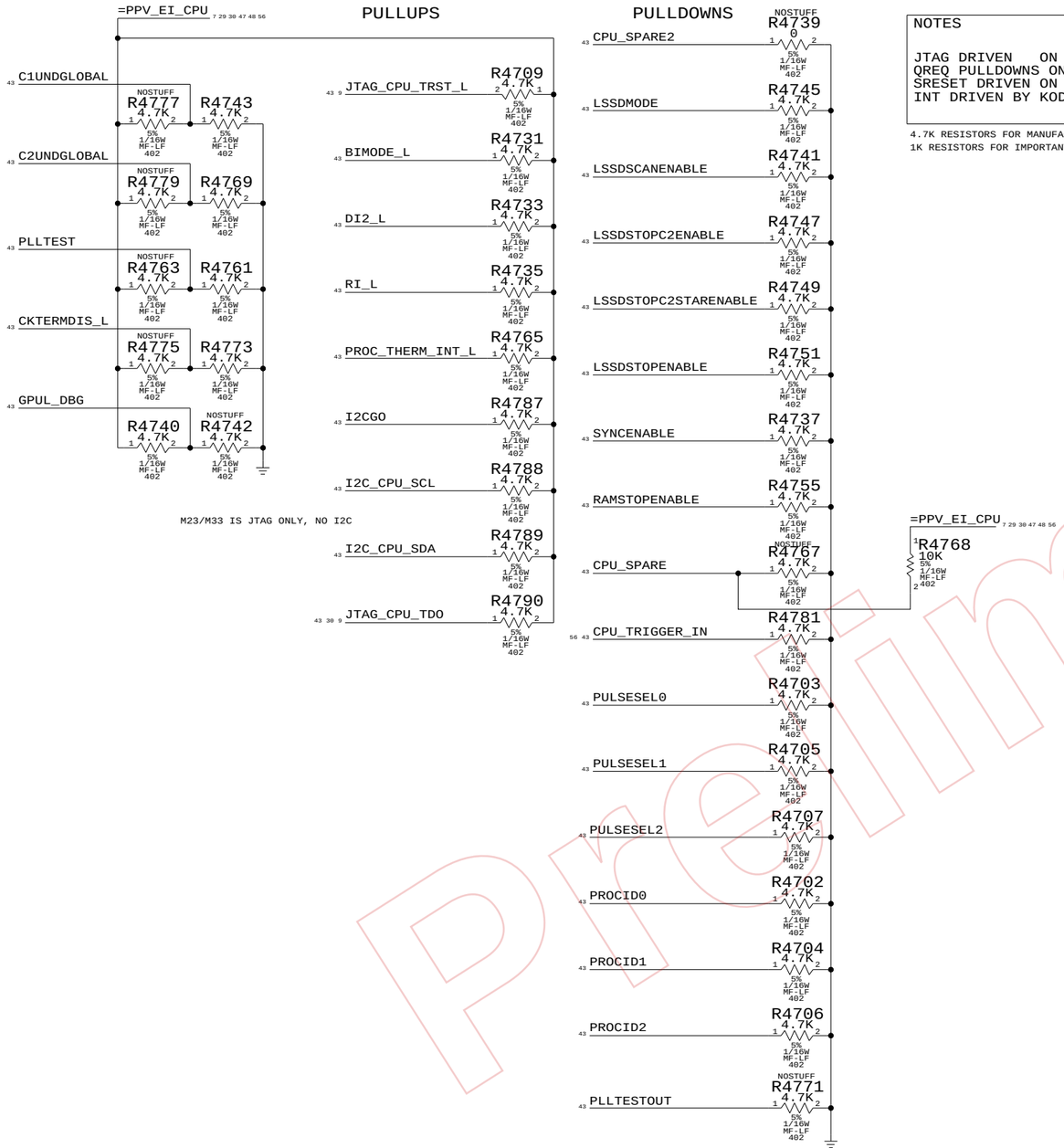
TITLE=KLLOOOAA
ABBREV=OOOAOOAA



M23/M33 IS JTAG ONLY, NO I2C

NOTES

JTAG DRIVEN ON SMU PG 30
QREQ PULLDOWNS ON Q63 SHARED PAGE
SRESET DRIVEN ON PG 56
INT DRIVEN BY KODIAK

4.7K RESISTORS FOR MANUFACTURING-TEST-TYPE PULLUPS OR PULLDOWNS.
1K RESISTORS FOR IMPORTANT USE OR STRAPPING OPTIONS.

SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4734	EI_3TO1	SYSCLK * 12
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4718	EI_2TO1	SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4728	EI_2TO1	PROC / 2
*	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4712	EI_3TO1	PROC / 3
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4728	NOSTUFF	PROC / 4
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4712	NOSTUFF	PROC / 6
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4728	NOSTUFF	PROC / 8
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4712	NOSTUFF	PROC / 12
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4728	NOSTUFF	PROC / 16
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4712	NOSTUFF	

SELECT ELASTIC MODE OR BYPASS.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4736		
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4720	NOSTUFF	BYPASS MODE

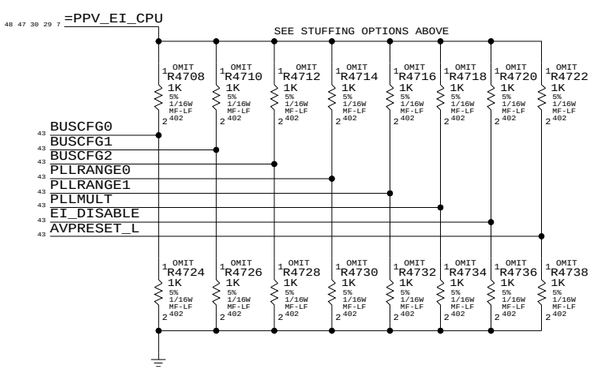
SELECT PLL FREQUENCY RANGE.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4732	CPU_PLL_LOW	
>= 1.8 GHZ *	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4716	CPU_PLL_HIGH	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4732	CPU_PLL_MEDIUM	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4716	NOSTUFF	RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4722		AVPRESET OFF
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4738	NOSTUFF	AVPRESET ON

* STUFF THESE ON M23.

PROCESSOR BUS CONFIGURATION



CPU STRAPS

SYNC_MASTER=FINO-MS SYNC_DATE=05/18/2005

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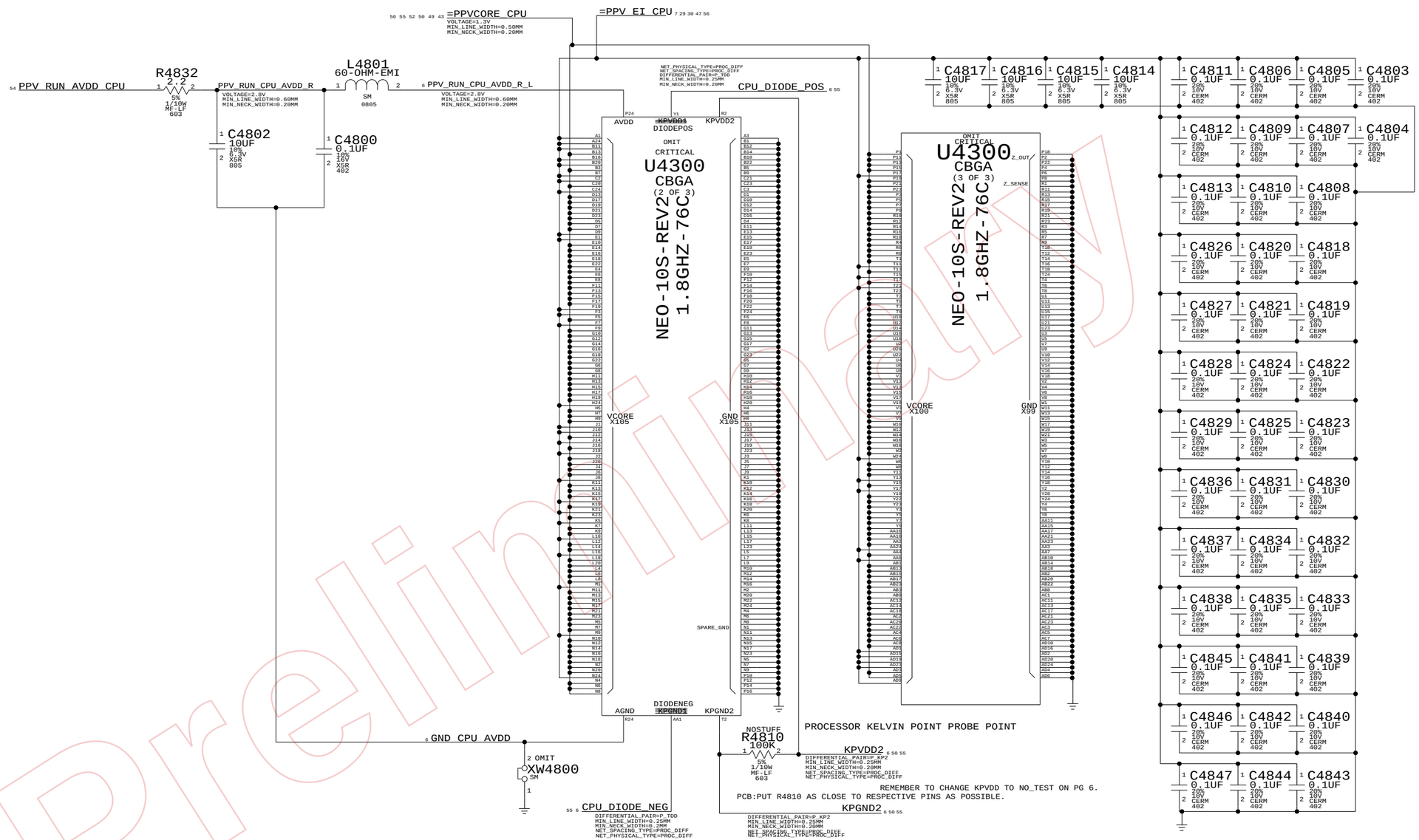

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CPU POWER AND BYPASS

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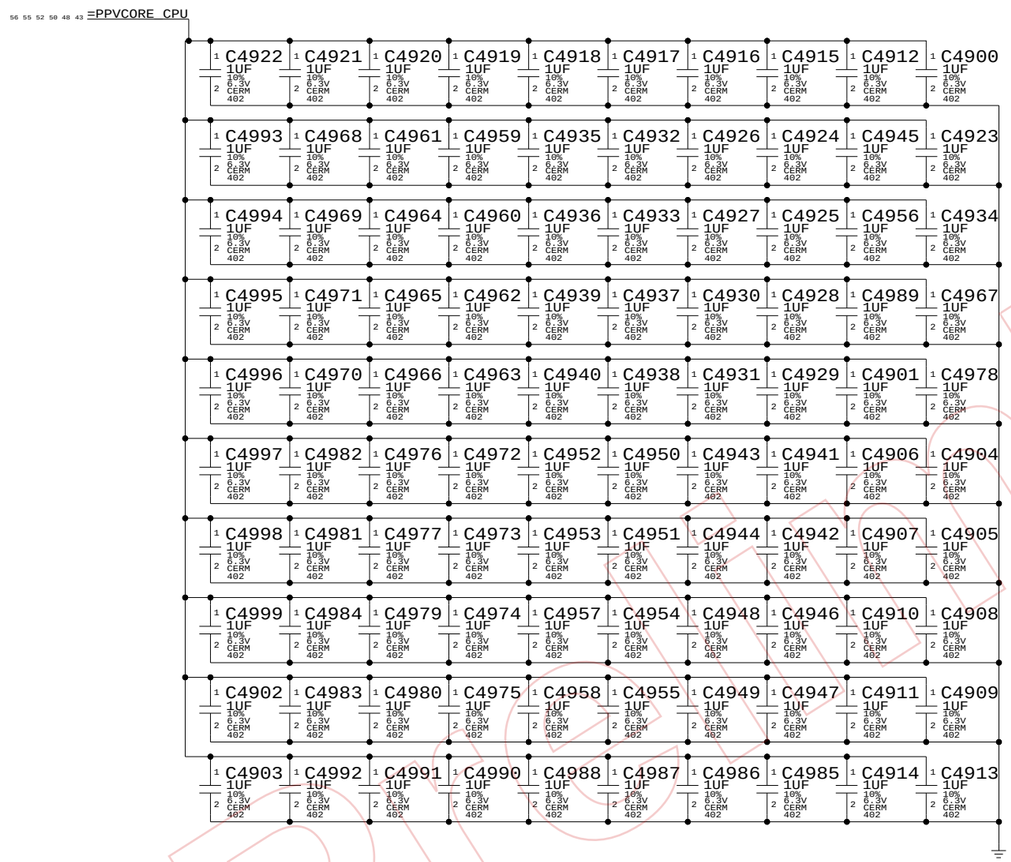

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PROC DECOUPLING

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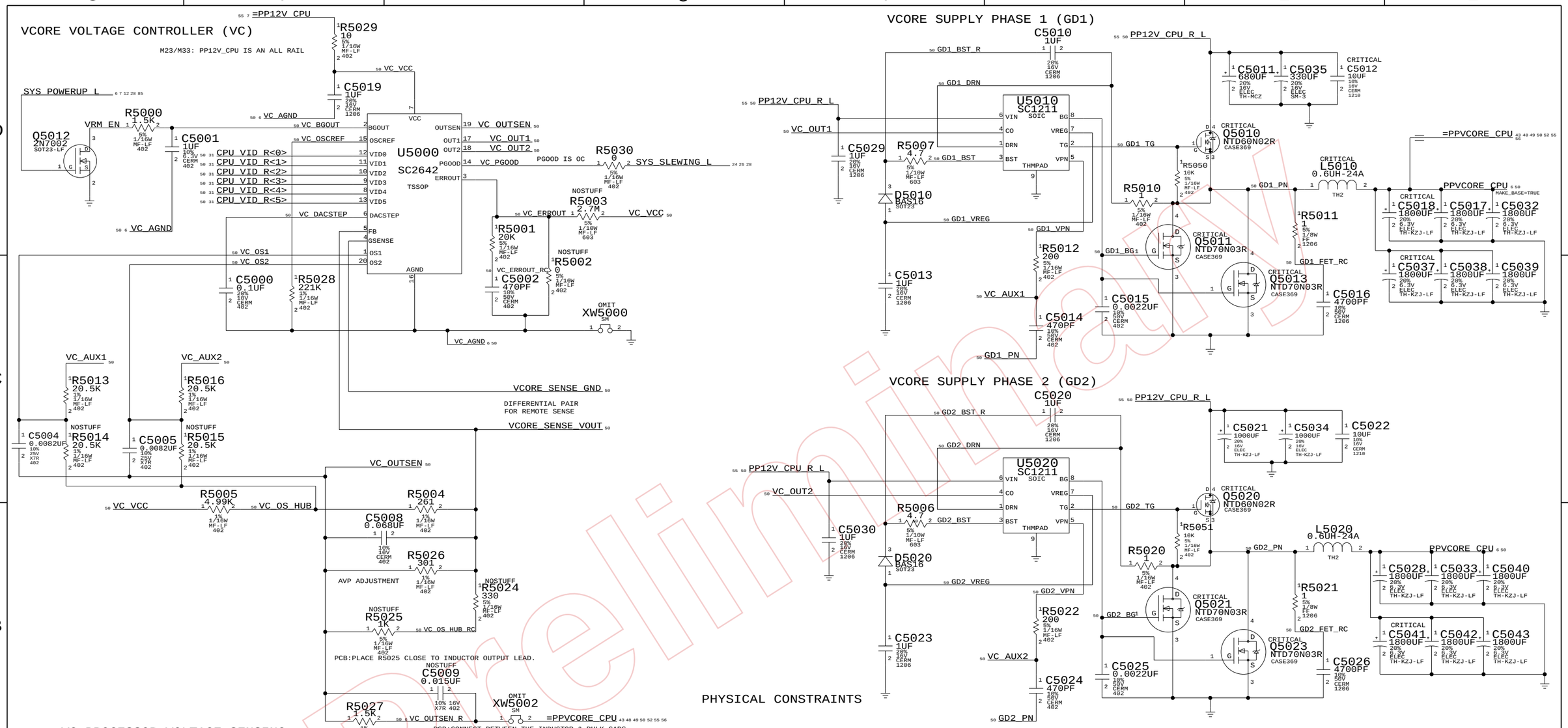

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
VC_OSCREF	0.25 MM	0.20 MM
CPU_VID_R<0..5>	0.25 MM	0.20 MM
VC_DACSTEP	0.25 MM	0.20 MM
VC_AGND	0.50 MM	0.20 MM
VC_BGOUT	0.25 MM	0.20 MM
VC_OS1	0.25 MM	0.20 MM
VC_OS2	0.25 MM	0.20 MM
VC_VCC	0.25 MM	0.25 MM
VC_OS_HUB	0.25 MM	0.20 MM
VC_OUTSEN	0.25 MM	0.20 MM
VC_OUTSEN_R	0.25 MM	0.20 MM
VCORE_SENSE_GND	0.25 MM	0.20 MM
VCORE_SENSE_VOUT	0.25 MM	0.20 MM
VC_AUX1	0.25 MM	0.25 MM
VC_AUX2	0.25 MM	0.25 MM
VC_OUT1	0.45 MM	0.25 MM
VC_OUT2	0.45 MM	0.25 MM
VC_ERROUT	0.25 MM	0.20 MM
VC_ERROUT_RC	0.25 MM	0.20 MM
VC_OS_HUB_RC	0.25 MM	0.20 MM
EI_REFCLK_AVDD	0.50 MM	0.08 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GD1_DRN	0.25 MM	0.25 MM
GD1_BST	0.25 MM	0.25 MM
GD1_VREG	0.25 MM	0.25 MM
GD1_VPN	0.25 MM	0.25 MM
GD1_TG	0.25 MM	0.25 MM
GD1_BG	0.25 MM	0.25 MM
GD1_FET_RC	0.25 MM	0.25 MM
GD1_PN	0.60 MM	0.25 MM
GD1_BST_R	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GD2_DRN	0.25 MM	0.25 MM
GD2_BST	0.25 MM	0.25 MM
GD2_VREG	0.25 MM	0.25 MM
GD2_VPN	0.25 MM	0.25 MM
GD2_TG	0.25 MM	0.25 MM
GD2_BG	0.25 MM	0.25 MM
GD2_FET_RC	0.25 MM	0.25 MM
GD2_PN	0.60 MM	0.25 MM
GD2_BST_R	0.25 MM	0.25 MM

CPU VCORE VREG

SYNC_MASTER=M23-MS SYNC_DATE=05/18/2005

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56 55 50 49 48 43 =PPVCORE_CPU

CRITICAL

C5200 10UF 10% 6.3V X5R 805	C5212 10UF 10% 6.3V X5R 805	C5223 10UF 10% 6.3V X5R 805	C5234 10UF 10% 6.3V X5R 805	C5245 10UF 10% 6.3V X5R 805	C5201 10UF 10% 6.3V X5R 805	C5289 10UF 10% 6.3V X5R 805	C5278 10UF 10% 6.3V X5R 805	C5267 10UF 10% 6.3V X5R 805	C5256 10UF 10% 6.3V X5R 805
C5213 10UF 10% 6.3V X5R 805	C5211 10UF 10% 6.3V X5R 805	C5210 10UF 10% 6.3V X5R 805	C5209 10UF 10% 6.3V X5R 805	C5208 10UF 10% 6.3V X5R 805	C5207 10UF 10% 6.3V X5R 805	C5206 10UF 10% 6.3V X5R 805	C5205 10UF 10% 6.3V X5R 805	C5204 10UF 10% 6.3V X5R 805	C5203 10UF 10% 6.3V X5R 805
C5224 10UF 10% 6.3V X5R 805	C5222 10UF 10% 6.3V X5R 805	C5221 10UF 10% 6.3V X5R 805	C5220 10UF 10% 6.3V X5R 805	C5219 10UF 10% 6.3V X5R 805	C5218 10UF 10% 6.3V X5R 805	C5217 10UF 10% 6.3V X5R 805	C5216 10UF 10% 6.3V X5R 805	C5215 10UF 10% 6.3V X5R 805	C5214 10UF 10% 6.3V X5R 805
C5235 10UF 10% 6.3V X5R 805	C5233 10UF 10% 6.3V X5R 805	C5232 10UF 10% 6.3V X5R 805	C5231 10UF 10% 6.3V X5R 805	C5230 10UF 10% 6.3V X5R 805	C5229 10UF 10% 6.3V X5R 805	C5228 10UF 10% 6.3V X5R 805	C5227 10UF 10% 6.3V X5R 805	C5226 10UF 10% 6.3V X5R 805	C5225 10UF 10% 6.3V X5R 805
C5246 10UF 10% 6.3V X5R 805	C5244 10UF 10% 6.3V X5R 805	C5243 10UF 10% 6.3V X5R 805	C5242 10UF 10% 6.3V X5R 805	C5241 10UF 10% 6.3V X5R 805	C5240 10UF 10% 6.3V X5R 805	C5239 10UF 10% 6.3V X5R 805	C5238 10UF 10% 6.3V X5R 805	C5237 10UF 10% 6.3V X5R 805	C5236 10UF 10% 6.3V X5R 805
C5257 10UF 10% 6.3V X5R 805	C5255 10UF 10% 6.3V X5R 805	C5254 10UF 10% 6.3V X5R 805	C5253 10UF 10% 6.3V X5R 805	C5252 10UF 10% 6.3V X5R 805	C5251 10UF 10% 6.3V X5R 805	C5250 10UF 10% 6.3V X5R 805	C5249 10UF 10% 6.3V X5R 805	C5248 10UF 10% 6.3V X5R 805	C5247 10UF 10% 6.3V X5R 805
C5268 10UF 10% 6.3V X5R 805	C5266 10UF 10% 6.3V X5R 805	C5265 10UF 10% 6.3V X5R 805	C5264 10UF 10% 6.3V X5R 805	C5263 10UF 10% 6.3V X5R 805	C5262 10UF 10% 6.3V X5R 805	C5261 10UF 10% 6.3V X5R 805	C5260 10UF 10% 6.3V X5R 805	C5259 10UF 10% 6.3V X5R 805	C5258 10UF 10% 6.3V X5R 805
C5279 10UF 10% 6.3V X5R 805	C5277 10UF 10% 6.3V X5R 805	C5276 10UF 10% 6.3V X5R 805	C5275 10UF 10% 6.3V X5R 805	C5274 10UF 10% 6.3V X5R 805	C5273 10UF 10% 6.3V X5R 805	C5272 10UF 10% 6.3V X5R 805	C5271 10UF 10% 6.3V X5R 805	C5270 10UF 10% 6.3V X5R 805	C5269 10UF 10% 6.3V X5R 805
C5290 10UF 10% 6.3V X5R 805	C5288 10UF 10% 6.3V X5R 805	C5287 10UF 10% 6.3V X5R 805	C5286 10UF 10% 6.3V X5R 805	C5285 10UF 10% 6.3V X5R 805	C5284 10UF 10% 6.3V X5R 805	C5283 10UF 10% 6.3V X5R 805	C5282 10UF 10% 6.3V X5R 805	C5281 10UF 10% 6.3V X5R 805	C5280 10UF 10% 6.3V X5R 805
C5202 10UF 10% 6.3V X5R 805	C5299 10UF 10% 6.3V X5R 805	C5298 10UF 10% 6.3V X5R 805	C5297 10UF 10% 6.3V X5R 805	C5296 10UF 10% 6.3V X5R 805	C5295 10UF 10% 6.3V X5R 805	C5294 10UF 10% 6.3V X5R 805	C5293 10UF 10% 6.3V X5R 805	C5292 10UF 10% 6.3V X5R 805	C5291 10UF 10% 6.3V X5R 805

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CPU VCORE MORE BYPASS

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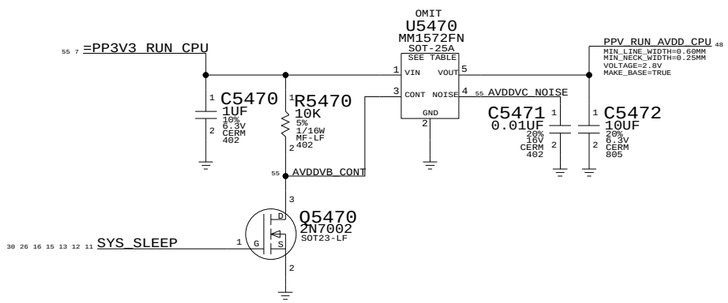
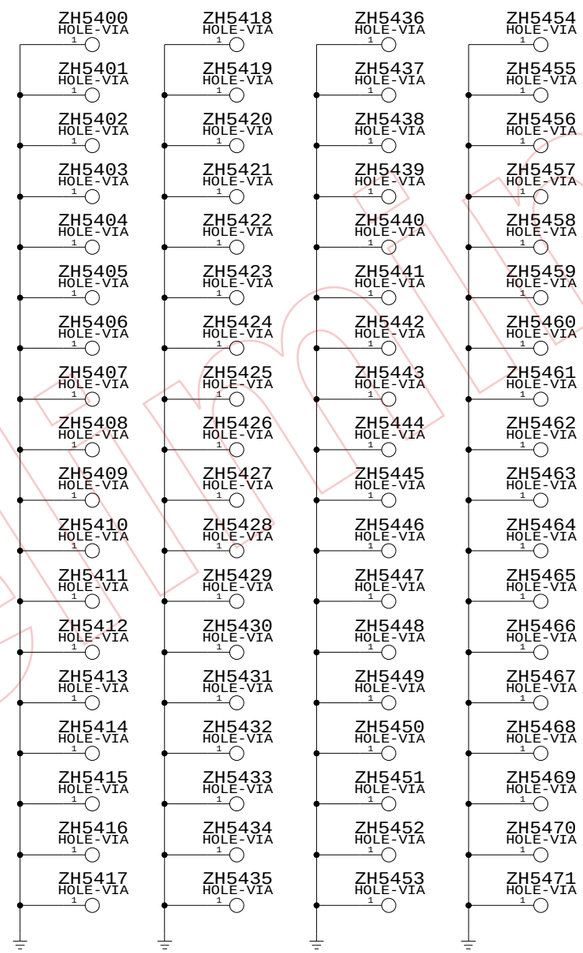
PROCESSOR AVDD VREG



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0671	1	IIC,MM1572FN,2.5V,150MA,REG,5P SOT-25A	U5470	AVDD_2V5
353S0807	1	IIC,MM1572,2.8V,150MA,REG,5P SOT-25A	U5470	AVDD_2V8



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CPU AVDD VREG

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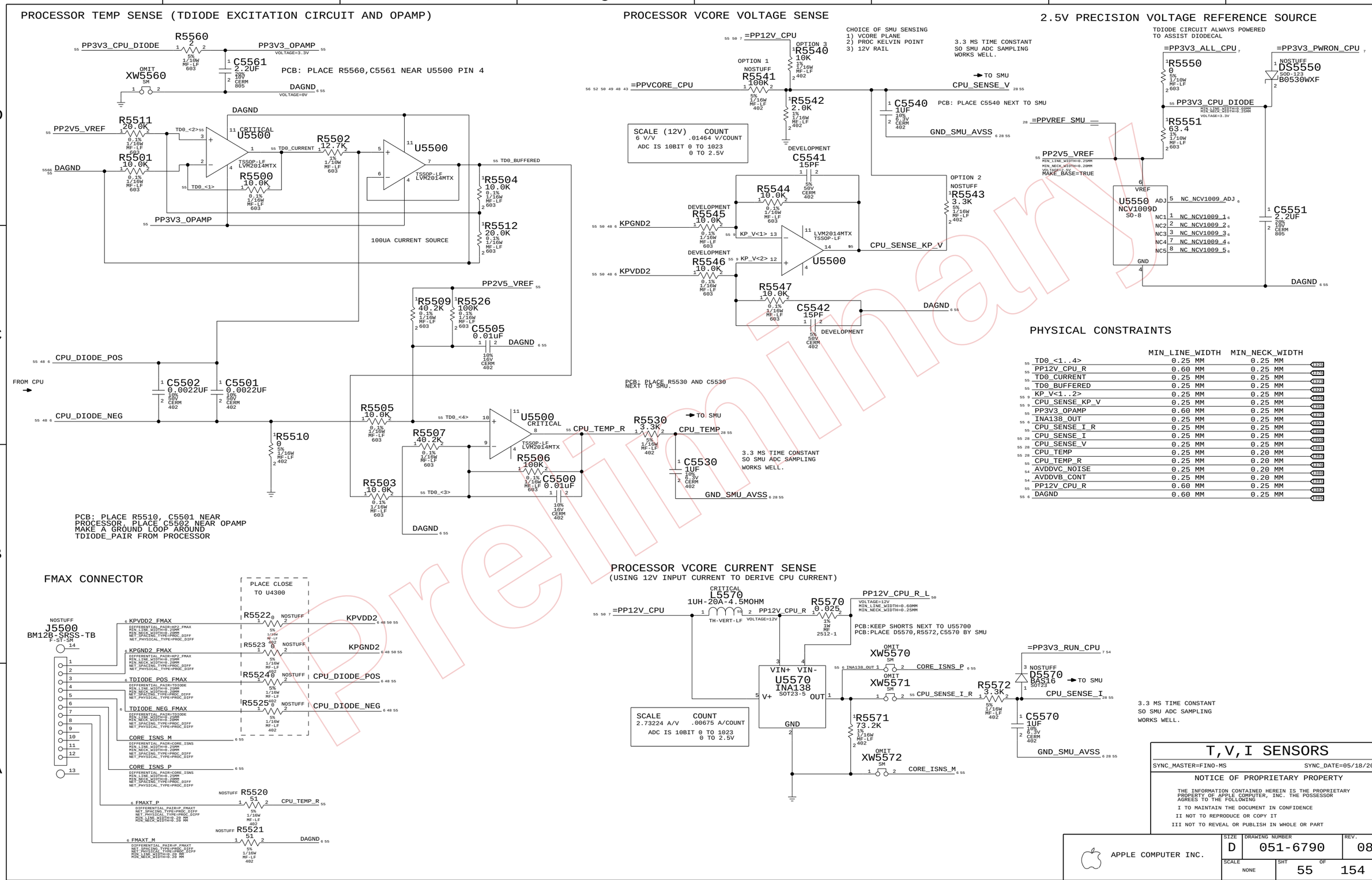
PROCESSOR TEMP SENSE (TDIODE EXCITATION CIRCUIT AND OPAMP)
PCB: PLACE R5560,C5561 NEAR U5500 PIN 4
PCB: PLACE R5510, C5501 NEAR PROCESSOR. PLACE C5502 NEAR OPAMP MAKE A GROUND LOOP AROUND TDIODE_PAIR FROM PROCESSOR
100UA CURRENT SOURCE
PROCESSOR VCORE VOLTAGE SENSE
CHOICE OF SMU SENSING
1) VCORE PLANE
2) PROC KELVIN POINT
3) 12V RAIL
3.3 MS TIME CONSTANT SO SMU ADC SAMPLING WORKS WELL.
PCB: PLACE C5540 NEXT TO SMU
SCALE (12V) COUNT
6 V/V .01464 V/COUNT
ADC IS 10BIT 0 TO 1023
0 TO 2.5V
2.5V PRECISION VOLTAGE REFERENCE SOURCE
TDIODE CIRCUIT ALWAYS POWERED TO ASSIST DIODECAL
PCB: PLACE R5530 AND C5530 NEXT TO SMU.
3.3 MS TIME CONSTANT SO SMU ADC SAMPLING WORKS WELL.
PHYSICAL CONSTRAINTS
MIN_LINE_WIDTH MIN_NECK_WIDTH
TD0_<1..4> 0.25 MM 0.25 MM
PP12V_CPU_R 0.60 MM 0.25 MM
TD0_CURRENT 0.25 MM 0.25 MM
TD0_BUFFERED 0.25 MM 0.25 MM
KP_V<1..2> 0.25 MM 0.25 MM
CPU_SENSE_KP_V 0.25 MM 0.25 MM
PP3V3_OPAMP 0.60 MM 0.25 MM
INA138_OUT 0.25 MM 0.25 MM
CPU_SENSE_I_R 0.25 MM 0.25 MM
CPU_SENSE_I 0.25 MM 0.25 MM
CPU_SENSE_V 0.25 MM 0.25 MM
CPU_TEMP 0.25 MM 0.20 MM
CPU_TEMP_R 0.25 MM 0.20 MM
AVDDVC_NOISE 0.25 MM 0.20 MM
AVDDVB_CONT 0.25 MM 0.20 MM
PP12V_CPU_R 0.60 MM 0.25 MM
DAGND 0.60 MM 0.25 MM
FMAX CONNECTOR
PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)
PCB:KEEP SHORTS NEXT TO U55700
PCB:PLACE D5570,R5572,C5570 BY SMU
SCALE COUNT
2.73224 A/V .00675 A/COUNT
ADC IS 10BIT 0 TO 1023
0 TO 2.5V
T,V,I SENSORS
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CONNECT PULSAR CLKS TO CPU/NB

56 43	EI_CPU_SYSCLK_P	MAKE_BASE=TRUE	EI_CPU_A_SYSCLK_P 26
56 43	EI_CPU_SYSCLK_N	MAKE_BASE=TRUE	EI_CPU_A_SYSCLK_N 26
56 43	EI_CPU_APSYNC	MAKE_BASE=TRUE	CPU_A_APSYNC 26
43	EI_CPU_TBEN_CLK	MAKE_BASE=TRUE	CPU_A_TBEN_CLK_US 26
56	EI_NB_APSYNC	MAKE_BASE=TRUE	NB_APSYNC 26 42

CONNECT KODIAK EI A TO/FROM CPU

56 43 9	EI_NB_TO_CPU_CLK_P		EI_NB_TO_CPU_A_CLK_P 42
56 43 9	EI_NB_TO_CPU_CLK_N	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_CLK_N 42
56 43	EI_NB_TO_CPU_AD<0..43>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_AD<0..43> 42
56 43 9	EI_NB_TO_CPU_SR_P<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_SR_P<0..1> 42
56 43 9	EI_NB_TO_CPU_SR_N<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_SR_N<0..1> 42
56 43 9	EI_CPU_TO_NB_CLK_P		EI_CPU_A_TO_NB_CLK_P 42
56 43 9	EI_CPU_TO_NB_CLK_N	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_CLK_N 42
56 43	EI_CPU_TO_NB_AD<0..43>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_AD<0..43> 42
56 43 9	EI_CPU_TO_NB_SR_P<0..1>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_SR_P<0..1> 42
56 43 9	EI_CPU_TO_NB_SR_N<0..1>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_SR_N<0..1> 42

CONNECT CPU TO KODIAK QREQ A0

43	CPU_TO_NB_QREQ_L	MAKE_BASE=TRUE	CPU_A0_TO_NB_QREQ_L 42

CONNECT CPU TO KODIAK QACK A0, NC OTHERWISE

43	CPU_QACK_L		CPU_A0_QACK_L 42
6	NC_CPU_A1_QACK_L	MAKE_BASE=TRUE	CPU_A1_QACK_L 42
6	NC_CPU_B0_QACK_L	MAKE_BASE=TRUE	CPU_B0_QACK_L 44
6	NC_CPU_B1_QACK_L	MAKE_BASE=TRUE	CPU_B1_QACK_L 44

CONNECT CPU TO KODIAK/SHASTA INT A0, NC OTHERWISE

43	CPU_INT_L		CPU_A0_INT_R_L 24 56
6	NC_NB_CPU_A1_INT_L	MAKE_BASE=TRUE	NB_CPU_A1_INT_L 42
6	NC_NB_CPU_B0_INT_L	MAKE_BASE=TRUE	NB_CPU_B0_INT_L 44
6	NC_NB_CPU_B1_INT_L	MAKE_BASE=TRUE	NB_CPU_B1_INT_L 44

CONNECT CPU TO SHASTA SRESET A0, NC OTHERWISE

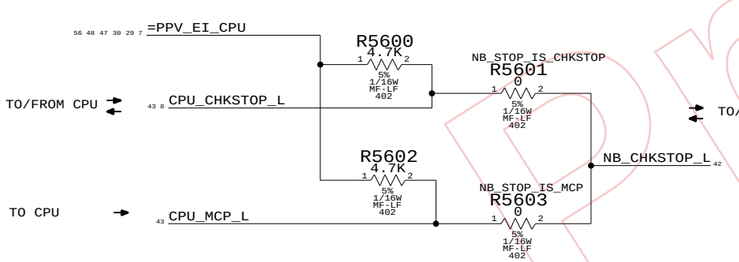
	CPU_SRESET_L_R		SB_CPU_A0_SRESET_L 24 56
	NOTUSED_CPU_A1_SRESET_L	MAKE_BASE=TRUE	SB_CPU_A1_SRESET_L 24 56
	NOTUSED_CPU_B0_SRESET_L	MAKE_BASE=TRUE	SB_CPU_B0_SRESET_L 24 56
	NOTUSED_CPU_B1_SRESET_L	MAKE_BASE=TRUE	SB_CPU_B1_SRESET_L 24 56

WIRE OUT KODIAK AND CPU SIGNALS FOR TP'S

9	TP_NB_B_TRIGGER_OUT		NB_B_TRIGGER_OUT 44
9	TP_NB_A_TRIGGER_OUT	MAKE_BASE=TRUE	NB_A_TRIGGER_OUT 42
	TP_CPU_APSYNCOUT	MAKE_BASE=TRUE	CPU_APSYNCOUT 43
	TP_CPU_TRIGGER_IN	MAKE_BASE=TRUE	CPU_TRIGGER_IN 43 47
	TP_CPU_TRIGGER_OUT	MAKE_BASE=TRUE	CPU_TRIGGER_OUT 43
9	NC_PSRO	MAKE_BASE=TRUE	CPU_PSRO 43
9	NC_PSRO_ENABLE	MAKE_BASE=TRUE	CPU_PSRO_ENABLE 43
	TP_CPU_ATTENTION	MAKE_BASE=TRUE	CPU_ATTENTION 43
9	NC_CPU_AFN	MAKE_BASE=TRUE	CPU_AFN 43

REMEMBER TO UPDATE NO_TEST PROPERTIES ON PG 6

CPU CHKSTOP OR MCP TO NB



EI BUS AND SYSCLK CONSTRAINT LABELS

		ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
56 43 9	EI_CPU_TO_NB_CLK_P	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	128
56 43 9	EI_CPU_TO_NB_CLK_N	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	127
56 43	EI_CPU_TO_NB_AD<0..21>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		131
56 43 9	EI_CPU_TO_NB_SR_P<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		134
56 43 9	EI_CPU_TO_NB_SR_N<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		132
56 43 9	EI_NB_TO_CPU_CLK_P	EINCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	
56 43 9	EI_NB_TO_CPU_CLK_N	EINCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	129
56 43	EI_NB_TO_CPU_AD<0..43>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		138
56 43 9	EI_NB_TO_CPU_SR_P<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		135
56 43 9	EI_NB_TO_CPU_SR_N<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		136
						137
56	EI_NB_APSYNC	EIPNAPSYNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		
56 43	EI_CPU_APSYNC	EIPCAPSYNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		139
56 43	EI_CPU_SYSCLK_P	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	138
56 43	EI_CPU_SYSCLK_N	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	140
42 26	EI_NB_SYSCLK_P	EIPNSYSCLK_P	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	141
42 26	EI_NB_SYSCLK_N	EIPNSYSCLK_N	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	139
56 43	EI_CPU_TO_NB_AD<22>	EICNCAD_PP	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		142
						140
56 43	EI_CPU_TO_NB_AD<23..43>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		
						140

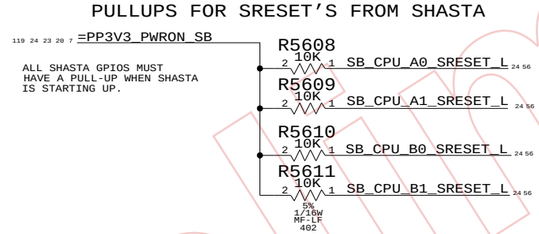
NC KODIAK EI B OUTPUT PORT

6	NC_EI_NB_TO_CPU_B_CLK_P		EI_NB_TO_CPU_B_CLK_P
6	NC_EI_NB_TO_CPU_B_CLK_N	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_CLK_N 44
6	NC_EI_NB_TO_CPU_B_AD<0..43>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_AD<0..43> 44
6	NC_EI_NB_TO_CPU_B_SR_P<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_SR_P<0..1> 44
6	NC_EI_NB_TO_CPU_B_SR_N<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_SR_N<0..1> 44
		MAKE_BASE=TRUE	

NC KODIAK EI B INPUT PORT

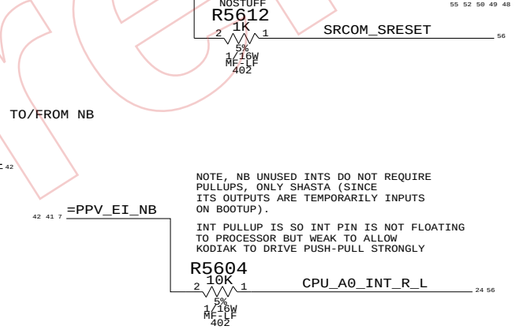
6	NC_EI_CPU_B_TO_NB_CLK_P		EI_CPU_B_TO_NB_CLK_P 44
6	NC_EI_CPU_B_TO_NB_CLK_N	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_CLK_N 44
6	NC_EI_CPU_B_TO_NB_AD<0..43>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_AD<0..43> 44
6	NC_EI_CPU_B_TO_NB_SR_P<0..1>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_SR_P<0..1> 44
6	NC_EI_CPU_B_TO_NB_SR_N<0..1>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_SR_N<0..1> 44
		MAKE_BASE=TRUE	

PULLUPS FOR SRESET'S FROM SHASTA



ALL SHASTA GPIOS MUST HAVE A PULL-UP WHEN SHASTA IS STARTING UP.

IF SHASTA SHOULD DRIVE OD WITH EI LEVEL PULLUP, STUFF R5612, NOSTUFF R5608, STUFF R5646

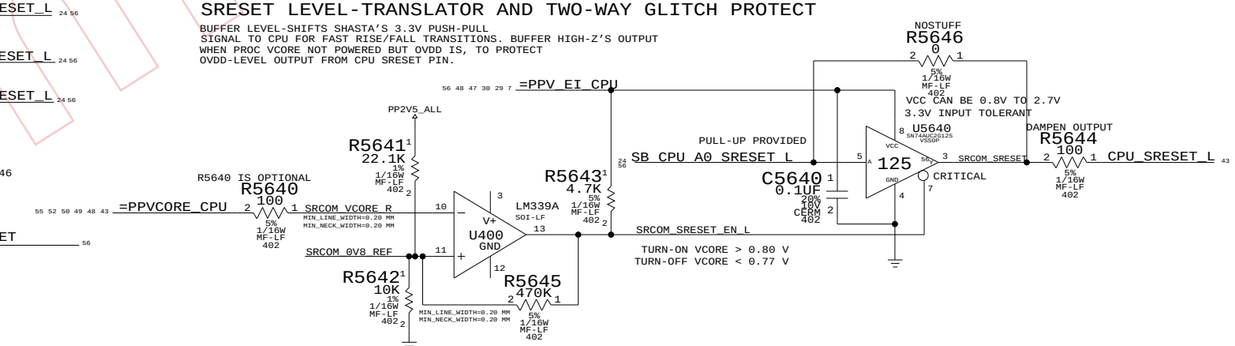


NOTE, NB UNUSED INTS DO NOT REQUIRE PULLUPS, ONLY SHASTA (SINCE ITS OUTPUTS ARE TEMPORARILY INPUTS ON BOOTUP).

INT PULLUP IS SO INT PIN IS NOT FLOATING TO PROCESSOR BUT WEAK TO ALLOW KODIAK TO DRIVE PUSH-PULL STRONGLY

SRESET LEVEL-TRANSLATOR AND TWO-WAY GLITCH PROTECT

BUFFER LEVEL-SHIFTS SHASTA'S 3.3V PUSH-PULL SIGNAL TO CPU FOR FAST RISE/FALL TRANSITIONS. BUFFER HIGH-Z'S OUTPUT WHEN PROC VCORE NOT POWERED BUT OVDD IS, TO PROTECT OVDD-LEVEL OUTPUT FROM CPU SRESET PIN.



CPU ALIASES & MISC

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D	051-6790	08
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Preliminary

Q63: SEE P.20 FOR MORE DECOUPLING CAPS FOR THESE PINS.

Preliminary

KODIAC NBMEM PWR & CAPS

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

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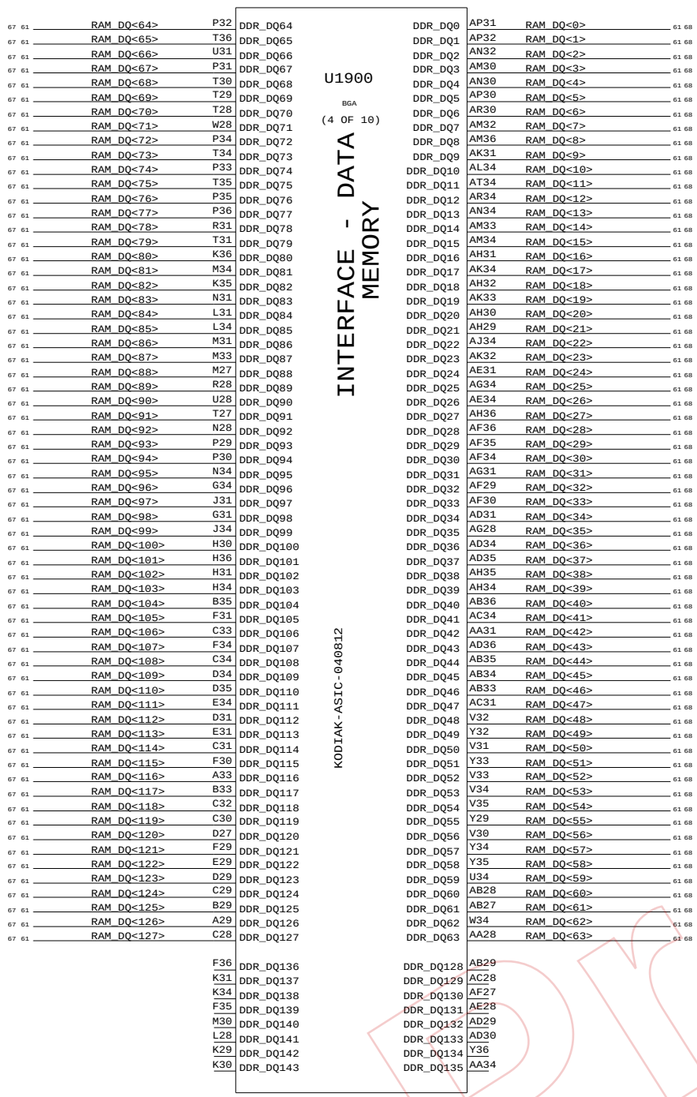
D	051-6790	08

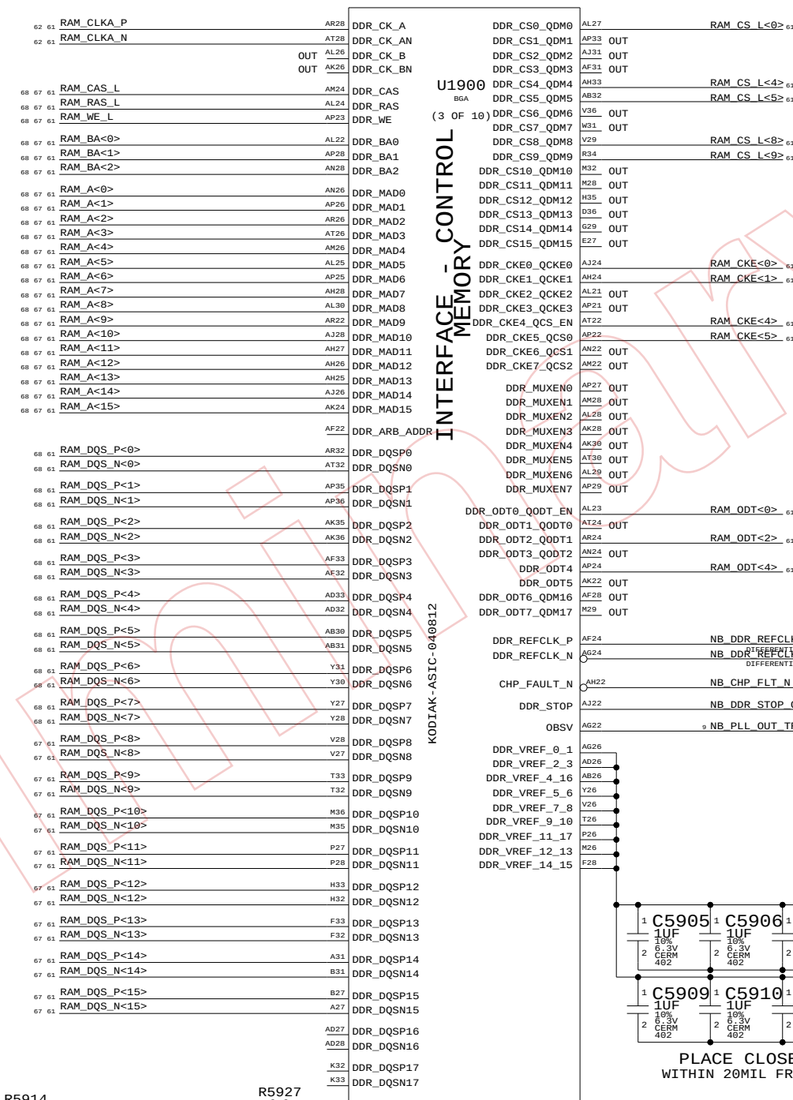
SCALE NONE SHT 58 OF 154

LAST_MODIFIED=Thu May 19 14:09:19 2005

DRAWING



DQ/DQS OKAY TO TIE TO GROUND FOR THERMALS

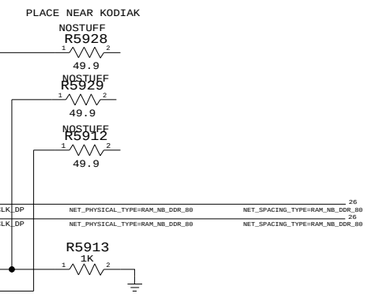


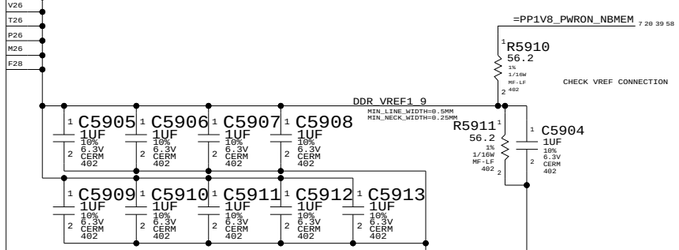
Kodiak 128bit CS/CKE/ODT mapping (Q63 style)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	-	*unused*	0:63
B2	0	0	4	J6700 rank 1	64:127
B3	1	1	-	J6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	3	-	*unused*	0:63
D6	10	3	5	*unused*	64:127
D7	11	3	-	*unused*	64:127
E8	4	4	2	*unused*	0:63
E9	5	5	-	*unused*	0:63
F10	12	4	6	*unused*	64:127
F11	13	5	-	*unused*	64:127
G12	6	6	3	*unused*	0:63
G13	7	7	-	*unused*	0:63
H14	14	6	7	*unused*	64:127
H15	15	7	-	*unused*	64:127

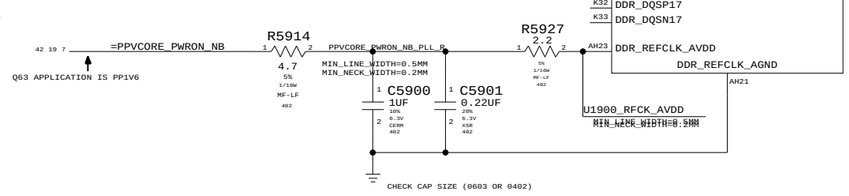
Kodiak 128bit CS/CKE/ODT mapping (v1.1 only)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	-	*unused*	0:63
B2	4	4	2	J6700 rank 1	64:127
B3	5	5	-	J6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	3	-	*unused*	0:63
D6	6	6	3	*unused*	64:127
D7	7	7	-	*unused*	64:127





PLACE CLOSE TO KODIAK PIN
WITHIN 20MIL FROM VIA FOR EACH VREF



Kodiak Memory Dq/Ctl

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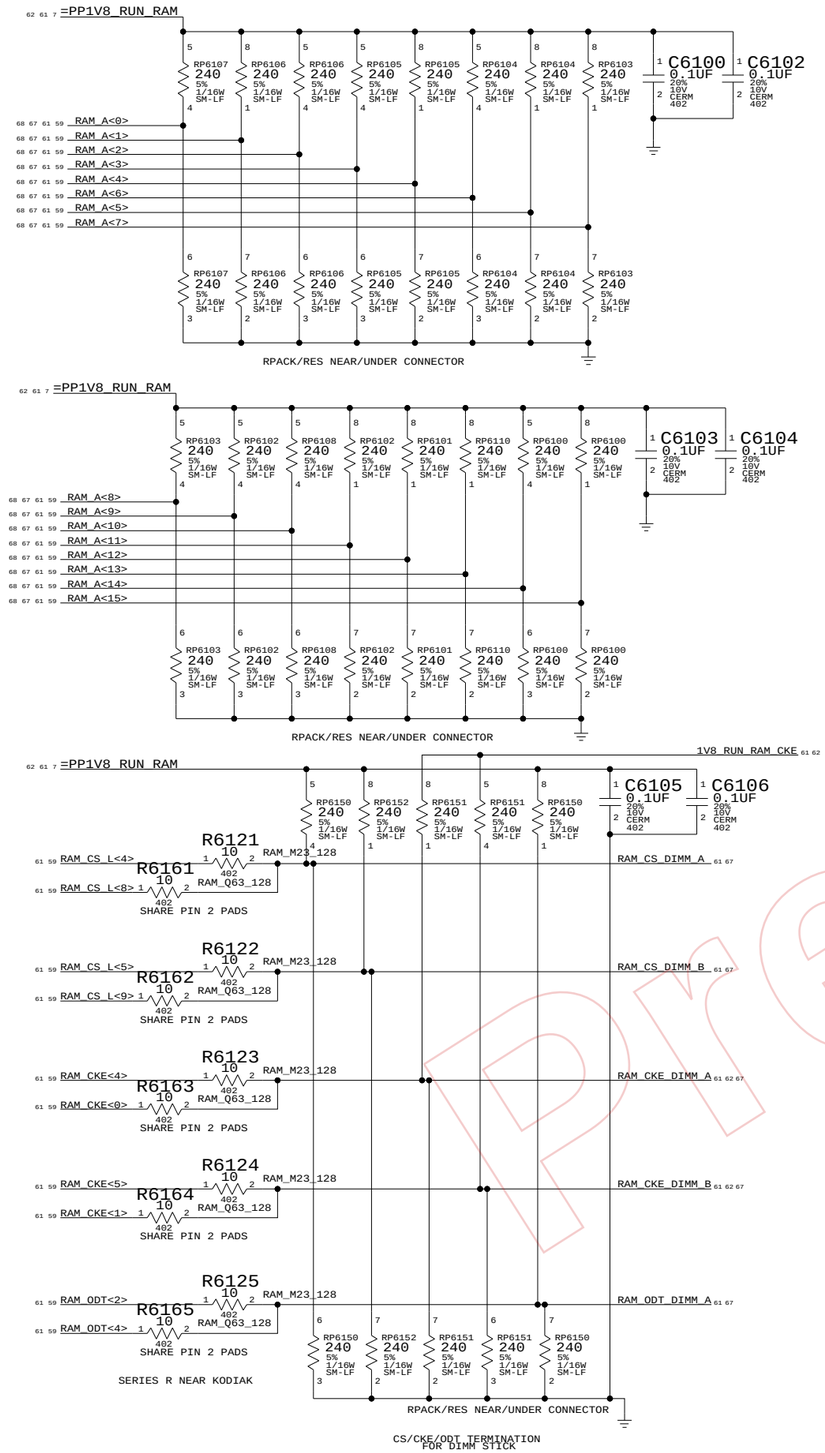
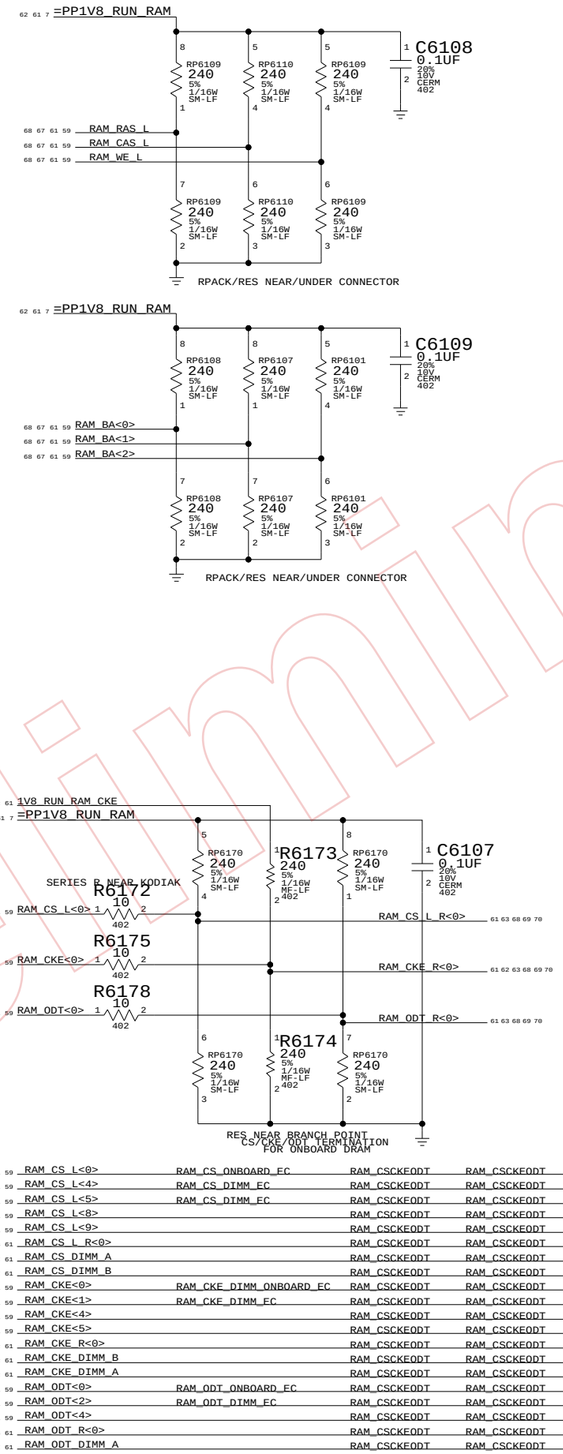
D	051-6790	08
SCALE NONE	SHT 59 OF 154	

KODIAK MEMORY INTERFACE

Preliminary

ALL R PACKS ARE 1/16W 5%





		ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
62 59	RAM_CLKA_P	RAM_KODIAK_CLK_EC	RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP	2206
62 59	RAM_CLKA_N		RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP	2207
67 62	RAM_DIMM_A_CLK_P0	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK0_DP	2210
67 62	RAM_DIMM_A_CLK_N0	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK0_DP	2211
67 62	RAM_DIMM_A_CLK_P1	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK1_DP	2212
67 62	RAM_DIMM_A_CLK_N1	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK1_DP	2213
67 62	RAM_DIMM_A_CLK_P2	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK2_DP	2214
67 62	RAM_DIMM_A_CLK_N2	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK2_DP	2215
69 62	RAM_ONBOARD_CLK_P0_1	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK0_DP	2216
69 62	RAM_ONBOARD_CLK_N0_1	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK0_DP	2217
69 62	RAM_ONBOARD_CLK_P2_3	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK2_DP	2218
69 62	RAM_ONBOARD_CLK_N2_3	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK2_DP	2219
70 62	RAM_ONBOARD_CLK_P4_5	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK4_DP	2220
70 62	RAM_ONBOARD_CLK_N4_5	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK4_DP	2221
70 62	RAM_ONBOARD_CLK_P6_7	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK6_DP	2222
70 62	RAM_ONBOARD_CLK_N6_7	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK6_DP	2223
62	RAM_CLK_FBIN_P	RAM_FB_CLK_EC	RAM_CLK	RAM_CLK	RAM_FBIN_CLK_DP	2224
62	RAM_CLK_FBIN_N		RAM_CLK	RAM_CLK	RAM_FBIN_CLK_DP	2225
62	RAM_CLK_FBOUT_P		RAM_CLK	RAM_CLK	RAM_FBOUT_CLK_DP	2226
62	RAM_CLK_FBOUT_N		RAM_CLK	RAM_CLK	RAM_FBOUT_CLK_DP	2227
68 59	RAM_DQ<7..0>	RAM_DQS0_EC	RAM_CAD	RAM_CAD		2248
68 59	RAM_DQS_P<0>	RAM_DQS0_EC	RAM_DQS	RAM_DQS	RAM_DQS_0_DP	2249
68 59	RAM_DQS_N<0>	RAM_DQS0_EC	RAM_DQS	RAM_DQS	RAM_DQS_0_DP	4470
68 59	RAM_DQ<15..8>	RAM_DQS1_EC	RAM_CAD	RAM_CAD		2252
68 59	RAM_DQS_P<1>	RAM_DQS1_EC	RAM_DQS	RAM_DQS	RAM_DQS_1_DP	2251
68 59	RAM_DQS_N<1>	RAM_DQS1_EC	RAM_DQS	RAM_DQS	RAM_DQS_1_DP	4471
68 59	RAM_DQ<23..16>	RAM_DQS2_EC	RAM_CAD	RAM_CAD		2254
68 59	RAM_DQS_P<2>	RAM_DQS2_EC	RAM_DQS	RAM_DQS	RAM_DQS_2_DP	2253
68 59	RAM_DQS_N<2>	RAM_DQS2_EC	RAM_DQS	RAM_DQS	RAM_DQS_2_DP	4472
68 59	RAM_DQ<31..24>	RAM_DQS3_EC	RAM_CAD	RAM_CAD		2256
68 59	RAM_DQS_P<3>	RAM_DQS3_EC	RAM_DQS	RAM_DQS	RAM_DQS_3_DP	2255
68 59	RAM_DQS_N<3>	RAM_DQS3_EC	RAM_DQS	RAM_DQS	RAM_DQS_3_DP	4473
68 59	RAM_DQ<39..32>	RAM_DQS4_EC	RAM_CAD	RAM_CAD		2258
68 59	RAM_DQS_P<4>	RAM_DQS4_EC	RAM_DQS	RAM_DQS	RAM_DQS_4_DP	2257
68 59	RAM_DQS_N<4>	RAM_DQS4_EC	RAM_DQS	RAM_DQS	RAM_DQS_4_DP	4474
68 59	RAM_DQ<47..40>	RAM_DQS5_EC	RAM_CAD	RAM_CAD		2260
68 59	RAM_DQS_P<5>	RAM_DQS5_EC	RAM_DQS	RAM_DQS	RAM_DQS_5_DP	2259
68 59	RAM_DQS_N<5>	RAM_DQS5_EC	RAM_DQS	RAM_DQS	RAM_DQS_5_DP	4475
68 59	RAM_DQ<55..48>	RAM_DQS6_EC	RAM_CAD	RAM_CAD		2262
68 59	RAM_DQS_P<6>	RAM_DQS6_EC	RAM_DQS	RAM_DQS	RAM_DQS_6_DP	2261
68 59	RAM_DQS_N<6>	RAM_DQS6_EC	RAM_DQS	RAM_DQS	RAM_DQS_6_DP	4476
68 59	RAM_DQ<63..56>	RAM_DQS7_EC	RAM_CAD	RAM_CAD		2264
68 59	RAM_DQS_P<7>	RAM_DQS7_EC	RAM_DQS	RAM_DQS	RAM_DQS_7_DP	2263
68 59	RAM_DQS_N<7>	RAM_DQS7_EC	RAM_DQS	RAM_DQS	RAM_DQS_7_DP	4477
67 59	RAM_DQ<71..64>	RAM_DQS8_EC	RAM_CAD	RAM_CAD		2267
67 59	RAM_DQS_P<8>	RAM_DQS8_EC	RAM_DQS	RAM_DQS	RAM_DQS_8_DP	2266
67 59	RAM_DQS_N<8>	RAM_DQS8_EC	RAM_DQS	RAM_DQS	RAM_DQS_8_DP	4478
67 59	RAM_DQ<79..72>	RAM_DQS9_EC	RAM_CAD	RAM_CAD		2268
67 59	RAM_DQS_P<9>	RAM_DQS9_EC	RAM_DQS	RAM_DQS	RAM_DQS_9_DP	2269
67 59	RAM_DQS_N<9>	RAM_DQS9_EC	RAM_DQS	RAM_DQS	RAM_DQS_9_DP	4479
67 59	RAM_DQ<87..80>	RAM_DQS10_EC	RAM_CAD	RAM_CAD		2269
67 59	RAM_DQS_P<10>	RAM_DQS10_EC	RAM_DQS	RAM_DQS	RAM_DQS_10_DP	2270
67 59	RAM_DQS_N<10>	RAM_DQS10_EC	RAM_DQS	RAM_DQS	RAM_DQS_10_DP	4480
67 59	RAM_DQ<95..88>	RAM_DQS11_EC	RAM_CAD	RAM_CAD		2271
67 59	RAM_DQS_P<11>	RAM_DQS11_EC	RAM_DQS	RAM_DQS	RAM_DQS_11_DP	2272
67 59	RAM_DQS_N<11>	RAM_DQS11_EC	RAM_DQS	RAM_DQS	RAM_DQS_11_DP	4481
67 59	RAM_DQ<103..96>	RAM_DQS12_EC	RAM_CAD	RAM_CAD		2275
67 59	RAM_DQS_P<12>	RAM_DQS12_EC	RAM_DQS	RAM_DQS	RAM_DQS_12_DP	2274
67 59	RAM_DQS_N<12>	RAM_DQS12_EC	RAM_DQS	RAM_DQS	RAM_DQS_12_DP	4482
67 59	RAM_DQ<111..104>	RAM_DQS13_EC	RAM_CAD	RAM_CAD		2277
67 59	RAM_DQS_P<13>	RAM_DQS13_EC	RAM_DQS	RAM_DQS	RAM_DQS_13_DP	2276
67 59	RAM_DQS_N<13>	RAM_DQS13_EC	RAM_DQS	RAM_DQS	RAM_DQS_13_DP	4483
67 59	RAM_DQ<119..112>	RAM_DQS14_EC	RAM_CAD	RAM_CAD		2278
67 59	RAM_DQS_P<14>	RAM_DQS14_EC	RAM_DQS	RAM_DQS	RAM_DQS_14_DP	2279
67 59	RAM_DQS_N<14>	RAM_DQS14_EC	RAM_DQS	RAM_DQS	RAM_DQS_14_DP	4484
67 59	RAM_DQ<127..120>	RAM_DQS15_EC	RAM_CAD	RAM_CAD		2280
67 59	RAM_DQS_P<15>	RAM_DQS15_EC	RAM_DQS	RAM_DQS	RAM_DQS_15_DP	2281
67 59	RAM_DQS_N<15>	RAM_DQS15_EC	RAM_DQS	RAM_DQS	RAM_DQS_15_DP	4485
70 69 68 6	RAM_DQ_R<127..0>		RAM_CAD	RAM_CAD		2354
70 69 68	RAM_DQS_P_R<15..0>		RAM_DQS	RAM_DQS		4356
70 69 68	RAM_DQS_N_R<15..0>		RAM_DQS	RAM_DQS		4486
68 67 61 59	RAM_A<15..14>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		2572
68 67 61 59	RAM_A<13..0>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		2298
68 67 61 59	RAM_BA<1..0>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		2298
68 67 61 59	RAM_BA<2>	RAM_A_CTL_1_EC	RAM_CAD	RAM_CAD		2573
68 67 61 59	RAM_RAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		2297
68 67 61 59	RAM_CAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		2688
68 67 61 59	RAM_WE_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		2299
70 69 68 63	RAM_A_R<15..0>		RAM_CAD	RAM_CAD		4386
70 69 68 63	RAM_BA_R<2..0>		RAM_CAD	RAM_CAD		4384
70 69 68 63	RAM_RAS_L_R		RAM_CAD	RAM_CAD		4383
70 69 68 63	RAM_CAS_L_R		RAM_CAD	RAM_CAD		4382
70 69 68 63	RAM_WE_L_R		RAM_CAD	RAM_CAD		4381

61 59	RAM_CS_L<0>	RAM_CS_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT	2243
61 59	RAM_CS_L<4>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT	4487
61 59	RAM_CS_L<5>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT	2242
61 59	RAM_CS_L<8>		RAM_CSCKEODT	RAM_CSCKEODT	2240
61 59	RAM_CS_L<9>		RAM_CSCKEODT	RAM_CSCKEODT	2244
70 69 68 63 61	RAM_CS_L_R<0>		RAM_CSCKEODT	RAM_CSCKEODT	2238
67 61	RAM_CS_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT	2241
67 61	RAM_CS_DIMM_B		RAM_CSCKEODT	RAM_CSCKEODT	4575
61 59	RAM_CKE<0>	RAM_CKE_DIMM_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT	2234
61 59	RAM_CKE<1>	RAM_CKE_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT	2236
61 59	RAM_CKE<4>		RAM_CSCKEODT	RAM_CSCKEODT	2235
61 59	RAM_CKE<5>		RAM_CSCKEODT	RAM_CSCKEODT	2237
70 69 68 63 62 61	RAM_CKE_R<0>		RAM_CSCKEODT	RAM_CSCKEODT	2236
67 62 61	RAM_CKE_DIMM_B		RAM_CSCKEODT	RAM_CSCKEODT	4592
67 62 61	RAM_CKE_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT	2232
61 59	RAM_ODT<0>	RAM_ODT_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT	4574
61 59	RAM_ODT<2>	RAM_ODT_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT	4576
61 59	RAM_ODT<4>		RAM_CSCKEODT	RAM_CSCKEODT	4577
70 69 68 63 61	RAM_ODT_R<0>		RAM_CSCKEODT	RAM_CSCKEODT	4593
67 61	RAM_ODT_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT	4594

RAM_CLK PRIMARY SPACING SET BASED ON DIFF IMPEDANCE
RAM_CLK LINE-LINE SPACING SET TO 15MIL
TOTAL LENGTH TOLERENCE = 20PS = 2.82MM

RAM_CAD SPACING IS 10MIL

Parallel Term

SYNC_MASTER=FINO-RT SYNC_DATE=05/18/2005

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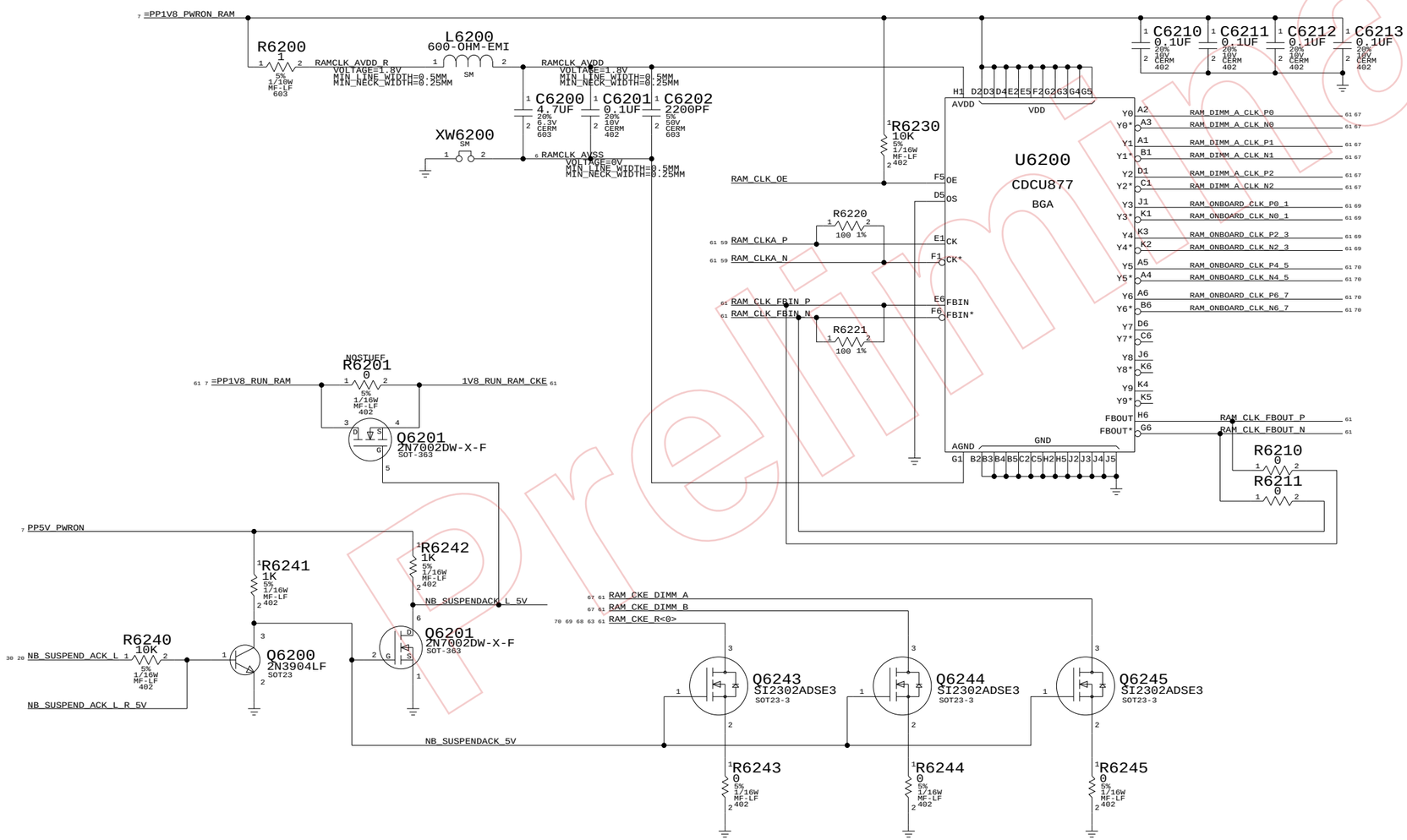
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 61 OF 154	

Preliminary



Preliminary

Main Memory Clock Buffer

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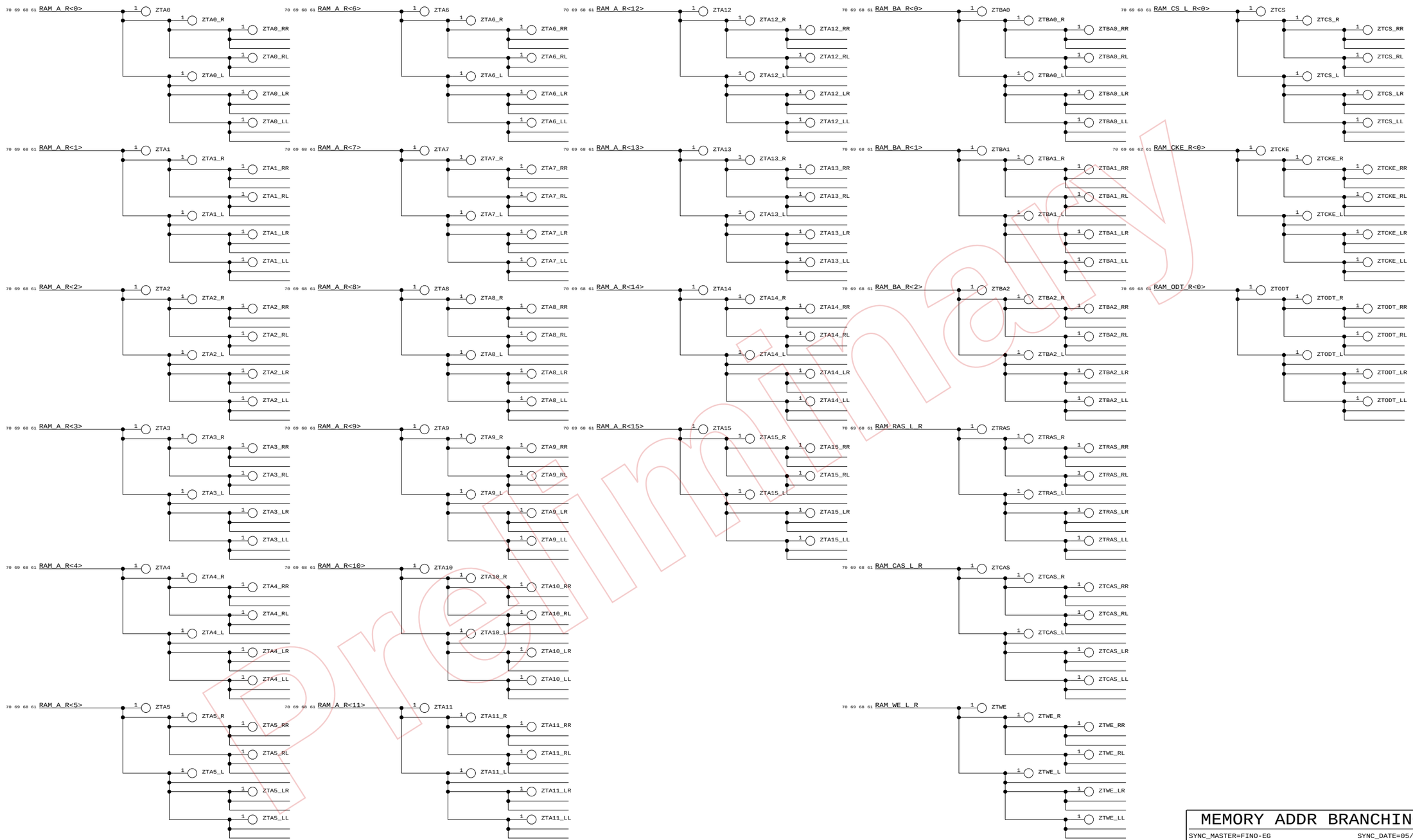

MEMORY ADDR BRANCHING

SYNC_MASTER=FINO-EG SYNC_DATE=05/18/2005

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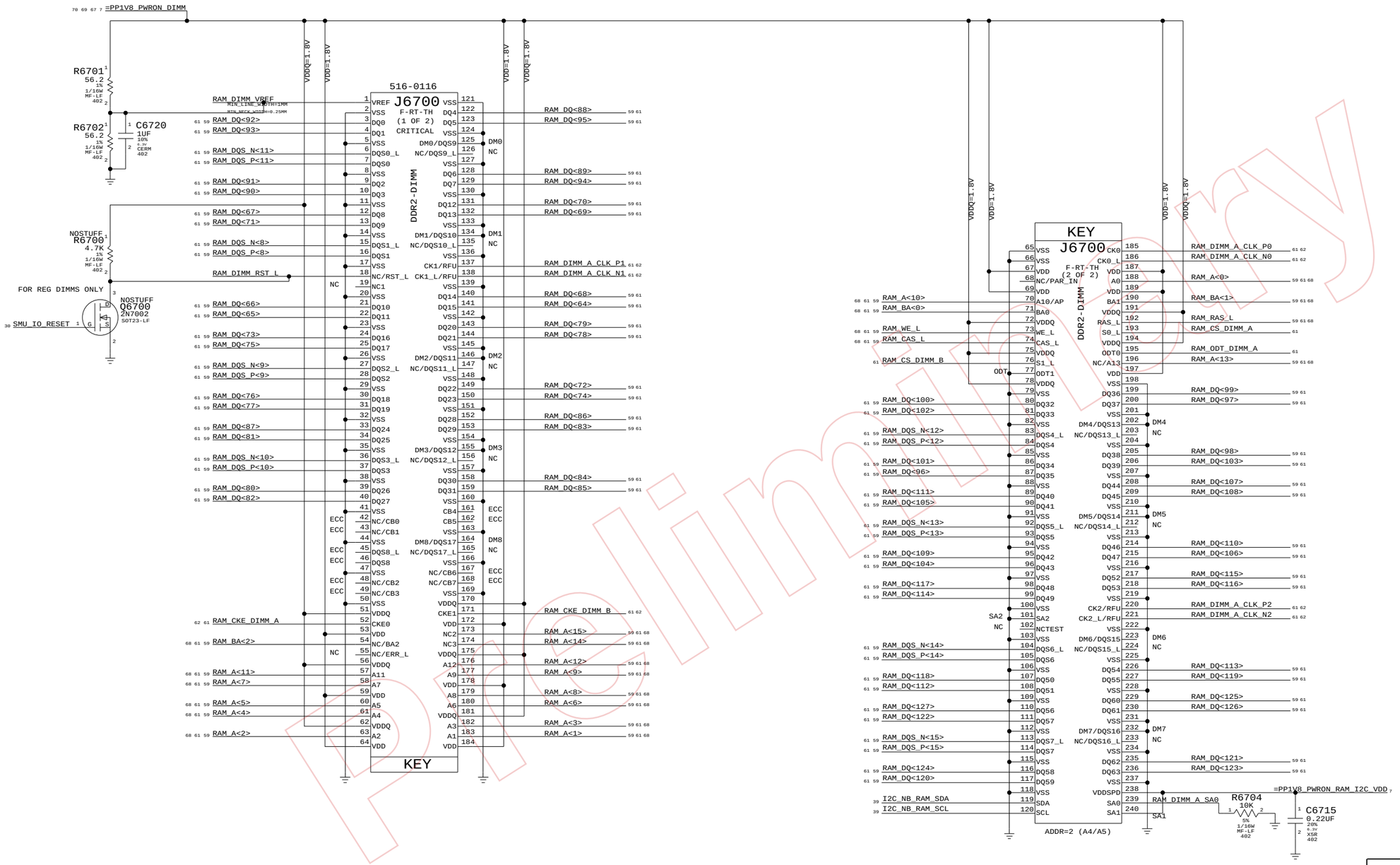
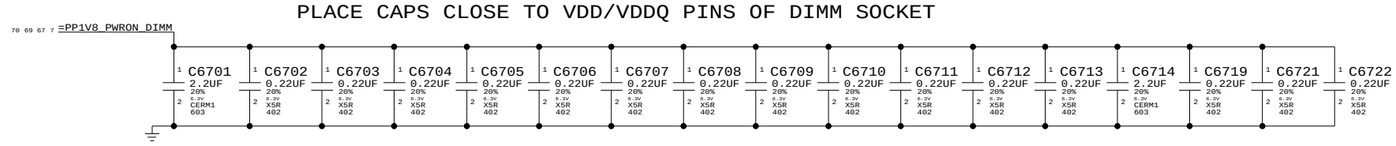
D	051-6790	08
SCALE NONE	SHT 63 OF 154	

Preliminary



PLACE CAPS CLOSE TO VDD/VDDQ PINS OF DIMM SOCKET



Memory Dimm A

SYNC_MASTER=FINO-RT SYNC_DATE=05/18/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 67 OF 154	

ONBOARD MEMORY SHOULD FOLLOW SPEC FOR RAW CARD VERSION A

61 59	RAM_DQ<0>	22	4	5	RP6800	RAM_DQ_R<0>	61 69
61 59	RAM_DQ<1>	22	3	6	RP6800	RAM_DQ_R<1>	6 61 69
61 59	RAM_DQ<2>	22	1	8	RP6801	RAM_DQ_R<2>	6 61 69
61 59	RAM_DQ<3>	22	3	6	RP6801	RAM_DQ_R<3>	6 61 69
61 59	RAM_DQ<4>	22	4	5	RP6801	RAM_DQ_R<4>	61 69
61 59	RAM_DQ<5>	22	2	7	RP6800	RAM_DQ_R<5>	6 61 69
61 59	RAM_DQ<6>	22	2	7	RP6801	RAM_DQ_R<6>	6 61 69
61 59	RAM_DQ<7>	22	1	8	RP6800	RAM_DQ_R<7>	6 61 69
61 59	RAM_DQ<8>	22	3	6	RP6802	RAM_DQ_R<8>	6 61 69
61 59	RAM_DQ<9>	22	4	5	RP6803	RAM_DQ_R<9>	61 69
61 59	RAM_DQ<10>	22	1	8	RP6803	RAM_DQ_R<10>	6 61 69
61 59	RAM_DQ<11>	22	4	5	RP6802	RAM_DQ_R<11>	6 61 69
61 59	RAM_DQ<12>	22	3	6	RP6803	RAM_DQ_R<12>	6 61 69
61 59	RAM_DQ<13>	22	2	7	RP6802	RAM_DQ_R<13>	6 61 69
61 59	RAM_DQ<14>	22	2	7	RP6803	RAM_DQ_R<14>	6 61 69
61 59	RAM_DQ<15>	22	1	8	RP6802	RAM_DQ_R<15>	61 69
61 59	RAM_DQ<16>	22	3	6	RP6805	RAM_DQ_R<16>	6 61 69
61 59	RAM_DQ<17>	22	4	5	RP6805	RAM_DQ_R<17>	6 61 69
61 59	RAM_DQ<18>	22	1	8	RP6804	RAM_DQ_R<18>	61 69
61 59	RAM_DQ<19>	22	2	7	RP6805	RAM_DQ_R<19>	6 61 69
61 59	RAM_DQ<20>	22	2	7	RP6804	RAM_DQ_R<20>	6 61 69
61 59	RAM_DQ<21>	22	4	5	RP6804	RAM_DQ_R<21>	6 61 69
61 59	RAM_DQ<22>	22	3	6	RP6804	RAM_DQ_R<22>	6 61 69
61 59	RAM_DQ<23>	22	1	8	RP6805	RAM_DQ_R<23>	61 69
61 59	RAM_DQ<24>	22	4	5	RP6807	RAM_DQ_R<24>	6 61 69
61 59	RAM_DQ<25>	22	2	7	RP6806	RAM_DQ_R<25>	6 61 69
61 59	RAM_DQ<26>	22	4	5	RP6806	RAM_DQ_R<26>	6 61 69
61 59	RAM_DQ<27>	22	1	8	RP6807	RAM_DQ_R<27>	61 69
61 59	RAM_DQ<28>	22	3	6	RP6807	RAM_DQ_R<28>	6 61 69
61 59	RAM_DQ<29>	22	3	6	RP6806	RAM_DQ_R<29>	6 61 69
61 59	RAM_DQ<30>	22	2	7	RP6807	RAM_DQ_R<30>	6 61 69
61 59	RAM_DQ<31>	22	1	8	RP6806	RAM_DQ_R<31>	61 69
61 59	RAM_DQ<32>	22	4	5	RP6809	RAM_DQ_R<32>	6 61 70
61 59	RAM_DQ<33>	22	2	7	RP6808	RAM_DQ_R<33>	6 61 70
61 59	RAM_DQ<34>	22	3	6	RP6808	RAM_DQ_R<34>	6 61 70
61 59	RAM_DQ<35>	22	1	8	RP6809	RAM_DQ_R<35>	61 70
61 59	RAM_DQ<36>	22	2	7	RP6809	RAM_DQ_R<36>	6 61 70
61 59	RAM_DQ<37>	22	1	8	RP6808	RAM_DQ_R<37>	61 70
61 59	RAM_DQ<38>	22	3	6	RP6809	RAM_DQ_R<38>	6 61 70
61 59	RAM_DQ<39>	22	4	5	RP6808	RAM_DQ_R<39>	6 61 70
61 59	RAM_DQ<40>	22	4	5	RP6810	RAM_DQ_R<40>	6 61 70
61 59	RAM_DQ<41>	22	3	6	RP6811	RAM_DQ_R<41>	6 61 70
61 59	RAM_DQ<42>	22	1	8	RP6811	RAM_DQ_R<42>	61 70
61 59	RAM_DQ<43>	22	2	7	RP6810	RAM_DQ_R<43>	6 61 70
61 59	RAM_DQ<44>	22	4	5	RP6811	RAM_DQ_R<44>	6 61 70
61 59	RAM_DQ<45>	22	3	6	RP6810	RAM_DQ_R<45>	6 61 70
61 59	RAM_DQ<46>	22	2	7	RP6811	RAM_DQ_R<46>	6 61 70
61 59	RAM_DQ<47>	22	1	8	RP6810	RAM_DQ_R<47>	61 70
61 59	RAM_DQ<48>	22	3	6	RP6812	RAM_DQ_R<48>	6 61 70
61 59	RAM_DQ<49>	22	4	5	RP6812	RAM_DQ_R<49>	6 61 70
61 59	RAM_DQ<50>	22	2	7	RP6813	RAM_DQ_R<50>	6 61 70
61 59	RAM_DQ<51>	22	1	8	RP6813	RAM_DQ_R<51>	61 70
61 59	RAM_DQ<52>	22	3	6	RP6813	RAM_DQ_R<52>	6 61 70
61 59	RAM_DQ<53>	22	4	5	RP6813	RAM_DQ_R<53>	6 61 70
61 59	RAM_DQ<54>	22	2	7	RP6812	RAM_DQ_R<54>	6 61 70
61 59	RAM_DQ<55>	22	1	8	RP6812	RAM_DQ_R<55>	61 70
61 59	RAM_DQ<56>	22	3	6	RP6814	RAM_DQ_R<56>	6 61 70
61 59	RAM_DQ<57>	22	4	5	RP6815	RAM_DQ_R<57>	6 61 70
61 59	RAM_DQ<58>	22	2	7	RP6815	RAM_DQ_R<58>	6 61 70
61 59	RAM_DQ<59>	22	3	6	RP6815	RAM_DQ_R<59>	6 61 70
61 59	RAM_DQ<60>	22	2	7	RP6814	RAM_DQ_R<60>	6 61 70
61 59	RAM_DQ<61>	22	1	8	RP6814	RAM_DQ_R<61>	61 70
61 59	RAM_DQ<62>	22	1	8	RP6815	RAM_DQ_R<62>	61 70
61 59	RAM_DQ<63>	22	4	5	RP6814	RAM_DQ_R<63>	6 61 70

61 59	RAM_DQS_P<0>	22	1	2	R6800	RAM_DQS_P_R<0>	61 69
61 59	RAM_DQS_N<0>	22	1	2	R6810	RAM_DQS_N_R<0>	61 69
61 59	RAM_DQS_P<1>	22	1	2	R6801	RAM_DQS_P_R<1>	61 69
61 59	RAM_DQS_N<1>	22	1	2	R6811	RAM_DQS_N_R<1>	61 69
61 59	RAM_DQS_P<2>	22	1	2	R6802	RAM_DQS_P_R<2>	61 69
61 59	RAM_DQS_N<2>	22	1	2	R6812	RAM_DQS_N_R<2>	61 69
61 59	RAM_DQS_P<3>	22	1	2	R6803	RAM_DQS_P_R<3>	61 69
61 59	RAM_DQS_N<3>	22	1	2	R6813	RAM_DQS_N_R<3>	61 69
61 59	RAM_DQS_P<4>	22	1	2	R6804	RAM_DQS_P_R<4>	61 70
61 59	RAM_DQS_N<4>	22	1	2	R6814	RAM_DQS_N_R<4>	61 70
61 59	RAM_DQS_P<5>	22	1	2	R6805	RAM_DQS_P_R<5>	61 70
61 59	RAM_DQS_N<5>	22	1	2	R6815	RAM_DQS_N_R<5>	61 70
61 59	RAM_DQS_P<6>	22	1	2	R6806	RAM_DQS_P_R<6>	61 70
61 59	RAM_DQS_N<6>	22	1	2	R6816	RAM_DQS_N_R<6>	61 70
61 59	RAM_DQS_P<7>	22	1	2	R6807	RAM_DQS_P_R<7>	61 70
61 59	RAM_DQS_N<7>	22	1	2	R6817	RAM_DQS_N_R<7>	61 70

67 61 59	RAM_A<0>	5.1	1	8	RP6824	RAM_A_R<0>	61 63 69 70	1 ZT6800
67 61 59	RAM_A<1>	5.1	1	8	RP6823	RAM_A_R<1>	61 63 69 70	1 ZT6801
67 61 59	RAM_A<2>	5.1	2	7	RP6823	RAM_A_R<2>	61 63 69 70	1 ZT6802
67 61 59	RAM_A<3>	5.1	4	5	RP6822	RAM_A_R<3>	61 63 69 70	1 ZT6803
67 61 59	RAM_A<4>	5.1	3	6	RP6822	RAM_A_R<4>	61 63 69 70	1 ZT6804
67 61 59	RAM_A<5>	5.1	2	7	RP6822	RAM_A_R<5>	61 63 69 70	1 ZT6805
67 61 59	RAM_A<6>	5.1	1	8	RP6822	RAM_A_R<6>	61 63 69 70	1 ZT6806
67 61 59	RAM_A<7>	5.1	3	6	RP6821	RAM_A_R<7>	61 63 69 70	1 ZT6807
67 61 59	RAM_A<8>	5.1	4	5	RP6821	RAM_A_R<8>	61 63 69 70	1 ZT6808
67 61 59	RAM_A<9>	5.1	1	8	RP6821	RAM_A_R<9>	61 63 69 70	1 ZT6809
67 61 59	RAM_A<10>	5.1	3	6	RP6824	RAM_A_R<10>	61 63 69 70	1 ZT6810
67 61 59	RAM_A<11>	5.1	2	7	RP6821	RAM_A_R<11>	61 63 69 70	1 ZT6811
67 61 59	RAM_A<12>	5.1	4	5	RP6820	RAM_A_R<12>	61 63 69 70	1 ZT6812
67 61 59	RAM_A<13>	5.1	4	5	RP6825	RAM_A_R<13>	61 63 69 70	1 ZT6813
67 61 59	RAM_A<14>	5.1	2	7	RP6820	RAM_A_R<14>	61 63 69 70	1 ZT6814
67 61 59	RAM_A<15>	5.1	1	8	RP6820	RAM_A_R<15>	61 63 69 70	1 ZT6815

VIAS FOR ECC STUB

67 61 59	RAM_BA<0>	5.1	4	5	RP6824	RAM_BA_R<0>	61 63 69 70	1 ZT6820
67 61 59	RAM_BA<1>	5.1	2	7	RP6824	RAM_BA_R<1>	61 63 69 70	ZT6821
67 61 59	RAM_BA<2>	5.1	3	6	RP6820	RAM_BA_R<2>	61 63 69 70	1 ZT6822
67 61 59	RAM_RAS_L	5.1	1	8	RP6825	RAM_RAS_L_R	61 63 69 70	1 ZT6825
67 61 59	RAM_CAS_L	5.1	3	6	RP6825	RAM_CAS_L_R	61 63 69 70	1 ZT6826
67 61 59	RAM_WE_L	5.1	2	7	RP6825	RAM_WE_L_R	61 63 69 70	1 ZT6827

VIAS FOR ECC STUB

PLACE NEAR KODIAK PRIOR TO BRANCH

PLACE AT END POINT TO SIMULATE ECC

C6870 24PF 5% 50V C0G 402	RAM_CS_L_R<0> 61 63 69 70	C6871 2PF +/-0.25PF 50V C0G 402-1	
C6880 24PF 5% 50V C0G 402	RAM_CKE_R<0> 61 62 63 69 70	C6881 2PF +/-0.25PF 50V C0G 402-1	
C6890 24PF 5% 50V C0G 402	RAM_ODT_R<0> 61 63 69 70	C6891 2PF +/-0.25PF 50V C0G 402-1	

Preliminary

MLB Mem Series Term

SYNC_MASTER=FINO-RT SYNC_DATE=05/18/2005

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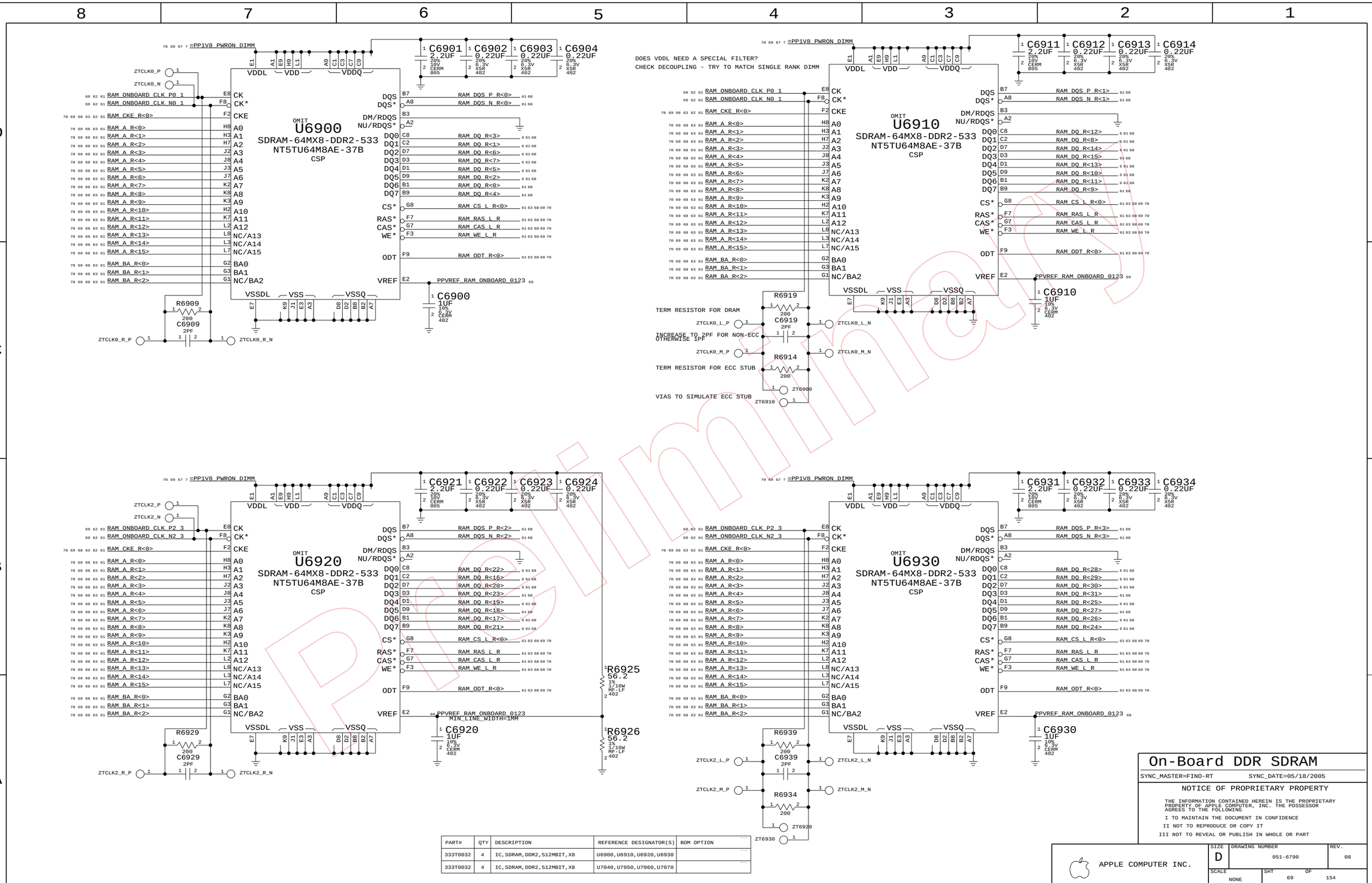
SCALE NONE	SHT 68 OF 154	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
333T0032	4	IC,SDRAM,DDR2,512MBIT,X8	U6900,U6910,U6920,U6930	
333T0032	4	IC,SDRAM,DDR2,512MBIT,X8	U7040,U7050,U7060,U7070	

On-Board DDR SDRAM

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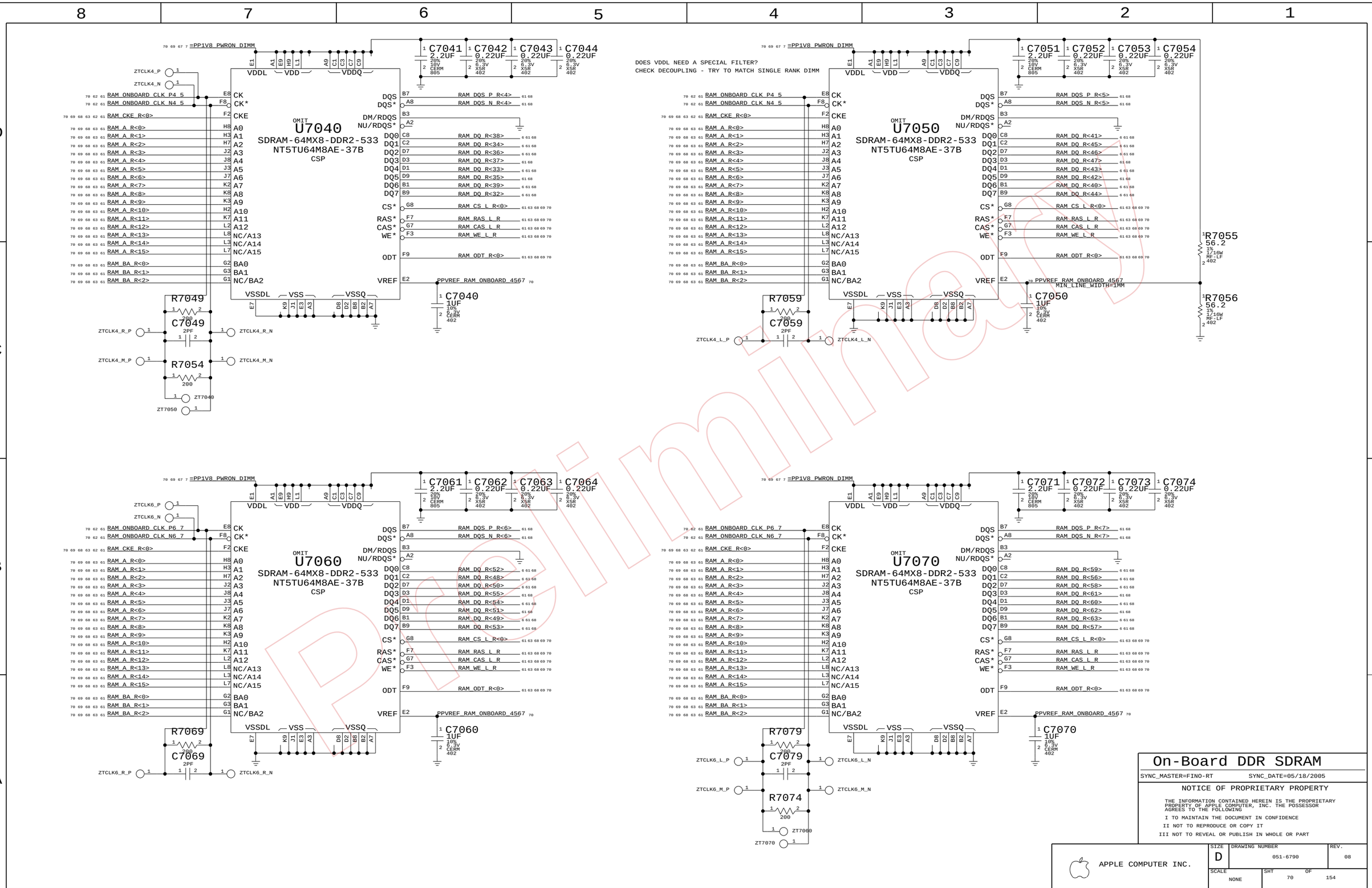
SCALE NONE SHT 69 OF 154


U7040
SDRAM-64MX8-DDR2-533
NT5TU64M8AE-37B
CSP
U7050
SDRAM-64MX8-DDR2-533
NT5TU64M8AE-37B
CSP
U7060
SDRAM-64MX8-DDR2-533
NT5TU64M8AE-37B
CSP
U7070
SDRAM-64MX8-DDR2-533
NT5TU64M8AE-37B
CSP
DOES VDDL NEED A SPECIAL FILTER?
CHECK DECOUPLING - TRY TO MATCH SINGLE RANK DIMM
=PP1V8_PWRON_DIMM
PPVREF_RAM_ONBOARD_4567
MIN_LINE_WIDTH=1MM
On-Board DDR SDRAM
SYNC_MASTER=FINO-RT
SYNC_DATE=05/18/2005
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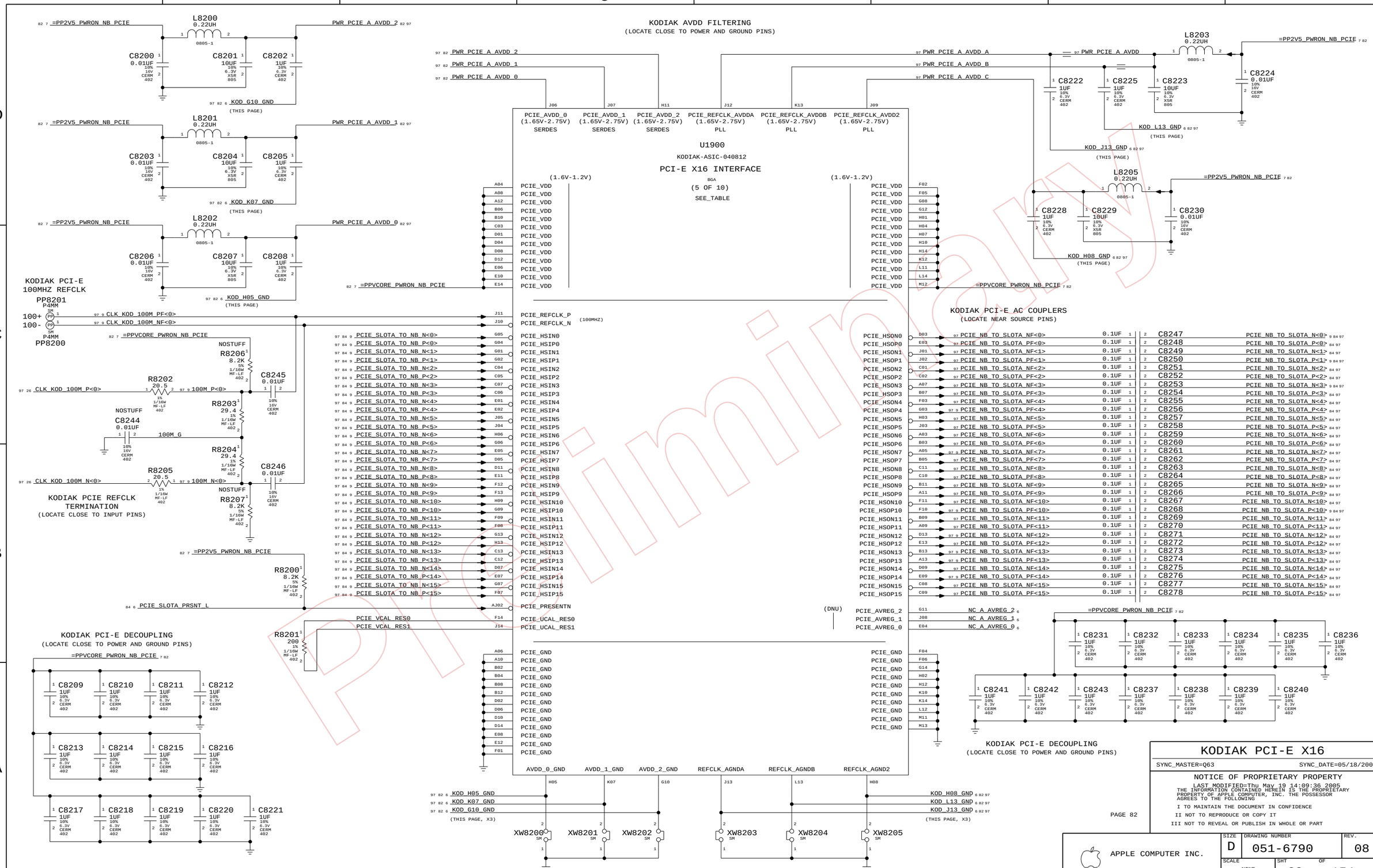
SIZE D
DRAWING NUMBER 051-6790
REV. 08
SCALE NONE
SHT 70 OF 154


KODIAK AVDD FILTERING
(LOCATE CLOSE TO POWER AND GROUND PINS)
L8200 0.22UH
L8201 0.22UH
L8202 0.22UH
L8203 0.22UH
L8205 0.22UH
=PP2V5_PWRON_NB_PCIE
PWR_PCIE_A_AVDD_2
PWR_PCIE_A_AVDD_1
PWR_PCIE_A_AVDD_0
PWR_PCIE_A_AVDD_A
PWR_PCIE_A_AVDD_B
PWR_PCIE_A_AVDD_C
PWR_PCIE_A_AVDD
KOD_G10_GND
KOD_K07_GND
KOD_H05_GND
KOD_L13_GND
KOD_J13_GND
KOD_H08_GND
(THIS PAGE)
U1900
KODIAK-ASIC-040812
PCI-E X16 INTERFACE
BGA
(5 OF 10)
SEE_TABLE
PCIE_AVDD_0 (1.65V-2.75V) SERDES
PCIE_AVDD_1 (1.65V-2.75V) SERDES
PCIE_AVDD_2 (1.65V-2.75V) SERDES
PCIE_REFCLK_AVDDA (1.65V-2.75V) PLL
PCIE_REFCLK_AVDDB (1.65V-2.75V) PLL
PCIE_REFCLK_AVDD2 (1.65V-2.75V) PLL
(1.6V-1.2V)
=PPVCORE_PWRON_NB_PCIE
KODIAK PCI-E 100MHZ REFCLK
PP8201 P4MM
PP8200 P4MM
CLK_KOD_100M_PF<0>
CLK_KOD_100M_NF<0>
CLK_KOD_100M_P<0>
CLK_KOD_100M_N<0>
100M_P<0>
100M_N<0>
100M_G
R8202 20.5
R8205 20.5
R8206 8.2K
R8207 8.2K
R8203 29.4
R8204 29.4
C8244 0.01UF
C8245 0.01UF
C8246 0.01UF
NOSTUFF
KODIAK PCIE REFCLK TERMINATION
(LOCATE CLOSE TO INPUT PINS)
PCIE_SLOTA_PRSNT_L
R8200 8.2K
R8201 200
PCIE_VCAL_RES0
PCIE_VCAL_RES1
PCIE_REFCLK_P
PCIE_REFCLK_N
(100MHZ)
PCIE_HSIN0
PCIE_HSIP0
PCIE_HSIN1
PCIE_HSIP1
PCIE_HSIN2
PCIE_HSIP2
PCIE_HSIN3
PCIE_HSIP3
PCIE_HSIN4
PCIE_HSIP4
PCIE_HSIN5
PCIE_HSIP5
PCIE_HSIN6
PCIE_HSIP6
PCIE_HSIN7
PCIE_HSIP7
PCIE_HSIN8
PCIE_HSIP8
PCIE_HSIN9
PCIE_HSIP9
PCIE_HSIN10
PCIE_HSIP10
PCIE_HSIN11
PCIE_HSIP11
PCIE_HSIN12
PCIE_HSIP12
PCIE_HSIN13
PCIE_HSIP13
PCIE_HSIN14
PCIE_HSIP14
PCIE_HSIN15
PCIE_HSIP15
PCIE_PRESENTN
PCIE_UCAL_RES0
PCIE_UCAL_RES1
(DNU)
PCIE_AVREG_2
PCIE_AVREG_1
PCIE_AVREG_0
NC_A_AVREG_2
NC_A_AVREG_1
NC_A_AVREG_0
PCIE_GND
KODIAK PCI-E AC COUPLERS
(LOCATE NEAR SOURCE PINS)
PCIE_NB_TO_SLOTA_NF<0>
PCIE_NB_TO_SLOTA_PF<0>
PCIE_NB_TO_SLOTA_NF<1>
PCIE_NB_TO_SLOTA_PF<1>
PCIE_NB_TO_SLOTA_NF<2>
PCIE_NB_TO_SLOTA_PF<2>
PCIE_NB_TO_SLOTA_NF<3>
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PCIE_NB_TO_SLOTA_PF<4>
PCIE_NB_TO_SLOTA_NF<5>
PCIE_NB_TO_SLOTA_PF<5>
PCIE_NB_TO_SLOTA_NF<6>
PCIE_NB_TO_SLOTA_PF<6>
PCIE_NB_TO_SLOTA_NF<7>
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PCIE_NB_TO_SLOTA_P<15>
KODIAK PCI-E DECOUPLING
(LOCATE CLOSE TO POWER AND GROUND PINS)
AVDD_0_GND
AVDD_1_GND
AVDD_2_GND
REFCLK_AGNDA
REFCLK_AGNDB
REFCLK_AGND2
XW8200
XW8201
XW8202
XW8203
XW8204
XW8205
KODIAK PCI-E X16
SYNC_MASTER=Q63
SYNC_DATE=05/18/2005
NOTICE OF PROPRIETARY PROPERTY
LAST MODIFIED=Thu May 19 14:09:36 2005
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PAGE 82
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6790
REV. 08
SCALE NONE
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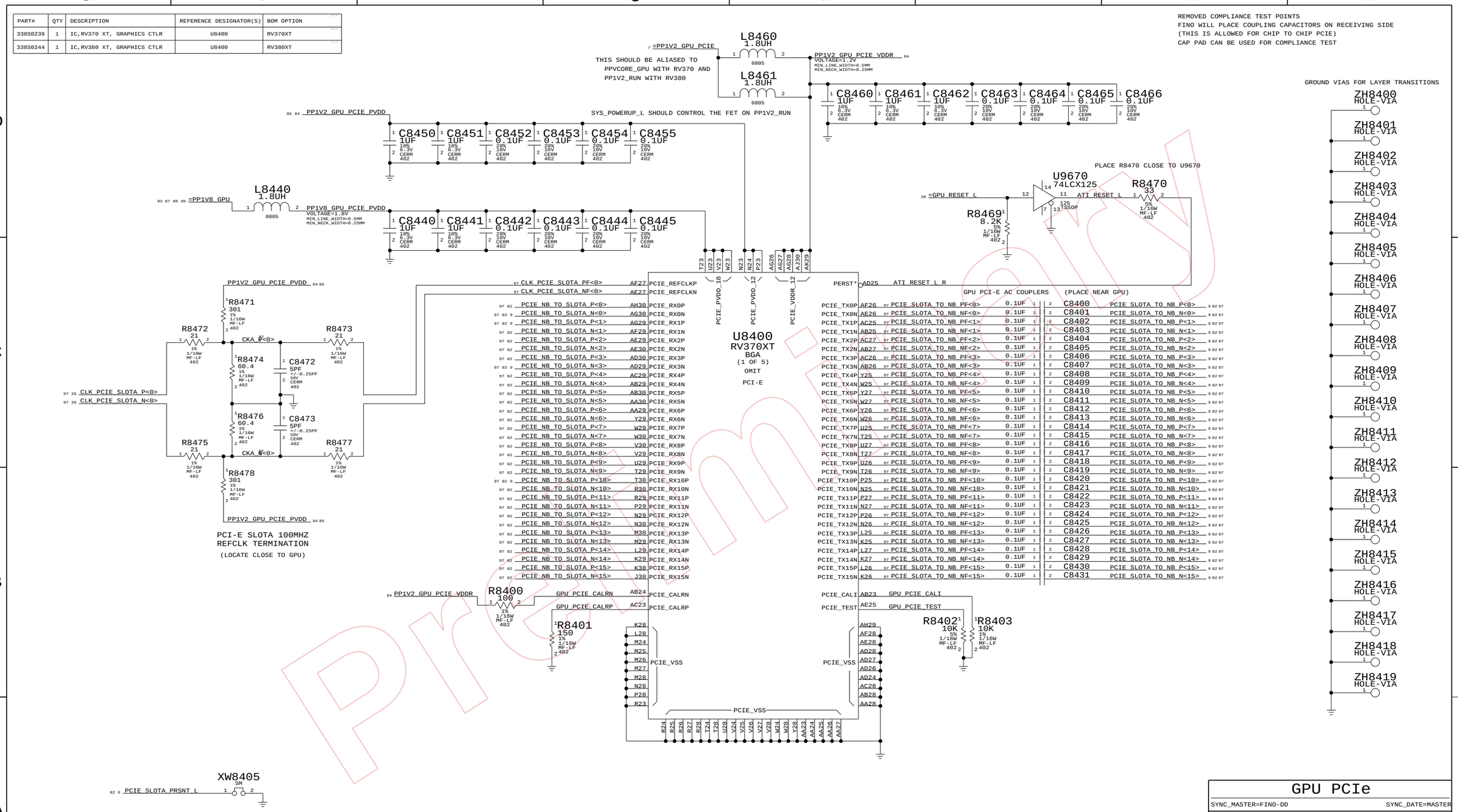
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0239	1	IC,RV370 XT, GRAPHICS CTLR	U8400	RV370XT
338S0244	1	IC,RV380 XT, GRAPHICS CTLR	U8400	RV380XT

REMOVED COMPLIANCE TEST POINTS
FINO WILL PLACE COUPLING CAPACITORS ON RECEIVING SIDE
(THIS IS ALLOWED FOR CHIP TO CHIP PCIE)
CAP PAD CAN BE USED FOR COMPLIANCE TEST



GPU PCIe

SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

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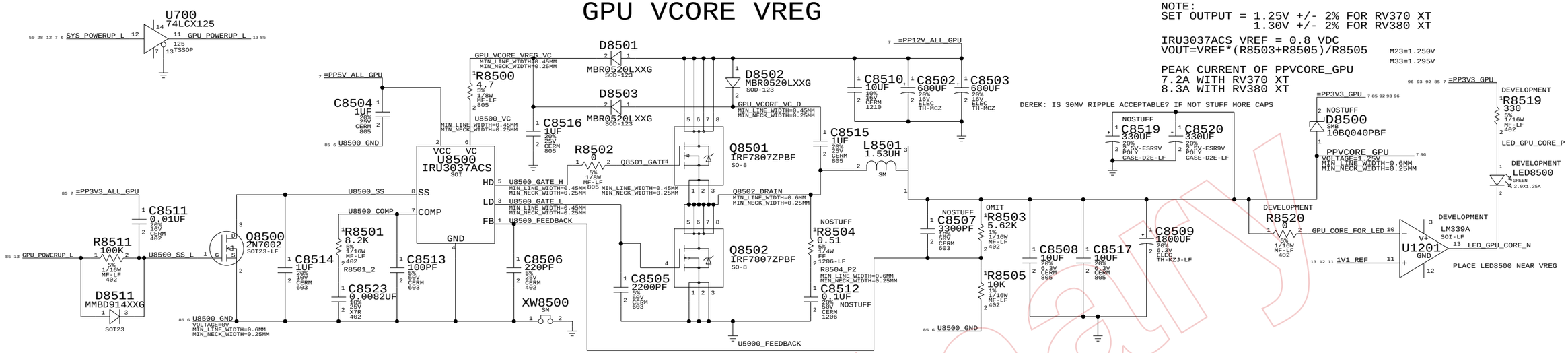
GPU VCORE VREG

NOTE:
SET OUTPUT = 1.25V +/- 2% FOR RV370 XT
1.30V +/- 2% FOR RV380 XT

IRU3037ACS VREF = 0.8 VDC
VOUT=VREF*(R8503+R8505)/R8505

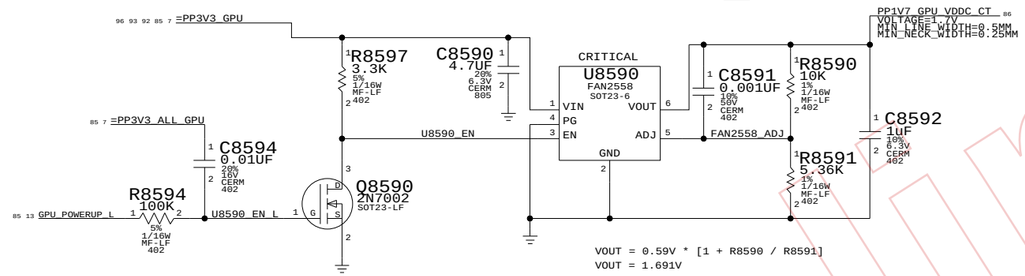
M23=1.250V
M33=1.295V

PEAK CURRENT OF PPVCORE_GPU
7.2A WITH RV370 XT
8.3A WITH RV380 XT

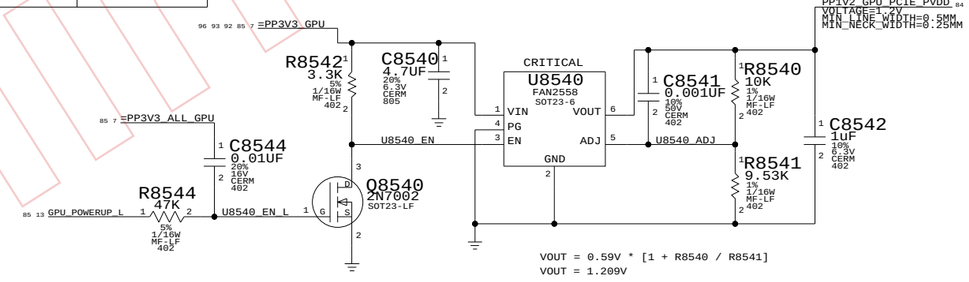


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0291	1	RES,5.62K OHM,1/16W,1%,0402	R8503	RV370XT
114S0295	1	RES,6.19K OHM,1/16W,1%,0402	R8503	RV380XT

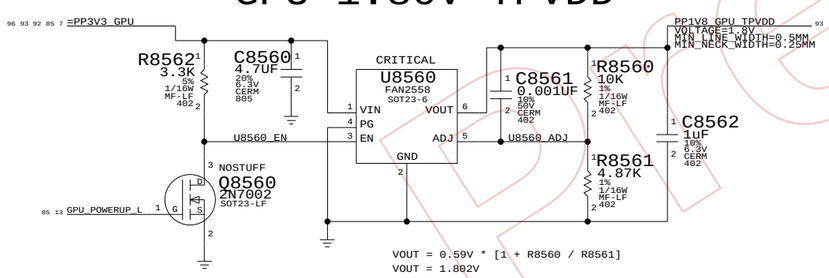
GPU 1.7V VDDC_CT



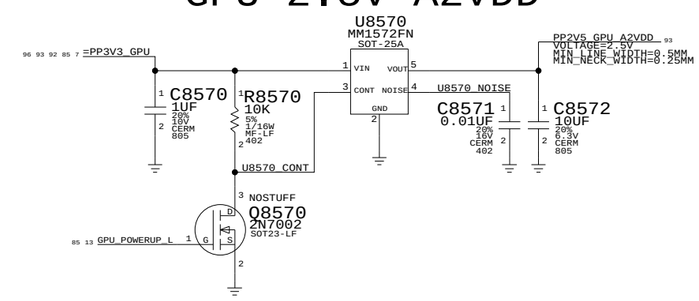
GPU 1.20V PCIE PVDD



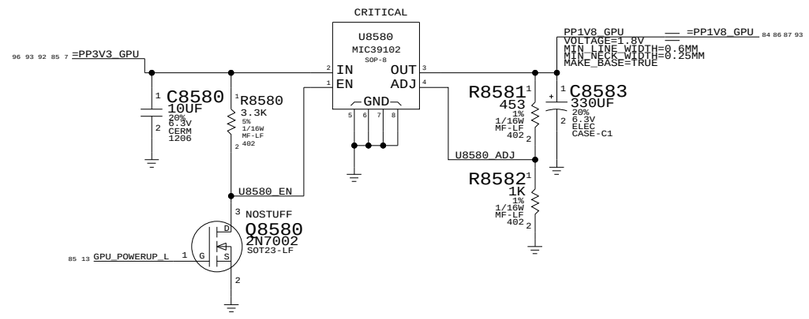
GPU 1.80V TPVDD



GPU 2.5V A2VDD



GPU 1.8V VREG



POWER SEQUENCING FOR RV370/80: =PP3V3_GPU > =PPV_GPU_MEM > VDDC_CT > PPVCORE_GPU
PP2V5_GPU_A2VDD > PP1V8_GPU > PCIE_PVDD

THE ENTIRE SEQUENCE SHOULD TAKE LESS THAN 40 MS (T1+T3 IN DATABOOK)
HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER
POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER

Graphics Vregs

SYNC_MASTER=M23-DD SYNC_DATE=MASTER

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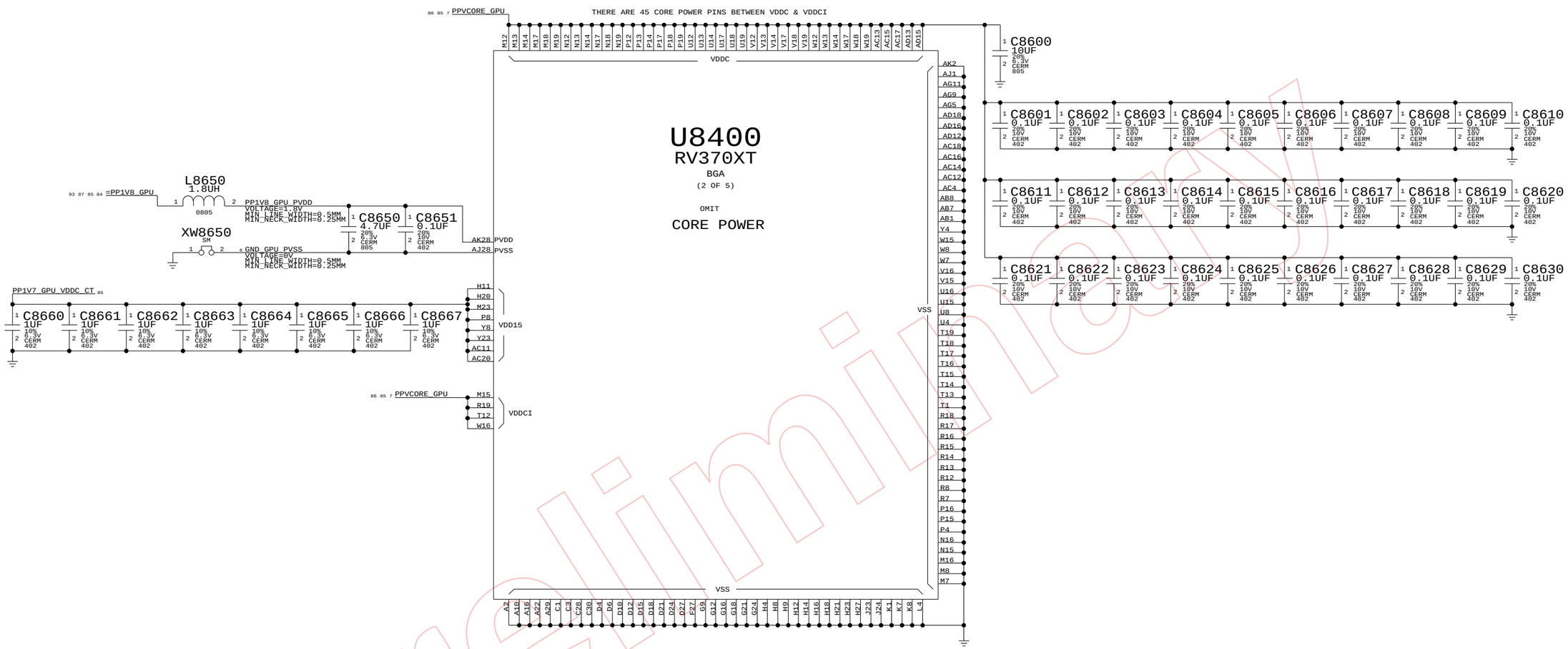
SCALE NONE	SHT 85	OF 154

Preliminary



Preliminary

GPU Core Power

SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

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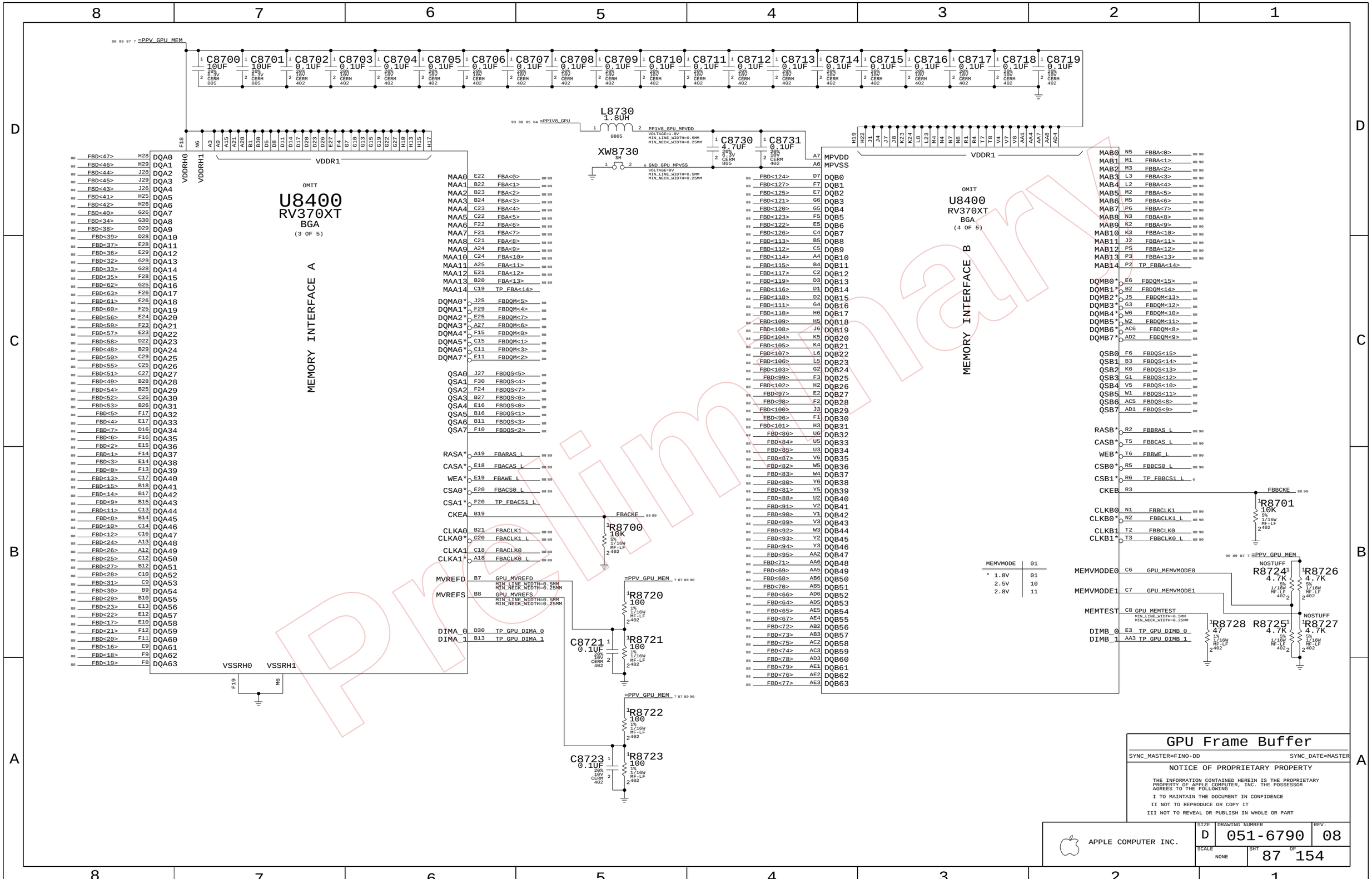
D	051-6790	08
SCALE NONE	SHT 86 OF 154	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C8701 10UF 20% 6.3V CERM 805
C8702 0.1UF 20% 10V CERM 402
C8703 0.1UF 20% 10V CERM 402
C8704 0.1UF 20% 10V CERM 402
C8705 0.1UF 20% 10V CERM 402
C8706 0.1UF 20% 10V CERM 402
C8707 0.1UF 20% 10V CERM 402
C8708 0.1UF 20% 10V CERM 402
C8709 0.1UF 20% 10V CERM 402
C8710 0.1UF 20% 10V CERM 402
C8711 0.1UF 20% 10V CERM 402
C8712 0.1UF 20% 10V CERM 402
C8713 0.1UF 20% 10V CERM 402
C8714 0.1UF 20% 10V CERM 402
C8715 0.1UF 20% 10V CERM 402
C8716 0.1UF 20% 10V CERM 402
C8717 0.1UF 20% 10V CERM 402
C8718 0.1UF 20% 10V CERM 402
C8719 0.1UF 20% 10V CERM 402
L8730 1.8UH 0805
=PP1V8_GPU
PP1V8_GPU_MPVDD
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
XW8730 SM
GND_GPU_MPVSS
VOLTAGE=0V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C8730 4.7UF 20% 6.3V CERM 805
C8731 0.1UF 20% 10V CERM 402
VDDR1
OMIT
U8400
RV370XT
BGA
(3 OF 5)
MEMORY INTERFACE A
OMIT
U8400
RV370XT
BGA
(4 OF 5)
MEMORY INTERFACE B
VDDRH0
VDDRH1
VSSRH0
VSSRH1
MPVDD
MPVSS
DQA0 DQA1 DQA2 DQA3 DQA4 DQA5 DQA6 DQA7 DQA8 DQA9 DQA10 DQA11 DQA12 DQA13 DQA14 DQA15 DQA16 DQA17 DQA18 DQA19 DQA20 DQA21 DQA22 DQA23 DQA24 DQA25 DQA26 DQA27 DQA28 DQA29 DQA30 DQA31 DQA32 DQA33 DQA34 DQA35 DQA36 DQA37 DQA38 DQA39 DQA40 DQA41 DQA42 DQA43 DQA44 DQA45 DQA46 DQA47 DQA48 DQA49 DQA50 DQA51 DQA52 DQA53 DQA54 DQA55 DQA56 DQA57 DQA58 DQA59 DQA60 DQA61 DQA62 DQA63
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MAA0 MAA1 MAA2 MAA3 MAA4 MAA5 MAA6 MAA7 MAA8 MAA9 MAA10 MAA11 MAA12 MAA13 MAA14
DQMA0* DQMA1* DQMA2* DQMA3* DQMA4* DQMA5* DQMA6* DQMA7*
QSA0 QSA1 QSA2 QSA3 QSA4 QSA5 QSA6 QSA7
RASA* CASA* WEA* CSA0* CSA1* CKEA
CLKA0 CLKA0* CLKA1 CLKA1*
MVREFD MVREFS
DIMA_0 DIMA_1
MAB0 MAB1 MAB2 MAB3 MAB4 MAB5 MAB6 MAB7 MAB8 MAB9 MAB10 MAB11 MAB12 MAB13 MAB14
DQMB0* DQMB1* DQMB2* DQMB3* DQMB4* DQMB5* DQMB6* DQMB7*
QSB0 QSB1 QSB2 QSB3 QSB4 QSB5 QSB6 QSB7
RASB* CASB* WEB* CSB0* CSB1* CKEB
CLKB0 CLKB0* CLKB1 CLKB1*
MEMVMODE0 MEMVMODE1 MEMTEST DIMB_0 DIMB_1
R8700 10K 5% 1/16W MF-LF 402
R8701 10K 5% 1/16W MF-LF 402
R8720 100 1% 1/16W MF-LF 402
R8721 100 1% 1/16W MF-LF 402
R8722 100 1% 1/16W MF-LF 402
R8723 100 1% 1/16W MF-LF 402
C8721 0.1UF 20% 10V CERM 402
C8723 0.1UF 20% 10V CERM 402
R8724 4.7K NOSTUFF
R8725 4.7K NOSTUFF
R8726 4.7K
R8727 4.7K NOSTUFF
R8728 47
MEMVMODE 01
* 1.8V 01
2.5V 10
2.8V 11
GPU Frame Buffer
SYNC_MASTER=FINO-DD
SYNC_DATE=MASTER
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SHT 87 OF 154

FRAME BUFFER A TERMINATION

PLACE R'S CLOSE TO MEMORY

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PLACE CLOCK TERMINATION AFTER MEMORY
GPU -> MEMORY -> TERMINATION

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R8821 56.2 1% 1/16W MF-LF 402 — C8821 0.01UF 20% 16V CERM 402
FBACLK0_L

FBACLK1
R8822 56.2 1% 1/16W MF-LF 402
FBACLK1_TERM MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
R8823 56.2 1% 1/16W MF-LF 402 — C8823 0.01UF 20% 16V CERM 402
FBACLK1_L

FRAME BUFFER B TERMINATION

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FBD<112>	22	3	RP8811 6	RFBD<112>
FBD<113>	22	4	RP8811 5	RFBD<113>
FBD<114>	22	2	RP8811 7	RFBD<114>
FBD<115>	22	1	RP8811 8	RFBD<115>
FBD<116>	22	3	RP8806 6	RFBD<116>
FBD<117>	22	4	RP8806 5	RFBD<117>
FBD<118>	22	2	RP8806 7	RFBD<118>
FBD<119>	22	1	RP8806 8	RFBD<119>
FBD<120>	22	3	RP8804 6	RFBD<120>
FBD<121>	22	4	RP8804 5	RFBD<121>
FBD<122>	22	2	RP8804 7	RFBD<122>
FBD<123>	22	1	RP8804 8	RFBD<123>
FBD<124>	22	4	RP8805 5	RFBD<124>
FBD<125>	22	2	RP8805 7	RFBD<125>
FBD<126>	22	3	RP8805 6	RFBD<126>
FBD<127>	22	1	RP8805 8	RFBD<127>

FBDQS<8>	22	1	R8808
FBDQS<9>	22	1	R8809
FBDQS<10>	22	1	R8810
FBDQS<11>	22	1	R8811
FBDQS<12>	22	1	R8812
FBDQS<13>	22	1	R8813
FBDQS<14>	22	1	R8814
FBDQS<15>	22	1	R8815

FBDQM<8>	22	1	R8838
FBDQM<9>	22	1	R8839
FBDQM<10>	22	1	R8840
FBDQM<11>	22	1	R8841
FBDQM<12>	22	1	R8842
FBDQM<13>	22	1	R8843
FBDQM<14>	22	1	R8844
FBDQM<15>	22	1	R8845

FBBCLK0
R8824 56.2 1% 1/16W MF-LF 402
FBBCLK0_TERM MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
R8825 56.2 1% 1/16W MF-LF 402 — C8825 0.01UF 20% 16V CERM 402
FBBCLK0_L

FBBCLK1
R8826 56.2 1% 1/16W MF-LF 402
FBBCLK1_TERM MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
R8827 56.2 1% 1/16W MF-LF 402 — C8827 0.01UF 20% 16V CERM 402
FBBCLK1_L

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FBD<127..0>		GPU_FB	GPU_FB	
RFBD<127..0>		GPU_FB	GPU_FB	
FBA<13..0>		GPU_FB	GPU_FB	
FBBA<13..0>		GPU_FB	GPU_FB	
FBDQM<15..0>		GPU_FB	GPU_FB	
FBDQS<15..0>		GPU_FB	GPU_FBDQS	
FBARAS_L		GPU_FB	GPU_FB	
FBACAS_L		GPU_FB	GPU_FB	
FBAWE_L		GPU_FB	GPU_FB	
FBACS0_L		GPU_FB	GPU_FB	
FBACKE		GPU_FB	GPU_FB	
FBBRAS_L		GPU_FB	GPU_FB	
FBBCAS_L		GPU_FB	GPU_FB	
FBBWE_L		GPU_FB	GPU_FB	
FBBCS0_L		GPU_FB	GPU_FB	
FBBCKE		GPU_FB	GPU_FB	

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FBACLK0		GPU_FBCLK	GPU_FBCLK	FBACLK0
FBACLK0_L		GPU_FBCLK	GPU_FBCLK	FBACLK0
FBACLK1		GPU_FBCLK	GPU_FBCLK	FBACLK1
FBACLK1_L		GPU_FBCLK	GPU_FBCLK	FBACLK1
FBBCLK0		GPU_FBCLK	GPU_FBCLK	FBBCLK0
FBBCLK0_L		GPU_FBCLK	GPU_FBCLK	FBBCLK0
FBBCLK1		GPU_FBCLK	GPU_FBCLK	FBBCLK1
FBBCLK1_L		GPU_FBCLK	GPU_FBCLK	FBBCLK1

FB Series Termination

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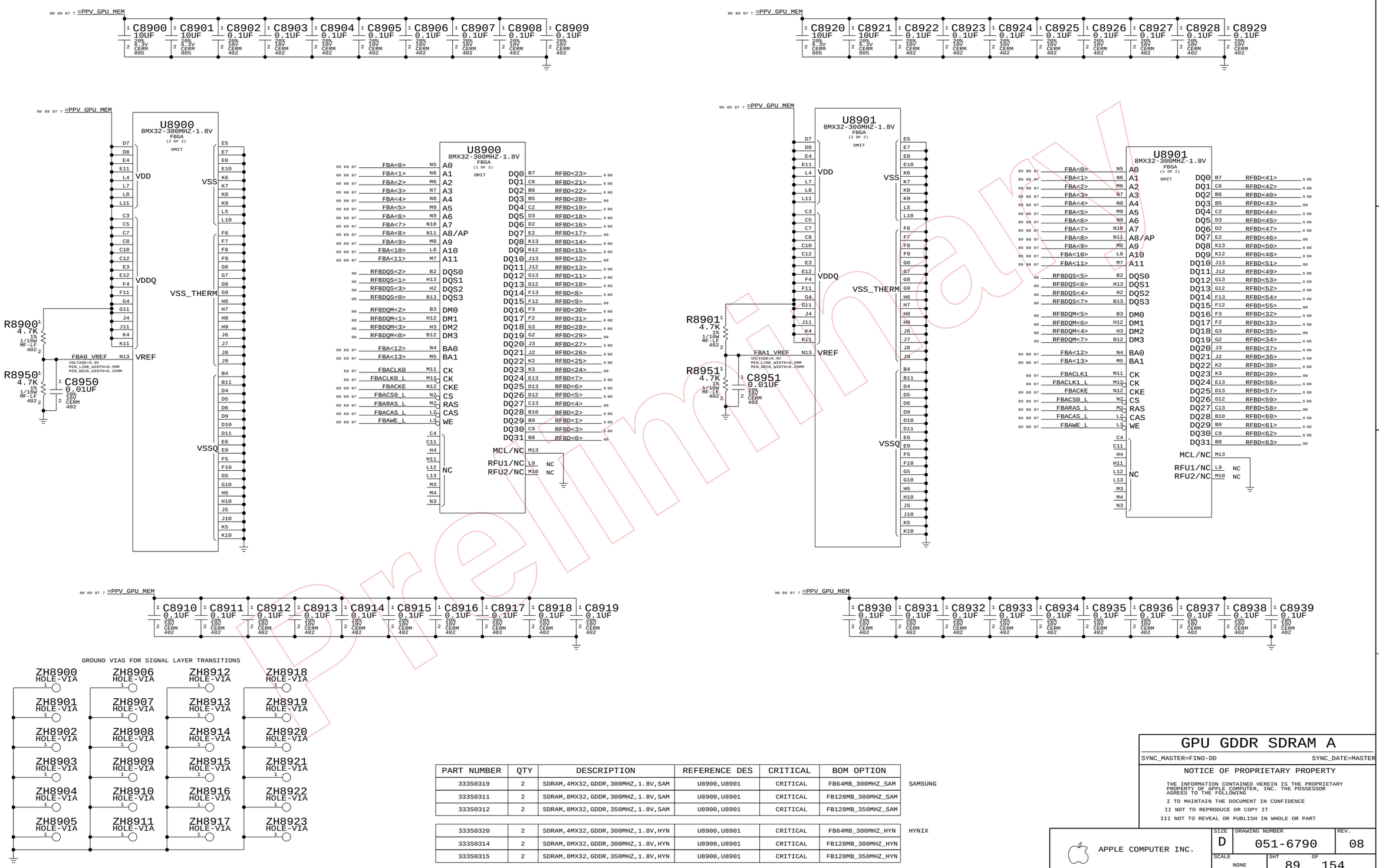

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
333S0319	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB64MB_300MHZ_SAM	SAMSUNG
333S0311	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB128MB_300MHZ_SAM	
333S0312	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB128MB_350MHZ_SAM	
333S0320	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB64MB_300MHZ_HYN	HYNIX
333S0314	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB128MB_300MHZ_HYN	
333S0315	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB128MB_350MHZ_HYN	

GPU GDDR SDRAM A

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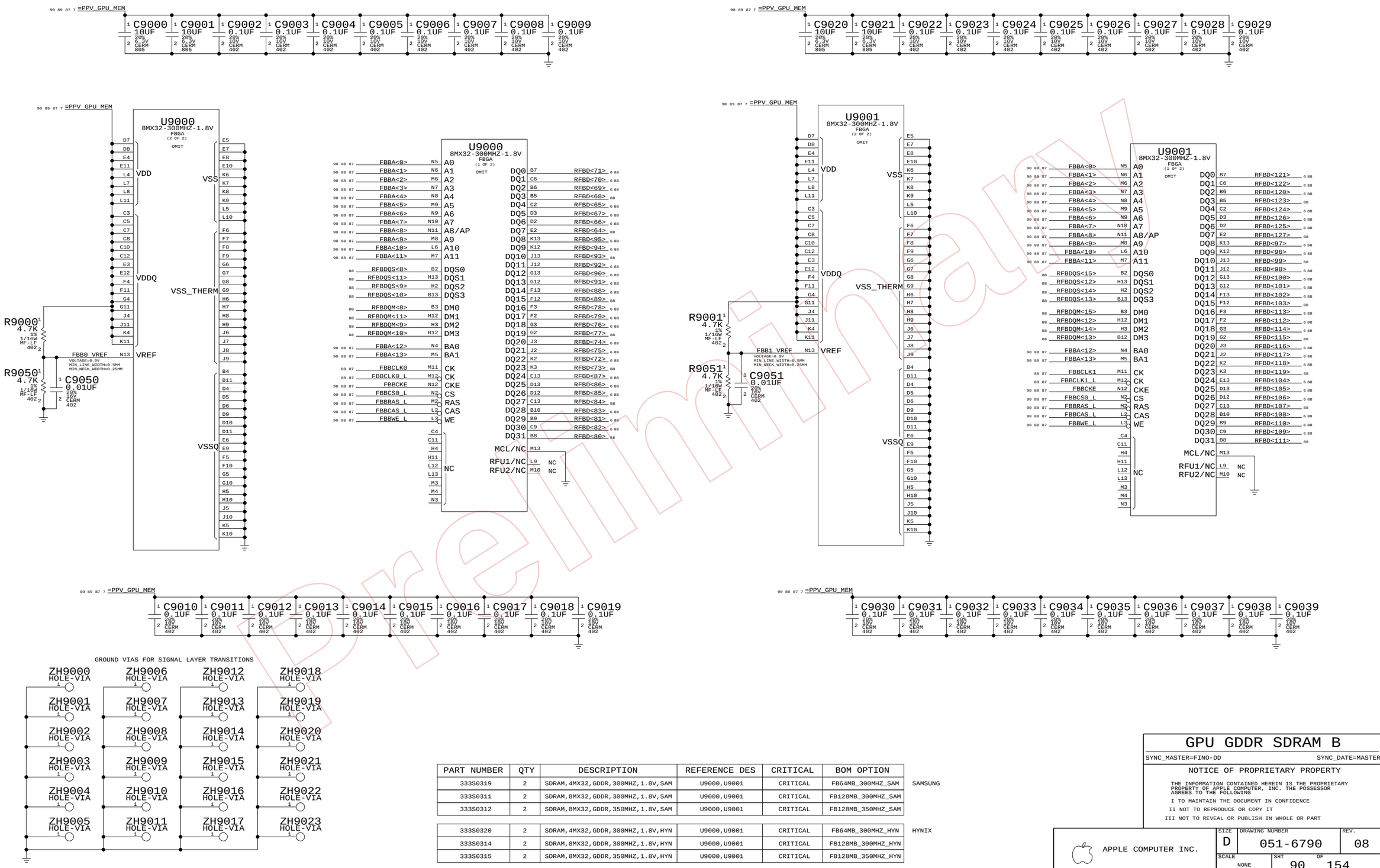

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
333S0319	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB64MB_300MHZ_SAM	SAMSUNG
333S0311	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB128MB_300MHZ_SAM	
333S0312	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB128MB_350MHZ_SAM	
333S0320	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB64MB_300MHZ_HYN	HYNIX
333S0314	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB128MB_300MHZ_HYN	
333S0315	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB128MB_350MHZ_HYN	

GPU GDDR SDRAM B

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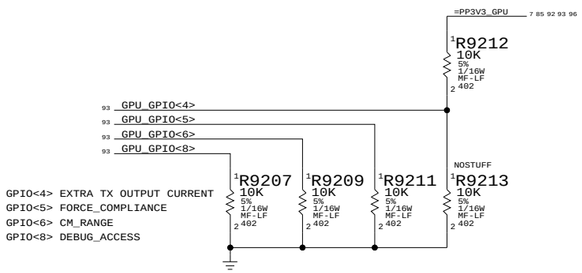
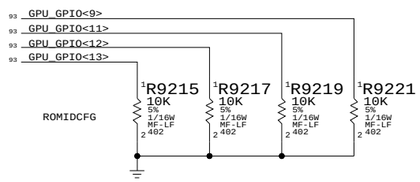
ATI STRAPS

GPIO<1> TRANSMITTER DE-EMPHASIS (ACTIVE LOW)

GPIO<0> TRANSMITTER POWER SAVINGS
(FEATURE DOES NOT WORK - PULLED HIGH TO DISABLE)

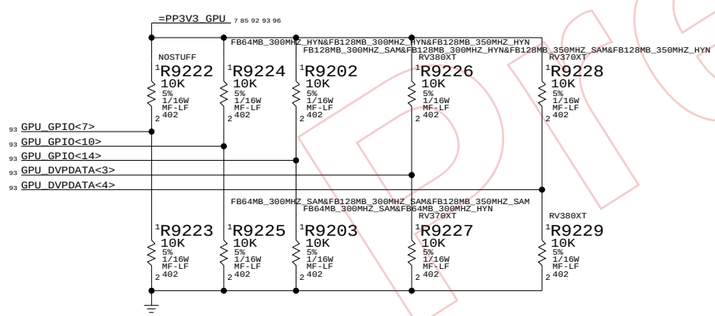


GPIO<4> EXTRA TX OUTPUT CURRENT
GPIO<5> FORCE_COMPLIANCE
GPIO<6> CM_RANGE
GPIO<8> DEBUG_ACCESS



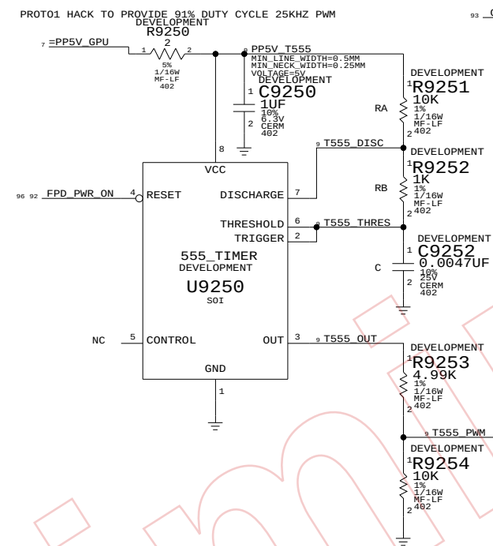
ROMIDCFG

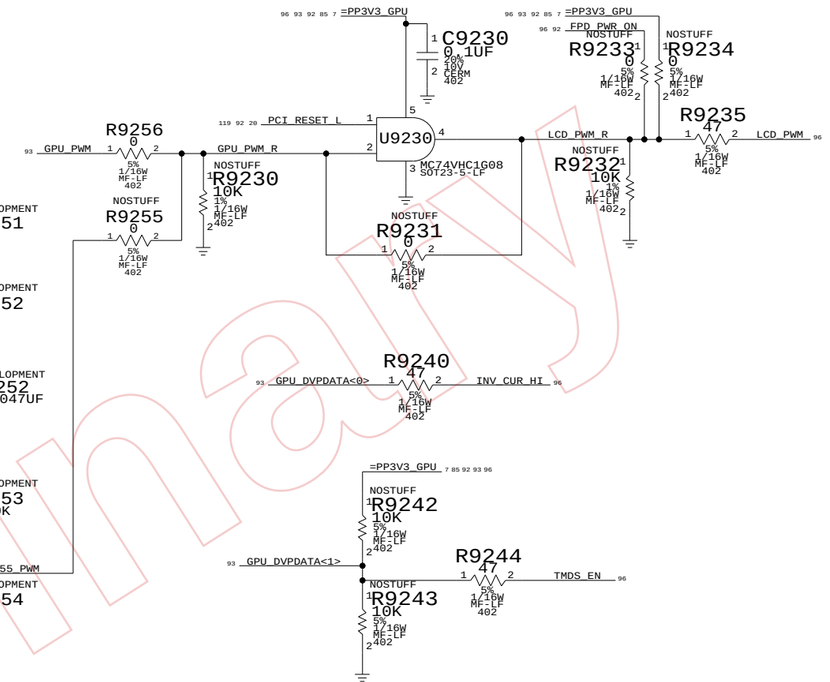
MEMORY STRAPS

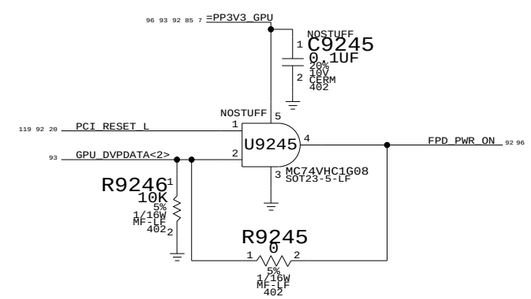


GPIO<7> - MEMORY DIE REVISION
  0 - ORIGINAL DIE REVISION
  1 - NEW (FUTURE) DIE REV
GPIO<10> - MEMORY VENDOR
  0 - SAMSUNG
  1 - HYNIX
GPIO<14> - MEMORY DENSITY
  0 - 4MX32
  1 - 8MX32
DVPDATA<3,4> - SPEED
  00 - 325E / 200M
  01 - 400E / 300M
  10 - 500E / 350M
  11 - RESERVED FOR FUTURE USE

APPLE GPIOS







GPU Straps

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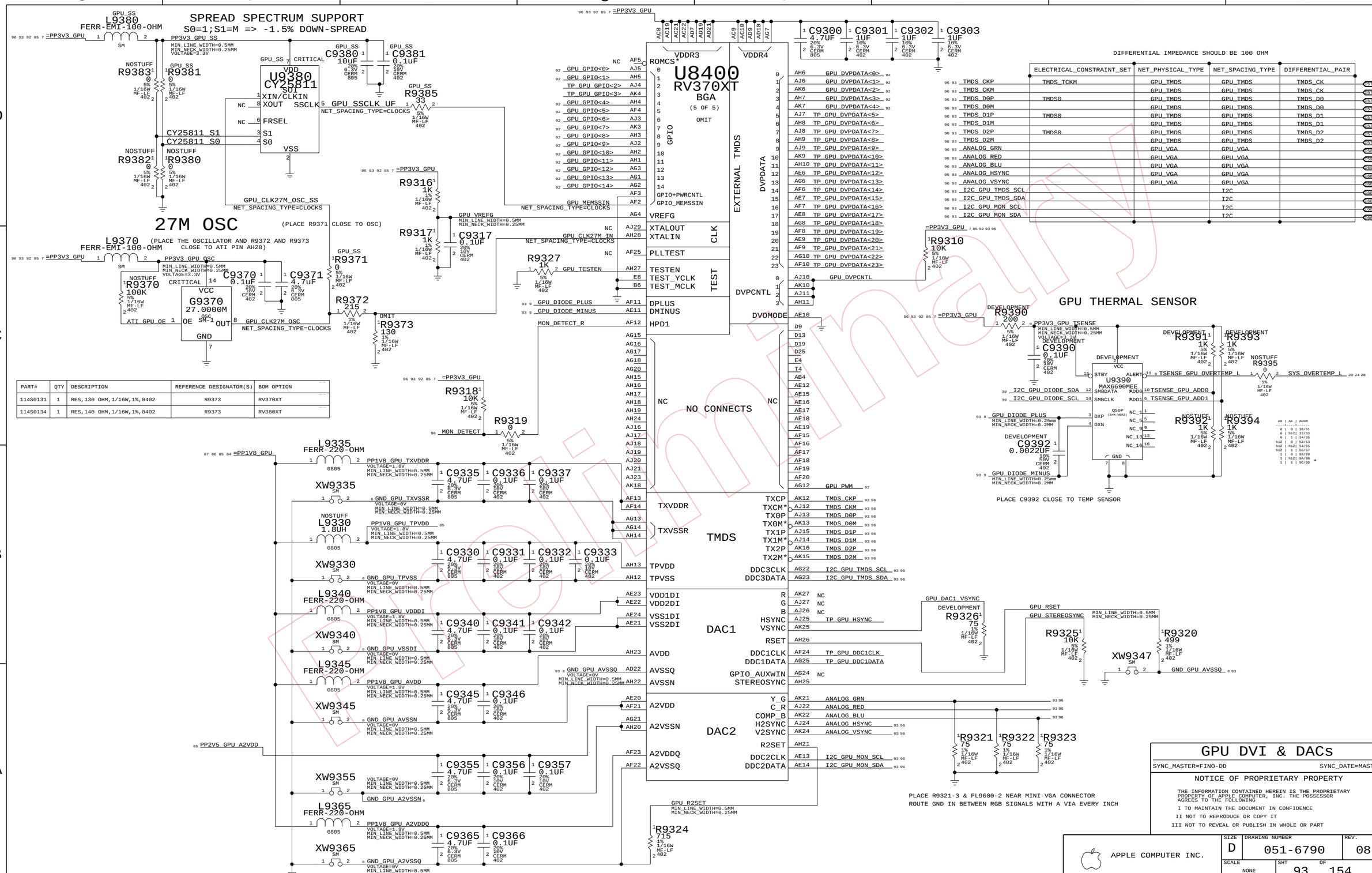


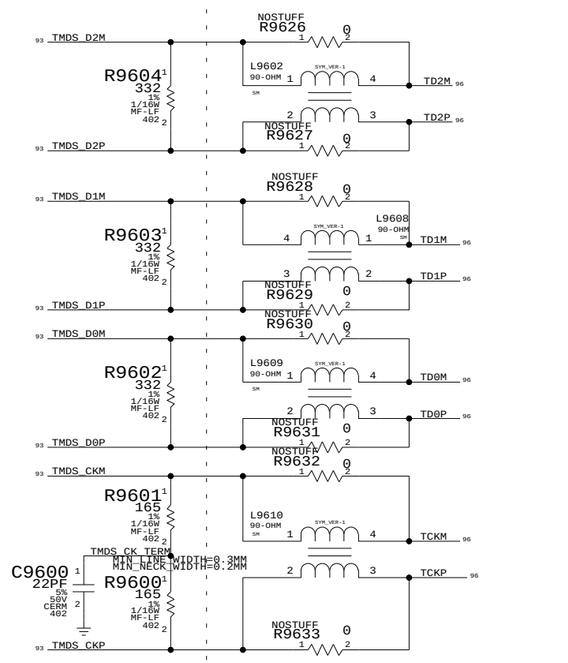
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0131	1	RES,130 OHM,1/16W,1%,0402	R9373	RV370XT
114S0134	1	RES,140 OHM,1/16W,1%,0402	R9373	RV380XT

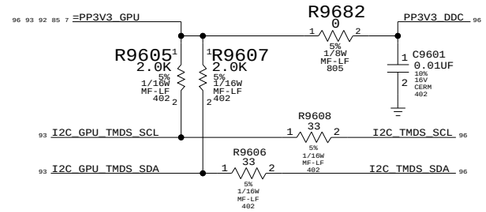
INTERNAL LCD

	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
TCKP	GPU_TMDS	GPU_TMDS	TCK	TB15
TCKM	GPU_TMDS	GPU_TMDS	TCK	TB17
TD0P	GPU_TMDS	GPU_TMDS	TD0	TB16
TD0M	GPU_TMDS	GPU_TMDS	TD0	TB18
TD1P	GPU_TMDS	GPU_TMDS	TD1	TB19
TD1M	GPU_TMDS	GPU_TMDS	TD1	TB20
TD2P	GPU_TMDS	GPU_TMDS	TD2	TB22
TD2M	GPU_TMDS	GPU_TMDS	TD2	TB21

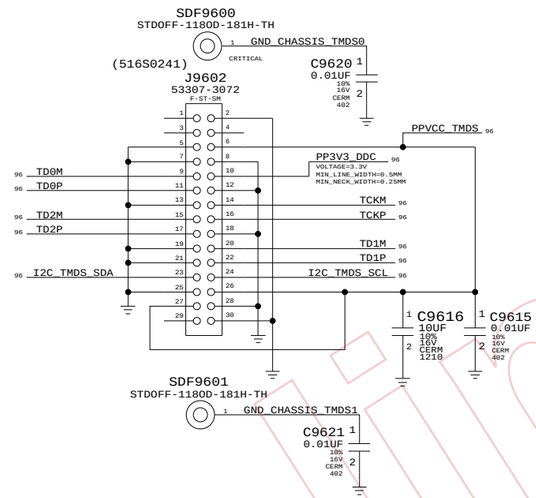
PLACE R9600-R9604, C9600 AS CLOSE TO GPU AS POSSIBLE

PLACE FILTER CLOSE TO TMDS CONNECTOR

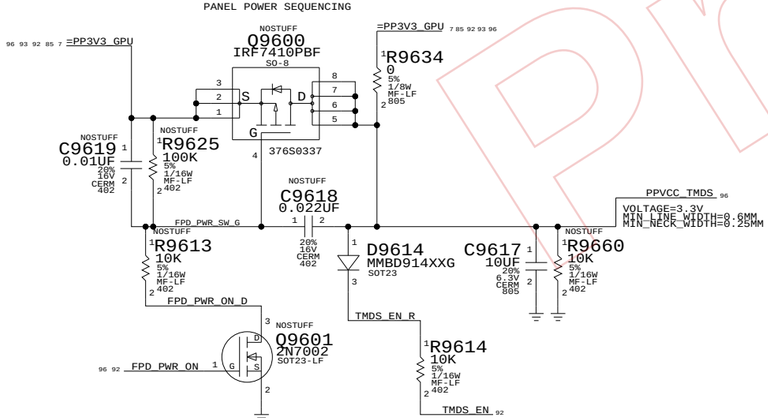


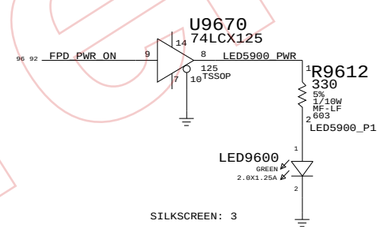


INTERNAL TMDS CONNECTOR



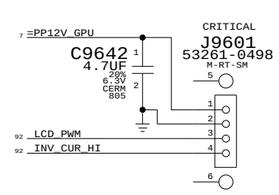
PANEL POWER SEQUENCING





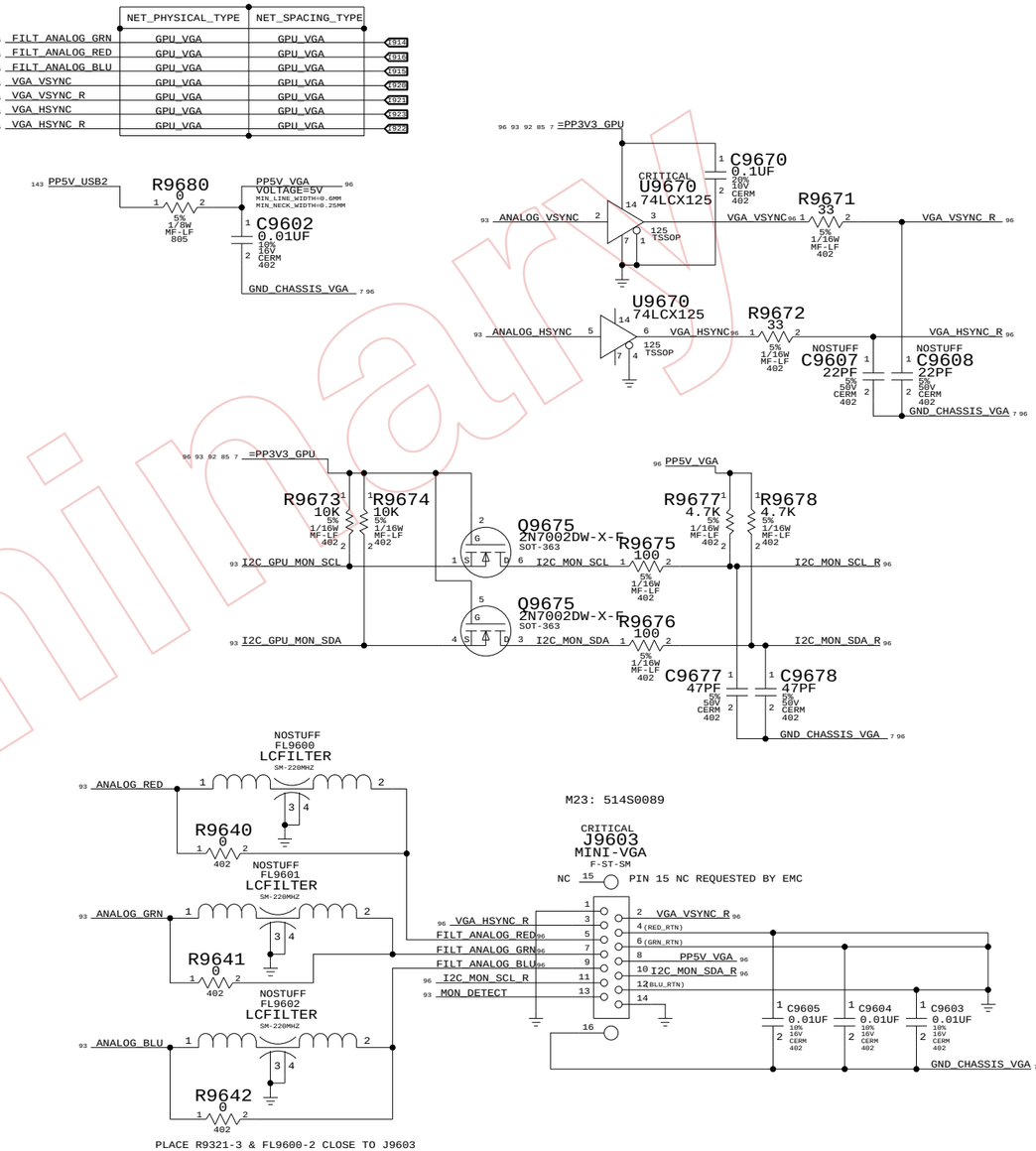
SILKSCREEN: 3

INVERTER INTERFACE



EXTERNAL VGA CONNECTOR

	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	
FILT_ANALOG_GRN	GPU_VGA	GPU_VGA	AD14
FILT_ANALOG_RED	GPU_VGA	GPU_VGA	AD16
FILT_ANALOG_BLU	GPU_VGA	GPU_VGA	AD15
VGA_VSYNC	GPU_VGA	GPU_VGA	AD20
VGA_VSYNC_R	GPU_VGA	GPU_VGA	AD21
VGA_HSYNC	GPU_VGA	GPU_VGA	AD23
VGA_HSYNC_R	GPU_VGA	GPU_VGA	AD22



PLACE R9321-3 & FL9600-2 CLOSE TO J9603

TMDS/Inverter/ExtVGA

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KODIAK PCI-E PHYSICAL CONSTRAINT TABLE

SIG_NAME	ELECTRICAL_CONSTRAINT_SET	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
9 82 100M N<0>		CLK_100M	PCIE_CLK	PCIE_CLK
9 82 100M P<0>		CLK_100M	PCIE_CLK	PCIE_CLK
82 26 CLK_KOD_100M_N<0>		CLK_KODPCIE_100M	PCIE_CLK	PCIE_CLK
82 26 CLK_KOD_100M_P<0>		CLK_KODPCIE_100M	PCIE_CLK	PCIE_CLK
9 82 CLK_KOD_100M_NF<0>		CLK_KODPCIE_100MF	PCIE_CLK	PCIE_CLK
9 82 CLK_KOD_100M_PF<0>		CLK_KODPCIE_100MF	PCIE_CLK	PCIE_CLK
82 PCIE_NB_TO_SLOTA_NF<0>	PCIE_NB2SA0	PCIE_NB_TO_SLOTA_0_F	PCIE_DATA	PCIE_DATA
82 PCIE_NB_TO_SLOTA_PF<0>	PCIE_NB2SA0	PCIE_NB_TO_SLOTA_0_F	PCIE_DATA	PCIE_DATA
82 PCIE_NB_TO_SLOTA_NF<1>	PCIE_NB2SA1	PCIE_NB_TO_SLOTA_1_F	PCIE_DATA	PCIE_DATA
82 PCIE_NB_TO_SLOTA_PF<1>	PCIE_NB2SA1	PCIE_NB_TO_SLOTA_1_F	PCIE_DATA	PCIE_DATA
82 PCIE_NB_TO_SLOTA_NF<2>	PCIE_NB2SA2	PCIE_NB_TO_SLOTA_2_F	PCIE_DATA	PCIE_DATA
82 PCIE_NB_TO_SLOTA_PF<2>	PCIE_NB2SA2	PCIE_NB_TO_SLOTA_2_F	PCIE_DATA	PCIE_DATA
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82 PCIE_NB_TO_SLOTA_PF<3>	PCIE_NB2SA3	PCIE_NB_TO_SLOTA_3_F	PCIE_DATA	PCIE_DATA
82 PCIE_NB_TO_SLOTA_NF<4>	PCIE_NB2SA4	PCIE_NB_TO_SLOTA_4_F	PCIE_DATA	PCIE_DATA
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9 82 PCIE_NB_TO_SLOTA_PF<10>	PCIE_NB2SA10	PCIE_NB_TO_SLOTA_10_F	PCIE_DATA	PCIE_DATA
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82 PCIE_NB_TO_SLOTA_PF<11>	PCIE_NB2SA11	PCIE_NB_TO_SLOTA_11_F	PCIE_DATA	PCIE_DATA
9 82 PCIE_NB_TO_SLOTA_NF<12>	PCIE_NB2SA12	PCIE_NB_TO_SLOTA_12_F	PCIE_DATA	PCIE_DATA
82 PCIE_NB_TO_SLOTA_PF<12>	PCIE_NB2SA12	PCIE_NB_TO_SLOTA_12_F	PCIE_DATA	PCIE_DATA
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82 PCIE_NB_TO_SLOTA_PF<15>	PCIE_NB2SA15	PCIE_NB_TO_SLOTA_15_F	PCIE_DATA	PCIE_DATA
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84 82 PCIE_NB_TO_SLOTA_N<1>		PCIE_NB_TO_SLOTA_1	PCIE_DATA	PCIE_DATA
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84 9 82 PCIE_NB_TO_SLOTA_N<3>		PCIE_NB_TO_SLOTA_3	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_P<3>		PCIE_NB_TO_SLOTA_3	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_N<4>		PCIE_NB_TO_SLOTA_4	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_P<4>		PCIE_NB_TO_SLOTA_4	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_N<5>		PCIE_NB_TO_SLOTA_5	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_P<5>		PCIE_NB_TO_SLOTA_5	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_N<6>		PCIE_NB_TO_SLOTA_6	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_P<6>		PCIE_NB_TO_SLOTA_6	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_N<7>		PCIE_NB_TO_SLOTA_7	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_P<7>		PCIE_NB_TO_SLOTA_7	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_N<8>		PCIE_NB_TO_SLOTA_8	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_P<8>		PCIE_NB_TO_SLOTA_8	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_N<9>		PCIE_NB_TO_SLOTA_9	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_P<9>		PCIE_NB_TO_SLOTA_9	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_N<10>		PCIE_NB_TO_SLOTA_10	PCIE_DATA	PCIE_DATA
84 9 82 PCIE_NB_TO_SLOTA_P<10>		PCIE_NB_TO_SLOTA_10	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_N<11>		PCIE_NB_TO_SLOTA_11	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_P<11>		PCIE_NB_TO_SLOTA_11	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_N<12>		PCIE_NB_TO_SLOTA_12	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_P<12>		PCIE_NB_TO_SLOTA_12	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_N<13>		PCIE_NB_TO_SLOTA_13	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_P<13>		PCIE_NB_TO_SLOTA_13	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_N<14>		PCIE_NB_TO_SLOTA_14	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_P<14>		PCIE_NB_TO_SLOTA_14	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_N<15>		PCIE_NB_TO_SLOTA_15	PCIE_DATA	PCIE_DATA
84 82 PCIE_NB_TO_SLOTA_P<15>		PCIE_NB_TO_SLOTA_15	PCIE_DATA	PCIE_DATA

KODIAK PCI-E POWER PHYSICAL CONSTRAINT TABLE

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
82 6 KOD_G10_GND	0.3MM	0.25MM	0
82 6 KOD_H05_GND	0.3MM	0.25MM	0
82 6 KOD_H08_GND	0.3MM	0.25MM	0
82 6 KOD_J13_GND	0.3MM	0.25MM	0
82 6 KOD_K07_GND	0.3MM	0.25MM	0
82 6 KOD_L13_GND	0.3MM	0.25MM	0
82 PWR_PCIE_A_AVDD	0.3MM	0.25MM	1.2
97 82 PWR_PCIE_A_AVDD_2	0.3MM	0.25MM	1.2
82 PWR_PCIE_A_AVDD_1	0.3MM	0.25MM	1.2
97 82 PWR_PCIE_A_AVDD_0	0.3MM	0.25MM	1.2
82 PWR_PCIE_A_AVDD_A	0.3MM	0.25MM	1.2
82 PWR_PCIE_A_AVDD_B	0.3MM	0.25MM	1.2
82 PWR_PCIE_A_AVDD_C	0.3MM	0.25MM	1.2
97 82 PWR_PCIE_A_AVDD_2	0.3MM	0.25MM	1.2
97 82 PWR_PCIE_A_AVDD_0	0.3MM	0.25MM	1.2

SIG_NAME	ELECTRICAL_CONSTRAINT_SET	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	
84 26 CLK_PCIE_SLOTA_N<0>		KODPCIE_CLK	PCIE_CLK	PCIE_CLK	
84 26 CLK_PCIE_SLOTA_P<0>		KODPCIE_CLK	PCIE_CLK	PCIE_CLK	
84 CLK_PCIE_SLOTA_NF<0>		KODPCIE_CLKF	PCIE_CLK	PCIE_CLK	
84 CLK_PCIE_SLOTA_PF<0>		KODPCIE_CLKF	PCIE_CLK	PCIE_CLK	
9 84 CKA_P<0>		CLK_SLOTA_CKA	PCIE_CLK	PCIE_CLK	
9 84 CKA_N<0>		CLK_SLOTA_CKA	PCIE_CLK	PCIE_CLK	
84 PCIE_SLOTA_TO_NB_NF<0>	PCIE_SA2NB0	PCIE_SLOTA_TO_NB_0_F	PCIE_DATA	PCIE_DATA	8312
84 PCIE_SLOTA_TO_NB_PF<0>	PCIE_SA2NB0	PCIE_SLOTA_TO_NB_0_F	PCIE_DATA	PCIE_DATA	8313
84 PCIE_SLOTA_TO_NB_NF<1>	PCIE_SA2NB1	PCIE_SLOTA_TO_NB_1_F	PCIE_DATA	PCIE_DATA	8311
84 PCIE_SLOTA_TO_NB_PF<1>	PCIE_SA2NB1	PCIE_SLOTA_TO_NB_1_F	PCIE_DATA	PCIE_DATA	8310
84 PCIE_SLOTA_TO_NB_NF<2>	PCIE_SA2NB2	PCIE_SLOTA_TO_NB_2_F	PCIE_DATA	PCIE_DATA	8317
84 PCIE_SLOTA_TO_NB_PF<2>	PCIE_SA2NB2	PCIE_SLOTA_TO_NB_2_F	PCIE_DATA	PCIE_DATA	8314
84 PCIE_SLOTA_TO_NB_NF<3>	PCIE_SA2NB3	PCIE_SLOTA_TO_NB_3_F	PCIE_DATA	PCIE_DATA	8315
84 PCIE_SLOTA_TO_NB_PF<3>	PCIE_SA2NB3	PCIE_SLOTA_TO_NB_3_F	PCIE_DATA	PCIE_DATA	8318
84 PCIE_SLOTA_TO_NB_NF<4>	PCIE_SA2NB4	PCIE_SLOTA_TO_NB_4_F	PCIE_DATA	PCIE_DATA	8319
84 PCIE_SLOTA_TO_NB_PF<4>	PCIE_SA2NB4	PCIE_SLOTA_TO_NB_4_F	PCIE_DATA	PCIE_DATA	8320
84 PCIE_SLOTA_TO_NB_NF<5>	PCIE_SA2NB5	PCIE_SLOTA_TO_NB_5_F	PCIE_DATA	PCIE_DATA	8321
84 PCIE_SLOTA_TO_NB_PF<5>	PCIE_SA2NB5	PCIE_SLOTA_TO_NB_5_F	PCIE_DATA	PCIE_DATA	8322
84 PCIE_SLOTA_TO_NB_NF<6>	PCIE_SA2NB6	PCIE_SLOTA_TO_NB_6_F	PCIE_DATA	PCIE_DATA	8323
84 PCIE_SLOTA_TO_NB_PF<6>	PCIE_SA2NB6	PCIE_SLOTA_TO_NB_6_F	PCIE_DATA	PCIE_DATA	8328
84 PCIE_SLOTA_TO_NB_NF<7>	PCIE_SA2NB7	PCIE_SLOTA_TO_NB_7_F	PCIE_DATA	PCIE_DATA	8329
84 PCIE_SLOTA_TO_NB_PF<7>	PCIE_SA2NB7	PCIE_SLOTA_TO_NB_7_F	PCIE_DATA	PCIE_DATA	8326
84 PCIE_SLOTA_TO_NB_NF<8>	PCIE_SA2NB8	PCIE_SLOTA_TO_NB_8_F	PCIE_DATA	PCIE_DATA	8327
84 PCIE_SLOTA_TO_NB_PF<8>	PCIE_SA2NB8	PCIE_SLOTA_TO_NB_8_F	PCIE_DATA	PCIE_DATA	8324
84 PCIE_SLOTA_TO_NB_NF<9>	PCIE_SA2NB9	PCIE_SLOTA_TO_NB_9_F	PCIE_DATA	PCIE_DATA	8332
84 PCIE_SLOTA_TO_NB_PF<9>	PCIE_SA2NB9	PCIE_SLOTA_TO_NB_9_F	PCIE_DATA	PCIE_DATA	8333
84 PCIE_SLOTA_TO_NB_NF<10>	PCIE_SA2NB10	PCIE_SLOTA_TO_NB_10_F	PCIE_DATA	PCIE_DATA	8334
84 PCIE_SLOTA_TO_NB_PF<10>	PCIE_SA2NB10	PCIE_SLOTA_TO_NB_10_F	PCIE_DATA	PCIE_DATA	8335
84 PCIE_SLOTA_TO_NB_NF<11>	PCIE_SA2NB11	PCIE_SLOTA_TO_NB_11_F	PCIE_DATA	PCIE_DATA	8336
84 PCIE_SLOTA_TO_NB_PF<11>	PCIE_SA2NB11	PCIE_SLOTA_TO_NB_11_F	PCIE_DATA	PCIE_DATA	8337
84 PCIE_SLOTA_TO_NB_NF<12>	PCIE_SA2NB12	PCIE_SLOTA_TO_NB_12_F	PCIE_DATA	PCIE_DATA	8338
84 PCIE_SLOTA_TO_NB_PF<12>	PCIE_SA2NB12	PCIE_SLOTA_TO_NB_12_F	PCIE_DATA	PCIE_DATA	8339
84 PCIE_SLOTA_TO_NB_NF<13>	PCIE_SA2NB13	PCIE_SLOTA_TO_NB_13_F	PCIE_DATA	PCIE_DATA	8340
84 PCIE_SLOTA_TO_NB_PF<13>	PCIE_SA2NB13	PCIE_SLOTA_TO_NB_13_F	PCIE_DATA	PCIE_DATA	8342
84 PCIE_SLOTA_TO_NB_NF<14>	PCIE_SA2NB14	PCIE_SLOTA_TO_NB_14_F	PCIE_DATA	PCIE_DATA	8341
84 PCIE_SLOTA_TO_NB_PF<14>	PCIE_SA2NB14	PCIE_SLOTA_TO_NB_14_F	PCIE_DATA	PCIE_DATA	8340
84 PCIE_SLOTA_TO_NB_NF<15>	PCIE_SA2NB15	PCIE_SLOTA_TO_NB_15_F	PCIE_DATA	PCIE_DATA	8339
84 PCIE_SLOTA_TO_NB_PF<15>	PCIE_SA2NB15	PCIE_SLOTA_TO_NB_15_F	PCIE_DATA	PCIE_DATA	
84 9 82 PCIE_SLOTA_TO_NB_N<0>		PCIE_SLOTA_TO_NB_0	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_P<0>		PCIE_SLOTA_TO_NB_0	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_N<1>		PCIE_SLOTA_TO_NB_1	PCIE_DATA	PCIE_DATA	
84 82 9 PCIE_SLOTA_TO_NB_P<1>		PCIE_SLOTA_TO_NB_1	PCIE_DATA	PCIE_DATA	
82 PCIE_SLOTA_TO_NB_N<2>		PCIE_SLOTA_TO_NB_2	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_P<2>		PCIE_SLOTA_TO_NB_2	PCIE_DATA	PCIE_DATA	
84 82 9 PCIE_SLOTA_TO_NB_N<3>		PCIE_SLOTA_TO_NB_3	PCIE_DATA	PCIE_DATA	
84 82 9 PCIE_SLOTA_TO_NB_P<3>		PCIE_SLOTA_TO_NB_3	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_N<4>		PCIE_SLOTA_TO_NB_4	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_P<4>		PCIE_SLOTA_TO_NB_4	PCIE_DATA	PCIE_DATA	
84 82 9 PCIE_SLOTA_TO_NB_N<5>		PCIE_SLOTA_TO_NB_5	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_P<5>		PCIE_SLOTA_TO_NB_5	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_N<6>		PCIE_SLOTA_TO_NB_6	PCIE_DATA	PCIE_DATA	
84 82 9 PCIE_SLOTA_TO_NB_P<6>		PCIE_SLOTA_TO_NB_6	PCIE_DATA	PCIE_DATA	
82 PCIE_SLOTA_TO_NB_N<7>		PCIE_SLOTA_TO_NB_7	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_P<7>		PCIE_SLOTA_TO_NB_7	PCIE_DATA	PCIE_DATA	
82 PCIE_SLOTA_TO_NB_N<8>		PCIE_SLOTA_TO_NB_8	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_P<8>		PCIE_SLOTA_TO_NB_8	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_N<9>		PCIE_SLOTA_TO_NB_9	PCIE_DATA	PCIE_DATA	
84 82 9 PCIE_SLOTA_TO_NB_P<9>		PCIE_SLOTA_TO_NB_9	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_N<10>		PCIE_SLOTA_TO_NB_10	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_P<10>		PCIE_SLOTA_TO_NB_10	PCIE_DATA	PCIE_DATA	
84 82 9 PCIE_SLOTA_TO_NB_N<11>		PCIE_SLOTA_TO_NB_11	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_P<11>		PCIE_SLOTA_TO_NB_11	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_N<12>		PCIE_SLOTA_TO_NB_12	PCIE_DATA	PCIE_DATA	
84 82 9 PCIE_SLOTA_TO_NB_P<12>		PCIE_SLOTA_TO_NB_12	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_N<13>		PCIE_SLOTA_TO_NB_13	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_P<13>		PCIE_SLOTA_TO_NB_13	PCIE_DATA	PCIE_DATA	
84 82 9 PCIE_SLOTA_TO_NB_N<14>		PCIE_SLOTA_TO_NB_14	PCIE_DATA	PCIE_DATA	
82 PCIE_SLOTA_TO_NB_P<14>		PCIE_SLOTA_TO_NB_14	PCIE_DATA	PCIE_DATA	
84 82 PCIE_SLOTA_TO_NB_N<15>		PCIE_SLOTA_TO_NB_15	PCIE_DATA	PCIE_DATA	
9 82 84 PCIE_SLOTA_TO_NB_P<15>		PCIE_SLOTA_TO_NB_15	PCIE_DATA	PCIE_DATA	

Preliminary

KODIAK PCI-E CONST

SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

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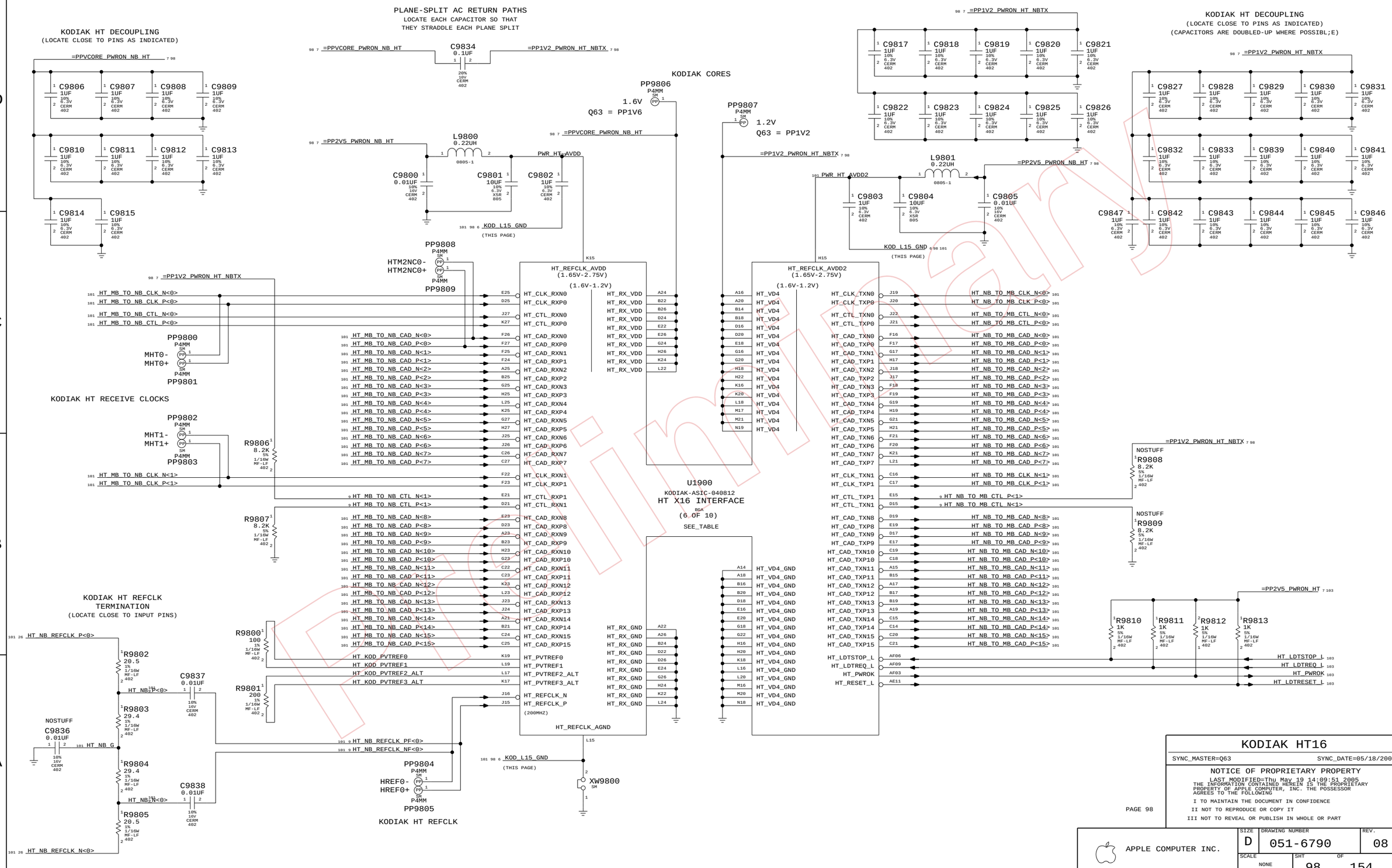
KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)
PLANE-SPLIT AC RETURN PATHS
LOCATE EACH CAPACITOR SO THAT
THEY STRADDLE EACH PLANE SPLIT
KODIAK CORES
KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)
(CAPACITORS ARE DOUBLED-UP WHERE POSSIBL;E)
KODIAK HT RECEIVE CLOCKS
KODIAK HT REFCLK
TERMINATION
(LOCATE CLOSE TO INPUT PINS)
KODIAK HT REFCLK
U1900
KODIAK-ASIC-040812
HT X16 INTERFACE
BGA
(6 OF 10)
SEE_TABLE
HT_REFCLK_AVDD
(1.65V-2.75V)
(1.6V-1.2V)
HT_REFCLK_AVDD2
(1.65V-2.75V)
(1.6V-1.2V)
HT_REFCLK_AGND
(200MHZ)
KOD_L15_GND
(THIS PAGE)
=PPVCORE_PWRON_NB_HT
=PP1V2_PWRON_HT_NBTX
=PP2V5_PWRON_NB_HT
=PP2V5_PWRON_HT
PWR_HT_AVDD
PWR_HT_AVDD2
1.6V
Q63 = PP1V6
1.2V
Q63 = PP1V2
NOSTUFF
XW9800
SM
PAGE 98
KODIAK HT16
SYNC_MASTER=Q63
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SHT
98
OF
154
DRAWING

	SIG_NAME	MAKE_BASE	DIFFERENTIAL_PAIR	EC_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE		
98C3 HT_NB_TO_MB_CLK_N<0>	HT_NB_TO_SB_CLK_N<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CLK	HT_MB_TO_SB_CLK_N<0>	103C6
98C3 HT_NB_TO_MB_CLK_P<0>	HT_NB_TO_SB_CLK_P<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CLK	HT_MB_TO_SB_CLK_P<0>	103C6
98C3 HT_NB_TO_MB_CAD_N<0>	HT_NB_TO_SB_CAD_N<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<0>	103C6
98C3 HT_NB_TO_MB_CAD_P<0>	HT_NB_TO_SB_CAD_P<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<0>	103C6
98C3 HT_NB_TO_MB_CAD_N<1>	HT_NB_TO_SB_CAD_N<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<1>	103C6
98C3 HT_NB_TO_MB_CAD_P<1>	HT_NB_TO_SB_CAD_P<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<1>	103C6
98C3 HT_NB_TO_MB_CAD_N<2>	HT_NB_TO_SB_CAD_N<2>	TRUE	HT_NB_TO_SB_CAD2	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<2>	103B6
98C3 HT_NB_TO_MB_CAD_P<2>	HT_NB_TO_SB_CAD_P<2>	TRUE	HT_NB_TO_SB_CAD2	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<2>	103B6
98C3 HT_NB_TO_MB_CAD_N<3>	HT_NB_TO_SB_CAD_N<3>	TRUE	HT_NB_TO_SB_CAD3	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<3>	103B6
98C3 HT_NB_TO_MB_CAD_P<3>	HT_NB_TO_SB_CAD_P<3>	TRUE	HT_NB_TO_SB_CAD3	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<3>	103B6
98C3 HT_NB_TO_MB_CAD_N<4>	HT_NB_TO_SB_CAD_N<4>	TRUE	HT_NB_TO_SB_CAD4	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<4>	103B6
98B3 HT_NB_TO_MB_CAD_P<4>	HT_NB_TO_SB_CAD_P<4>	TRUE	HT_NB_TO_SB_CAD4	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<4>	103B6
98B3 HT_NB_TO_MB_CAD_N<5>	HT_NB_TO_SB_CAD_N<5>	TRUE	HT_NB_TO_SB_CAD5	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<5>	103B6
98B3 HT_NB_TO_MB_CAD_P<5>	HT_NB_TO_SB_CAD_P<5>	TRUE	HT_NB_TO_SB_CAD5	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<5>	103B6
98B3 HT_NB_TO_MB_CAD_N<6>	HT_NB_TO_SB_CAD_N<6>	TRUE	HT_NB_TO_SB_CAD6	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<6>	103B6
98B3 HT_NB_TO_MB_CAD_P<6>	HT_NB_TO_SB_CAD_P<6>	TRUE	HT_NB_TO_SB_CAD6	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<6>	103B6
98B3 HT_NB_TO_MB_CAD_N<7>	HT_NB_TO_SB_CAD_N<7>	TRUE	HT_NB_TO_SB_CAD7	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<7>	103B6
98B3 HT_NB_TO_MB_CAD_P<7>	HT_NB_TO_SB_CAD_P<7>	TRUE	HT_NB_TO_SB_CAD7	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<7>	103B6
98C3 HT_NB_TO_MB_CTL_N<0>	HT_NB_TO_SB_CTL_N<0>	TRUE	HT_NB_TO_SB_CTL0	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CTL_N<0>	103B6
98C3 HT_NB_TO_MB_CTL_P<0>	HT_NB_TO_SB_CTL_P<0>	TRUE	HT_NB_TO_SB_CTL0	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CTL_P<0>	103B6
98C8 HT_MB_TO_NB_CLK_N<0>	HT_SB_TO_NB_CLK_N<0>	TRUE	HT_SB_TO_NB_CLK	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CLK	HT_SB_TO_MB_CLK_N<0>	103C3
98C8 HT_MB_TO_NB_CLK_P<0>	HT_SB_TO_NB_CLK_P<0>	TRUE	HT_SB_TO_NB_CLK	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CLK	HT_SB_TO_MB_CLK_P<0>	103C3
98C6 HT_MB_TO_NB_CAD_N<0>	HT_SB_TO_NB_CAD_N<0>	TRUE	HT_SB_TO_NB_CAD0	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<0>	103C3
98C6 HT_MB_TO_NB_CAD_P<0>	HT_SB_TO_NB_CAD_P<0>	TRUE	HT_SB_TO_NB_CAD0	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<0>	103C3
98C6 HT_MB_TO_NB_CAD_N<1>	HT_SB_TO_NB_CAD_N<1>	TRUE	HT_SB_TO_NB_CAD1	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<1>	103C3
98C6 HT_MB_TO_NB_CAD_P<1>	HT_SB_TO_NB_CAD_P<1>	TRUE	HT_SB_TO_NB_CAD1	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<1>	103C3
98C6 HT_MB_TO_NB_CAD_N<2>	HT_SB_TO_NB_CAD_N<2>	TRUE	HT_SB_TO_NB_CAD2	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<2>	103B3
98C6 HT_MB_TO_NB_CAD_P<2>	HT_SB_TO_NB_CAD_P<2>	TRUE	HT_SB_TO_NB_CAD2	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<2>	103B3
98C6 HT_MB_TO_NB_CAD_N<3>	HT_SB_TO_NB_CAD_N<3>	TRUE	HT_SB_TO_NB_CAD3	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<3>	103B3
98C6 HT_MB_TO_NB_CAD_P<3>	HT_SB_TO_NB_CAD_P<3>	TRUE	HT_SB_TO_NB_CAD3	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<3>	103B3
98C6 HT_MB_TO_NB_CAD_N<4>	HT_SB_TO_NB_CAD_N<4>	TRUE	HT_SB_TO_NB_CAD4	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<4>	103B3
98B6 HT_MB_TO_NB_CAD_P<4>	HT_SB_TO_NB_CAD_P<4>	TRUE	HT_SB_TO_NB_CAD4	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<4>	103B3
98B6 HT_MB_TO_NB_CAD_N<5>	HT_SB_TO_NB_CAD_N<5>	TRUE	HT_SB_TO_NB_CAD5	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<5>	103B3
98B6 HT_MB_TO_NB_CAD_P<5>	HT_SB_TO_NB_CAD_P<5>	TRUE	HT_SB_TO_NB_CAD5	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<5>	103B3
98B6 HT_MB_TO_NB_CAD_N<6>	HT_SB_TO_NB_CAD_N<6>	TRUE	HT_SB_TO_NB_CAD6	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<6>	103B3
98B6 HT_MB_TO_NB_CAD_P<6>	HT_SB_TO_NB_CAD_P<6>	TRUE	HT_SB_TO_NB_CAD6	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<6>	103B3
98B6 HT_MB_TO_NB_CAD_N<7>	HT_SB_TO_NB_CAD_N<7>	TRUE	HT_SB_TO_NB_CAD7	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<7>	103B3
98B6 HT_MB_TO_NB_CAD_P<7>	HT_SB_TO_NB_CAD_P<7>	TRUE	HT_SB_TO_NB_CAD7	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<7>	103B3
98C8 HT_MB_TO_NB_CTL_N<0>	HT_SB_TO_NB_CTL_N<0>	TRUE	HT_SB_TO_NB_CTL0	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CTL_N<0>	103B3
98C8 HT_MB_TO_NB_CTL_P<0>	HT_SB_TO_NB_CTL_P<0>	TRUE	HT_SB_TO_NB_CTL0	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CTL_P<0>	103B3
6B7 NC_HT_MB_TO_NB_CAD_P<8..15>		TRUE					HT_MB_TO_NB_CAD_P<8..15>	98A6 98B6
6B7 NC_HT_MB_TO_NB_CAD_N<8..15>		TRUE					HT_MB_TO_NB_CAD_N<8..15>	98A6 98B6
9C7 TP_HT_MB_TO_NB_CLK_N<1>		TRUE					HT_MB_TO_NB_CLK_N<1>	98B8
9C7 TP_HT_MB_TO_NB_CLK_P<1>		TRUE					HT_MB_TO_NB_CLK_P<1>	98B8
						I97		
6B7 NC_HT_NB_TO_MB_CAD_P<8..15>		TRUE					HT_NB_TO_MB_CAD_P<8..15>	98A3 98B3
6B7 NC_HT_NB_TO_MB_CAD_N<8..15>		TRUE					HT_NB_TO_MB_CAD_N<8..15>	98A3 98B3
6B7 NC_HT_NB_TO_MB_CLK_N<1>		TRUE					HT_NB_TO_MB_CLK_N<1>	98B3
6B7 NC_HT_NB_TO_MB_CLK_P<1>		TRUE					HT_NB_TO_MB_CLK_P<1>	98B3
98A8 26C2 HT_NB_REFCLK_P<0>			HT_NB_REFCLK0	HT_NB_REFCLK	HT_CLK	HT_CLK	IN	
98A8 26C2 HT_NB_REFCLK_N<0>			HT_NB_REFCLK0		HT_CLK	HT_CLK	IN	
98A8 HT_NB_P<0>			HT_NB0		HT_CLK	HT_CLK	IN	
98A8 HT_NB_N<0>			HT_NB0		HT_CLK	HT_CLK	IN	
98A6 HT_NB_REFCLK_PF<0>			HT_NB_REFCLK_F0		HT_CLK	HT_CLK	IN	
98A6 HT_NB_REFCLK_NF<0>			HT_NB_REFCLK_F0		HT_CLK	HT_CLK	IN	

	SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE	
98D5	PWR_HT_AVDD	0.4MM	0.2MM	2.5	IN
98D4	PWR_HT_AVDD2	0.4MM	0.2MM	2.5	IN
98C6 98C3 98A6 6D6	KOD_L15_GND	0.4MM	0.2MM	0	IN
98A8	HT_NB_G KEEP DIFF CLOCK FROM BEING A SINGLE XNET			0	IN

Preliminary

HT ALIASES

FINO-EG 05/18/2005

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 101 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	0.38mm SPACING	
HT_CLK66M_SB	0.38mm SPACING	
	P3MM SPACING	

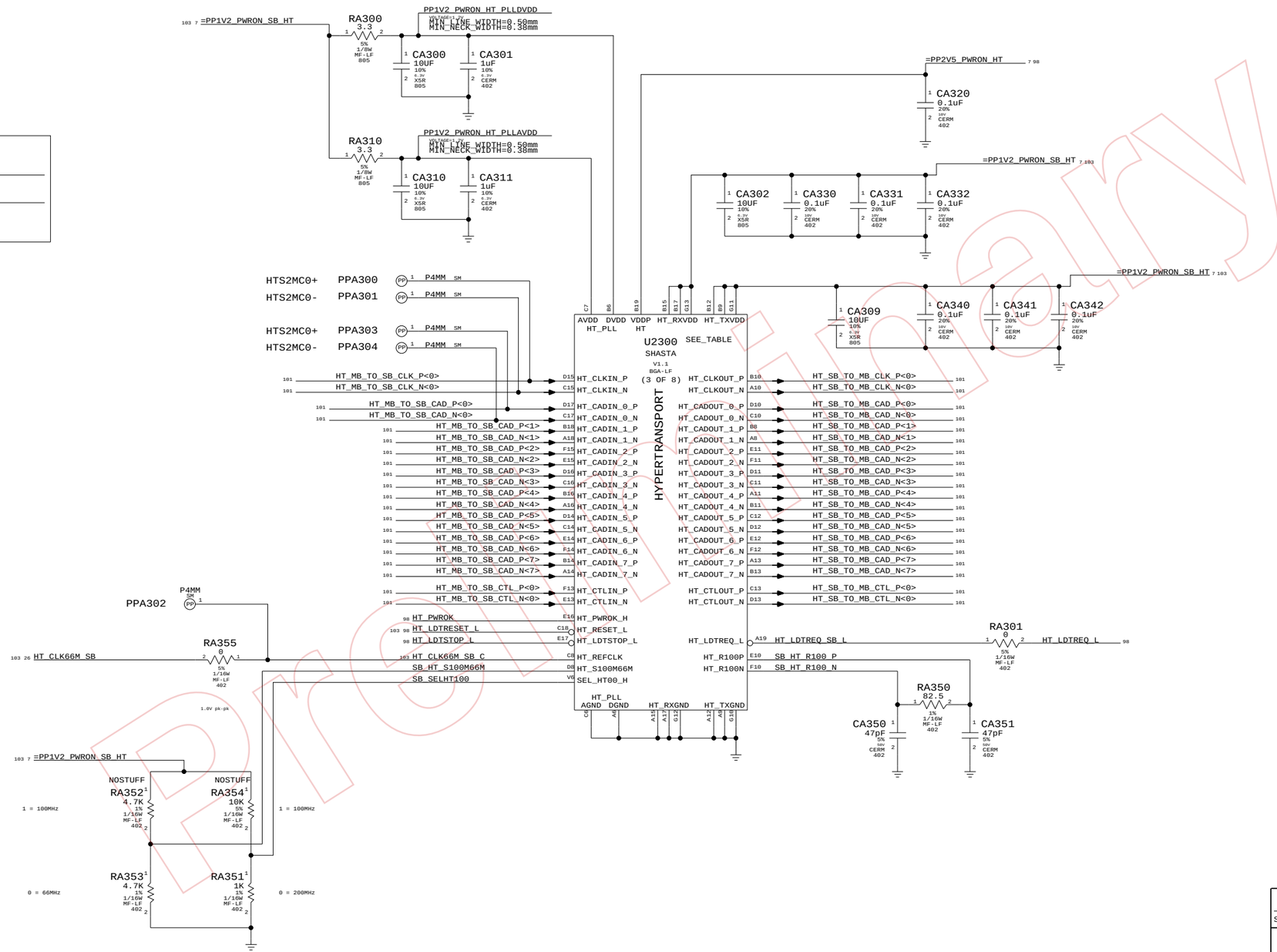
HT_CLK66M_SB_C 103
HT_CLK66M_SB 26 103
HT_LDTRESET_L 98 103

Page Notes

Power aliases required by this page:
=PP2V5_PWRON_HT
=PP1V2_PWRON_HT

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SB_HT_200M
  Stuffs resistor to select 200MHz HT I/F.



HT Refclk	HT I/F Speed
1 = 100MHz	1 = 100MHz
0 = 66MHz	0 = 200MHz

DETERMINES THE OPERATING FREQUENCY OF HT CORE
1: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 100 MHZ
0: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 200 MHZ

Preliminary

Shasta HyperTransport

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 103 OF 154	

LAST_MODIFIED=Thu May 19 14:08:29 2005
DRAWING
TITLE=K13LOWMA
ABBREV=YORKWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
		PCI_AD<31..28>	120 121 122 125
		PCI_AD<27>	120 121 122 125
		PCI_AD<26..24>	120 121 122 125
		PCI_AD<23>	120 121 122
		PCI_AD<22>	120 121 122
		PCI_AD<21>	120 121 122
		PCI_AD<20>	120 121 122 125
		PCI_AD<19..18>	120 121 122 125
		PCI_AD<17>	120 121 122 125
		PCI_AD<16..0>	120 121 122 125
		PCI_CBE_L<3..0>	120 121 122
		PCI_PAR	120 121 122
		PCI_DEVSEL_L	119 120 121 122
		PCI_FRAME_L	119 120 121 122
		PCI_IRDY_L	119 120 121 122
		PCI_TRDY_L	119 120 121 122
		PCI_STOP_L	119 120 121 122
1183	P3MM_SPACING	PCI_CLK66M_SB_INT	26 27 119

Q63 APPLICATION OF POWER NET "=PP3V3_SB_PCI" IS RUN

Page Notes

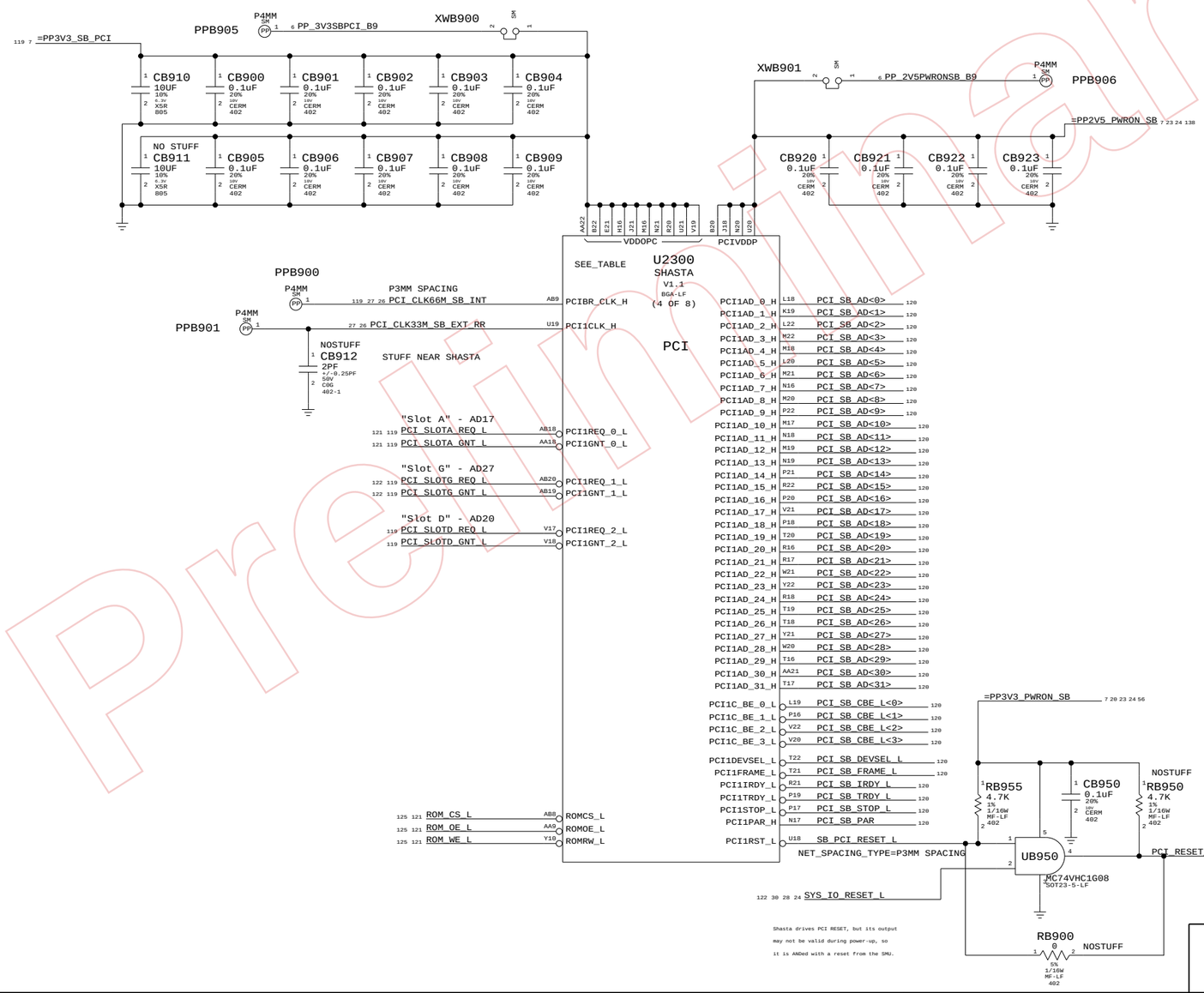
Power aliases required by this page:
- =PP3V3_PCI
- =PP3V3_SB_PCI (CAN BE _PP3V3_PCI)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)



Shasta PCI Interface

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 119	OF 154

LAST_MODIFIED=Thu May 19 14:08:34 2005

DRAWING

TITLE=K13LOWNWA

ABBREV=YORKWING

Preliminary

ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)

119	PCI_SB_AD<0>	RPC003	4	5	47	PCI_AD<0>	119 121 122 125
119	PCI_SB_AD<1>	RPC003	1	8	47	PCI_AD<1>	119 121 122 125
119	PCI_SB_AD<2>	RPC009	1	8	47	PCI_AD<2>	119 121 122 125
119	PCI_SB_AD<3>	RPC001	3	6	47	PCI_AD<3>	119 121 122 125
119	PCI_SB_AD<4>	RPC000	3	6	47	PCI_AD<4>	119 121 122 125
119	PCI_SB_AD<5>	RPC003	2	7	47	PCI_AD<5>	119 121 122 125
119	PCI_SB_AD<6>	RPC001	4	5	47	PCI_AD<6>	119 121 122 125
119	PCI_SB_AD<7>	RPC000	2	7	47	PCI_AD<7>	119 121 122 125
119	PCI_SB_AD<8>	RPC007	4	5	47	PCI_AD<8>	119 121 122 125
119	PCI_SB_AD<9>	RPC002	1	8	47	PCI_AD<9>	119 121 122 125
119	PCI_SB_AD<10>	RPC000	1	8	47	PCI_AD<10>	119 121 122 125
119	PCI_SB_AD<11>	RPC009	3	6	47	PCI_AD<11>	119 121 122 125
119	PCI_SB_AD<12>	RPC000	4	5	47	PCI_AD<12>	119 121 122 125
119	PCI_SB_AD<13>	RPC009	4	5	47	PCI_AD<13>	119 121 122 125
119	PCI_SB_AD<14>	RPC002	2	7	47	PCI_AD<14>	119 121 122 125
119	PCI_SB_AD<15>	RPC002	4	5	47	PCI_AD<15>	119 121 122 125
119	PCI_SB_AD<16>	RPC002	3	6	47	PCI_AD<16>	119 121 122 125

RC000

119	PCI_SB_AD<17>		1	2	47 5% 1/16W MF-LF 402	PCI_AD<17>	119 121 122 125

119	PCI_SB_AD<18>	RPC007	1	8	47	PCI_AD<18>	119 121 122 125
119	PCI_SB_AD<19>	RPC006	2	7	47	PCI_AD<19>	119 121 122 125
119	PCI_SB_AD<20>	RPC007	2	7	47	PCI_AD<20>	119 121 122 125
119	PCI_SB_AD<21>	RPC008	1	8	47	PCI_AD<21>	119 121 122
119	PCI_SB_AD<22>	RPC004	1	8	47	PCI_AD<22>	119 121 122
119	PCI_SB_AD<23>	RPC006	4	5	47	PCI_AD<23>	119 121 122
119	PCI_SB_AD<24>	RPC008	4	5	47	PCI_AD<24>	119 121 122 125
119	PCI_SB_AD<25>	RPC006	3	6	47	PCI_AD<25>	119 121 122 125
119	PCI_SB_AD<26>	RPC008	3	6	47	PCI_AD<26>	119 121 122 125

RC001

119	PCI_SB_AD<27>		1	2	47 5% 1/16W MF-LF 402	PCI_AD<27>	119 121 122 125

119	PCI_SB_AD<28>	RPC004	4	5	47	PCI_AD<28>	119 121 122 125
119	PCI_SB_AD<29>	RPC008	2	7	47	PCI_AD<29>	119 121 122 125
119	PCI_SB_AD<30>	RPC004	2	7	47	PCI_AD<30>	119 121 122 125
119	PCI_SB_AD<31>	RPC007	3	6	47	PCI_AD<31>	119 121 122 125
119	PCI_SB_CBE_L<0>	RPC003	3	6	47	PCI_CBE_L<0>	119 121 122
119	PCI_SB_CBE_L<1>	RPC001	1	8	47	PCI_CBE_L<1>	119 121 122
119	PCI_SB_CBE_L<2>	RPC006	1	8	47	PCI_CBE_L<2>	119 121 122
119	PCI_SB_CBE_L<3>	RPC004	3	6	47	PCI_CBE_L<3>	119 121 122
119	PCI_SB_DEVSEL_L	RPC005	3	6	47	PCI_DEVSEL_L	119 121 122
119	PCI_SB_FRAME_L	RPC005	4	5	47	PCI_FRAME_L	119 121 122
119	PCI_SB_IRDY_L	RPC005	2	7	47	PCI_IRDY_L	119 121 122
119	PCI_SB_TRDY_L	RPC005	1	8	47	PCI_TRDY_L	119 121 122
119	PCI_SB_STOP_L	RPC001	2	7	47	PCI_STOP_L	119 121 122
119	PCI_SB_PAR	RPC009	2	7	47	PCI_PAR	119 121 122

PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB

Preliminary

PCI SERIES TERMINATION

SYNC_MASTER=FINO-EG SYNC_DATE=05/18/2005

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 120 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	

PCI_CLK33M_AIRPORT 26 121

Page Notes

Power aliases required by this page:
- _PP3V3_PCI

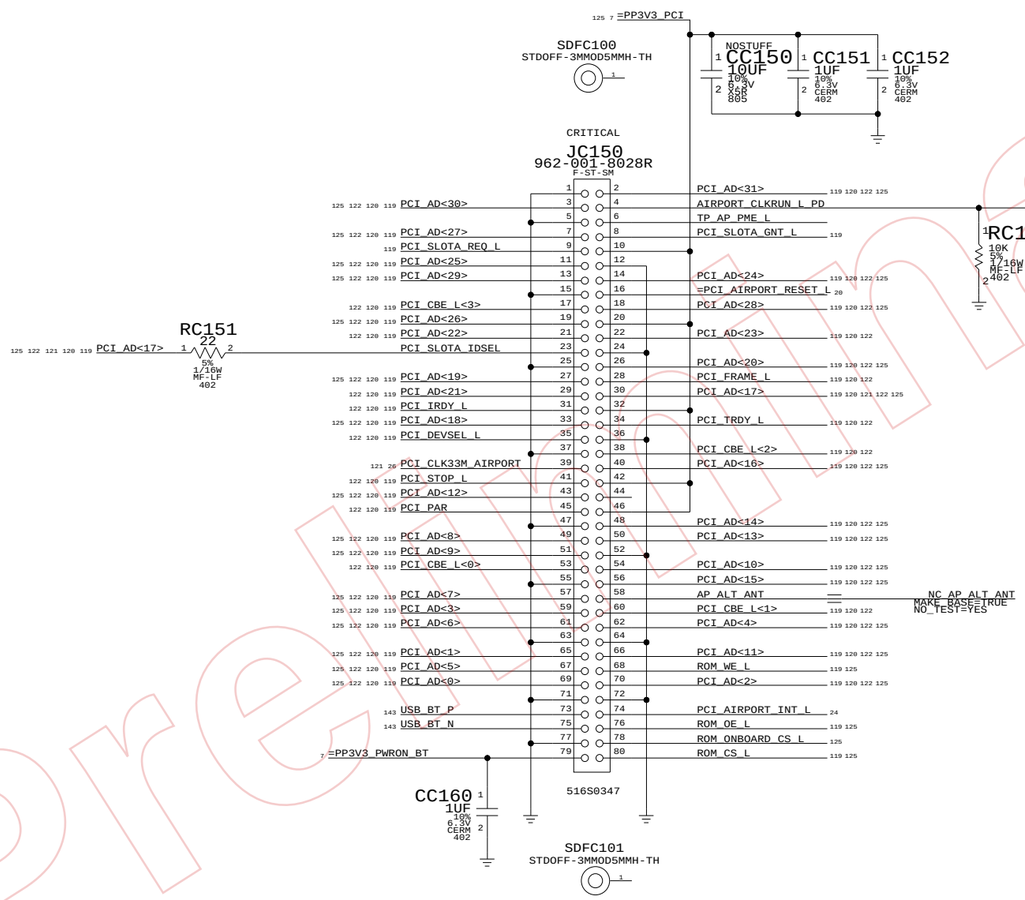
Signal aliases required by this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

Q85 WIRELESS CONNECTOR



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AIRPORT & BLUETOOTH

SYNC_MASTER=FINO-EG SYNC_DATE=05/18/2005

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 121 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	CLOCKS	

=PCI_CLK33M_USB2 27 122

Page Notes

Power aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

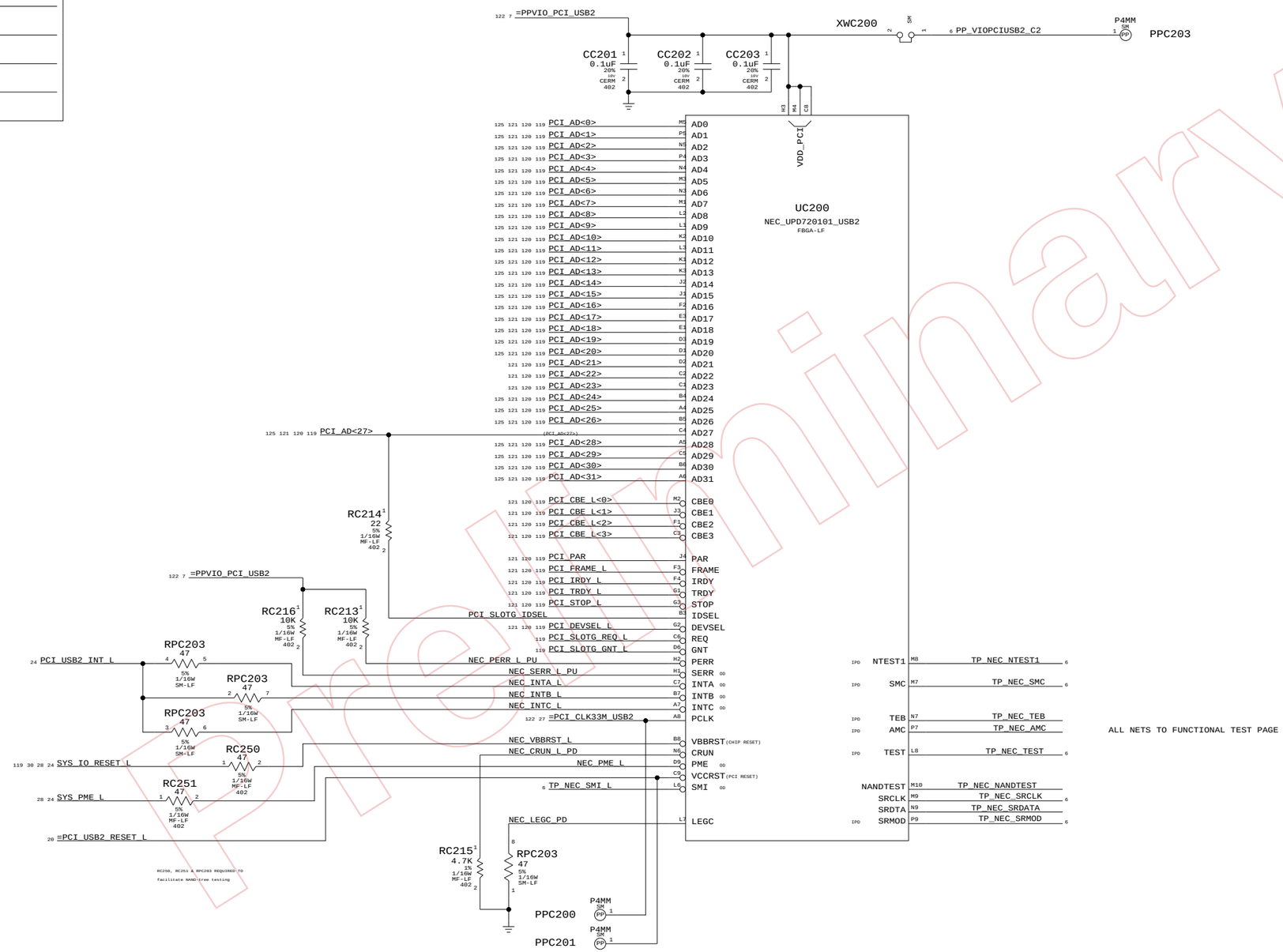
Signal aliases required by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports
D3cold.

Q63 APPLICATION OF POWER NET "=PPVIO_PCI_USB2" IS PP3V3_RUN



ALL NETS TO FUNCTIONAL TEST PAGE

Preliminary

USB 2.0 PCI Interface

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 122 OF 154	

LAST_MODIFIED=Thu May 19 14:08:36 2005

DRAWING

TITLE=X01e0000

ABBREV=D0NAD0A5

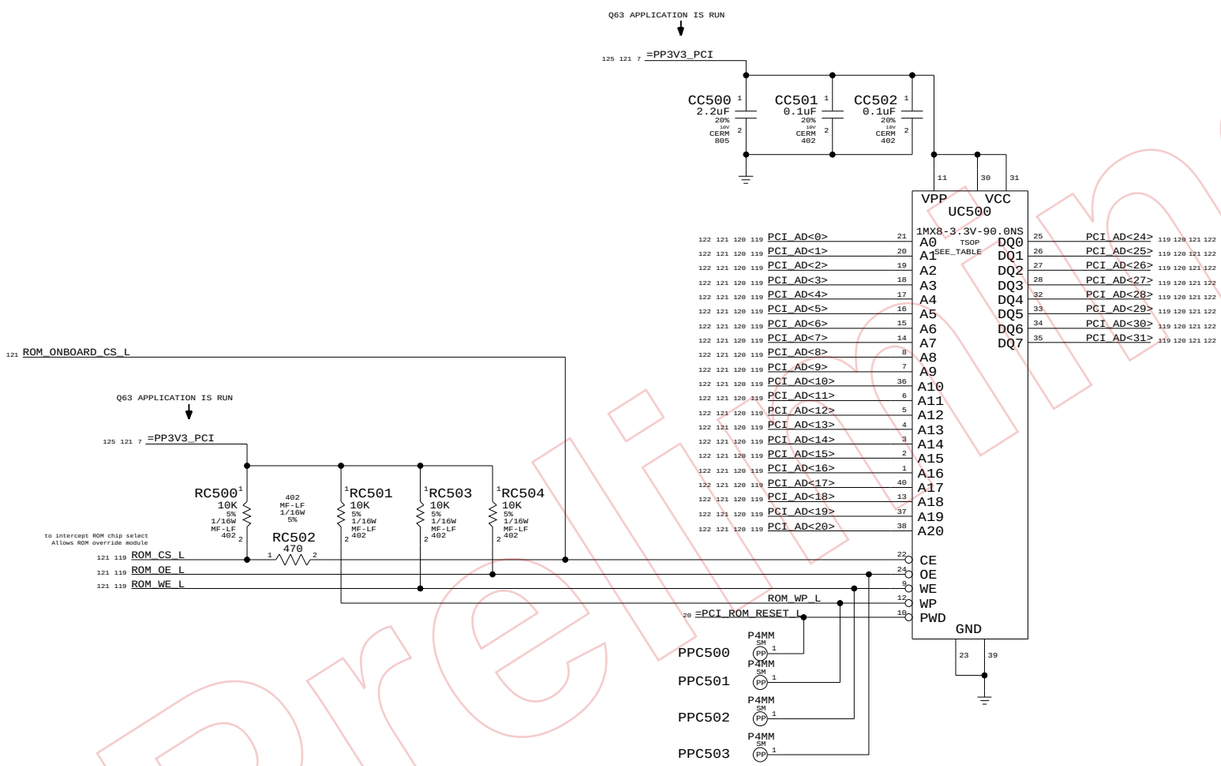
Page Notes

Power aliases required by this page:
- =PP3V3_PCI

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.



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BootROM

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

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APPLE COMPUTER INC.

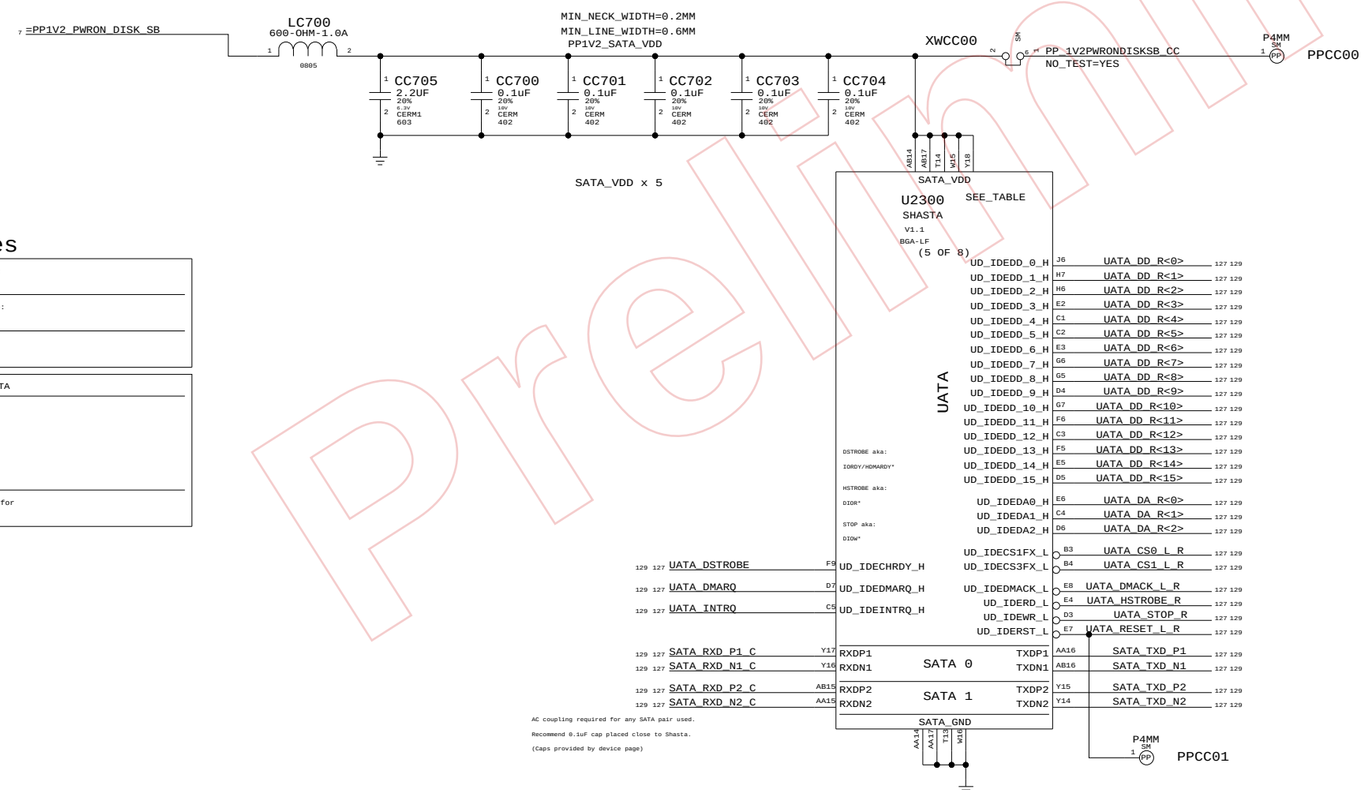
SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 125	OF 154

LAST_MODIFIED=Thu May 19 14:08:37 2005

DRAWING
TITLE=MILDWWA
ABBREV=ROMWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	SATA	SATA	SATA_RXD1_C	SATA_RXD_P1_C 127 129
	SATA	SATA	SATA_RXD1_C	SATA_RXD_N1_C 127 129
	SATA	SATA	SATA_TXD1	SATA_TXD_P1 127 129
	SATA	SATA	SATA_TXD1	SATA_TXD_N1 127 129
	SATA	SATA	SATA_RXD2_C	SATA_RXD_P2_C 127 129
	SATA	SATA	SATA_RXD2_C	SATA_RXD_N2_C 127 129
	SATA	SATA	SATA_TXD2	SATA_TXD_P2 127 129
	SATA	SATA	SATA_TXD2	SATA_TXD_N2 127 129
				UATA_DD<15..8> 9 127 129
				UATA_DD<7> 127 129
				UATA_DD<6..0> 9 127 129
				UATA_DA<2..0> 9 127 129
				UATA_CS0_L 127 129
				UATA_CS1_L 127 129
				UATA_HSTROBE 127 129
				UATA_STOP 127 129
				UATA_DMACK_L 127 129
	UATA_NETSPA			UATA_RESET_L 127 129
				UATA_DSTROBE 127 129
				UATA_DMARQ 127 129
				UATA_INTRQ 127 129
127				UATA_DD_R<15..8> 127 129
127				UATA_DD_R<7> 127 129
127				UATA_DD_R<6..0> 127 129
127				UATA_DA_R<2..0> 127 129
127				UATA_CS0_L_R 127 129
127				UATA_CS1_L_R 127 129
127				UATA_DMACK_L_R 127 129
127				UATA_HSTROBE_R 127 129
127				UATA_STOP_R 127 129
127				UATA_RESET_L_R 127 129

PLACE TERMINATION RESISTORS AT UATA CONNECTOR JC901



Page Notes

Power aliases required by this page:
- _PP1V2_PWRON_DISK

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: SATA

Line To Line:	0.38mm
Length Tolerance:	1.27mm
Primary Max Sep:	0.25mm outer
Primary Max Sep:	0.23mm inner
Secondary Max Sep:	2.54mm
Secondary Length:	12.70mm

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

Preliminary

Shasta Disk

SYNC_MASTER=M23-MB SYNC_DATE=05/18/2005

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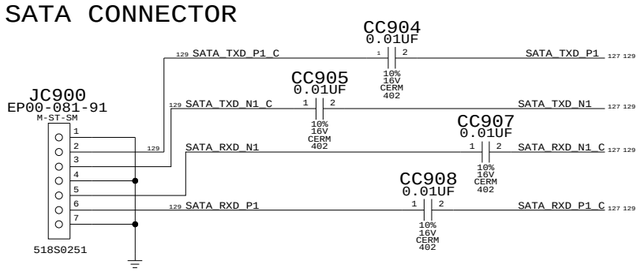
SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 127 OF 154	

LAST_MODIFIED=Thu May 19 14:08:37 2005

DRAWING
TITLE=M23LOANA
ABBREV=SHANANG

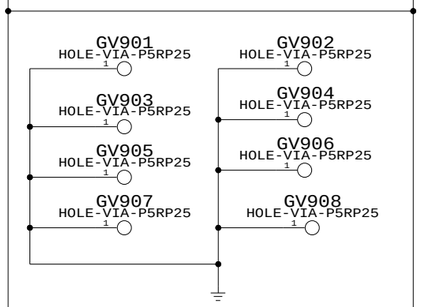
SATA CONNECTOR



SATA PORT1 IS NOT USED IN M23/M33:NO TEST

SATA_TXD_P2	NC_SATA_TXD_P2	MAKE_BASE=TRUE
SATA_TXD_N2	NC_SATA_TXD_N2	MAKE_BASE=TRUE
SATA_RXD_N2_C	NC_SATA_RXD_N2_C	MAKE_BASE=TRUE
SATA_RXD_P2_C	NC_SATA_RXD_P2_C	MAKE_BASE=TRUE

SATA DIFF PAIR GND VIAS



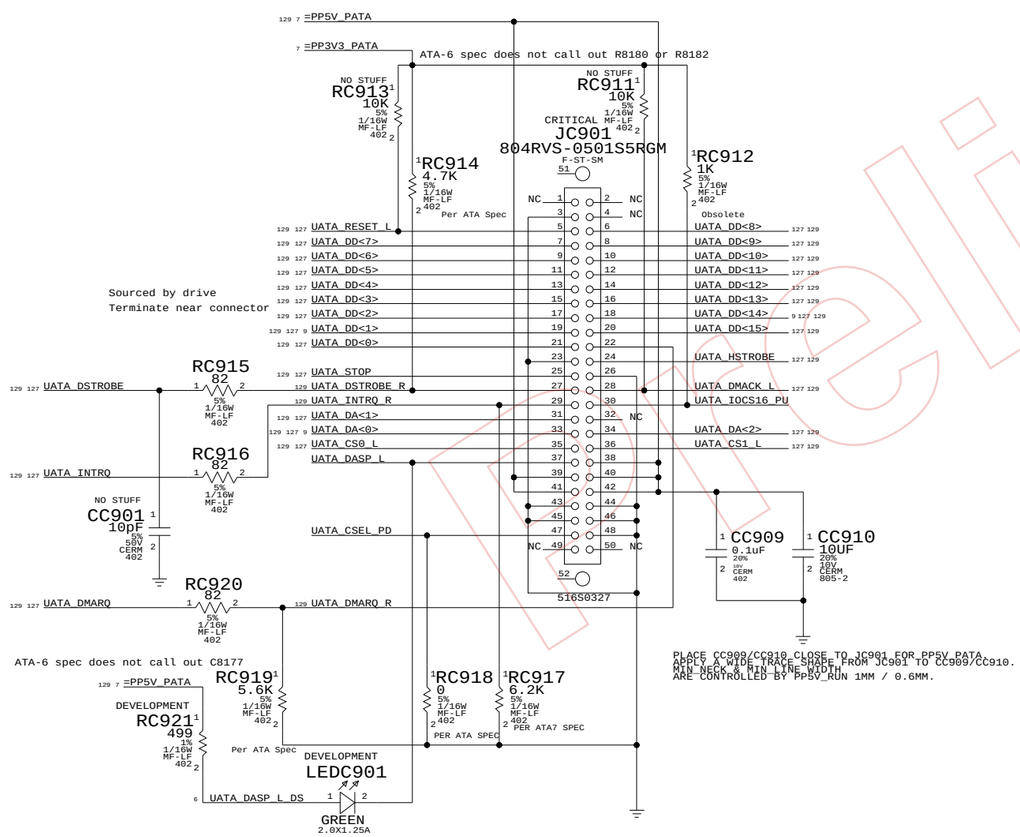
4-12-05
ADD THESE GROUND VIAS NEAR
EACH LAYER JUMP FOR THE SATA
DIFF PAIRS. ONE GND VIA PER
SIGNAL VIA, AND PLACE GND VIA
NO CLOSER THAN 0.152MM TO
SIGNAL VIA.

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NO_TEST
UATA FROM RPAKS TO JC901					
UATA_DD<15..8>	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_DD<7>	UATA_DD7	UATA_NETPH	UATA_NETSPA		
UATA_DD<6..0>	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_DA<2..0>	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_CS0_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_CS1_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_HSTROBE	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_STOP	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_DMACK_L	UATA_HOST_R	UATA_NETPH	UATA_NETSPA		
UATA_RESET_L	UATA_RESET_L	UATA_NETPH	UATA_NETSPA		
UATA_DSTROBE_R	UATA_DEV_R_C	UATA_NETPH	UATA_NETSPA		
UATA_DMARQ_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		
UATA_INTRQ_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		
UATA FROM SHASTA U2300 TO RPAKS					
UATA_DD_R<15..8>		UATA_NETPH	UATA_NETSPA		
UATA_DD_R<7>		UATA_NETPH	UATA_NETSPA		
UATA_DD_R<6..0>		UATA_NETPH	UATA_NETSPA		
UATA_DA_R<2..0>		UATA_NETPH	UATA_NETSPA		
UATA_CS0_L_R		UATA_NETPH	UATA_NETSPA		
UATA_CS1_L_R		UATA_NETPH	UATA_NETSPA		
UATA_HSTROBE_R		UATA_NETPH	UATA_NETSPA		
UATA_STOP_R		UATA_NETPH	UATA_NETSPA		
UATA_DMACK_L_R		UATA_NETPH	UATA_NETSPA		
UATA_RESET_L_R		UATA_NETPH	UATA_NETSPA		
UATA_DSTROBE		UATA_NETPH	UATA_NETSPA		
UATA_DMARQ		UATA_NETPH	UATA_NETSPA		
UATA_INTRQ		UATA_NETPH	UATA_NETSPA		
SATA_TXD_P1	SATA_TXD1	SATA	SATA		TRUE
SATA_TXD_N1	SATA_TXD1	SATA	SATA		TRUE
SATA_TXD_P1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
SATA_TXD_N1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
SATA_RXD_N1_C	SATA_RXD1	SATA	SATA		TRUE
SATA_RXD_P1_C	SATA_RXD1	SATA	SATA		TRUE
SATA_RXD_N1	SATA_RXD1	SATA	SATA	RX1C	TRUE
SATA_RXD_P1	SATA_RXD1	SATA	SATA	RX1C	TRUE

4-11-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGMENT ALREADY FOR SATA DIFF PAIRS (CAP TO SHASTA).
BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.

UATA TRACE IMPEDANCE ROUTE TO 50 OHMS

PATA CONNECTOR



4-8-05
NOTES FOR SHARED PAGE 127
FOR M23/M33 CREATE A WIDE SHAPE
FOR PP1V2_SATA_VDD AND THEN NECK DOWN
TO THE DEFAULT VALUE WHEN NECESSARY.
THE WIDTH/NECK PROPERTIES ON PAGE 127
ARE SET BY Q63 FOR SCHEMATIC SHARING.

LC700 CHANGED TO 155S0240 (600 OHM,0.2 OHM DCR,1A)
PREVIOUS ONE WAS 155S0031 (600 OHM,0.6 OHM DCR,0.2A)
PER TOKIN AMERICA PN: N2012Z601.

4-11-05.
PP1V2_ALL REG. IS SET TO BE 1.22V TO 1.23V
AS NOTED ON THE 1.2 REG PAGE 13. THIS WILL
HELP MITIGATE THE LOSS ACROSS THE Q1306 FET
SI3326DV.

4-12-05.
UPDATED AC COUPLING CAPS FOR SATA JC900.
ADDED DECOUPLING CAPS FOR JC901 PP5V_PATA NET.

Disk Connectors

SYNC_MASTER=M23-MB SYNC_DATE=05/18/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 129 OF 154	

PLACE THESE SERIES TERM CLOSE TO DRIVER: SB/SHASTA

SHASTA -> VESTA

131 9	ENET_TXD_R<0>	I59	MAKE_BASE=TRUE	ENET_TXD<0>	9 131 132
131 9	ENET_TXD_R<1>	I60	MAKE_BASE=TRUE	ENET_TXD<1>	9 131 132
131 9	ENET_TXD_R<2>	I61	MAKE_BASE=TRUE	ENET_TXD<2>	9 131 132
131 9	ENET_TXD_R<3>	I62	MAKE_BASE=TRUE	ENET_TXD<3>	9 131 132
131 9	ENET_TXD_R<4>	I63	MAKE_BASE=TRUE	ENET_TXD<4>	9 131 132
131 9	ENET_TXD_R<5>	I64	MAKE_BASE=TRUE	ENET_TXD<5>	9 131 132
131 9	ENET_TXD_R<6>	I65	MAKE_BASE=TRUE	ENET_TXD<6>	9 131 132
131 9	ENET_TXD_R<7>	I66	MAKE_BASE=TRUE	ENET_TXD<7>	9 131 132
131 9	ENET_TX_EN_R	I67	MAKE_BASE=TRUE	ENET_TX_EN	9 131 132
131 9	ENET_TX_ER_R	I68	MAKE_BASE=TRUE	ENET_TX_ER	9 131 132
131	ENET_CLK125M_GTX_R	I69	MAKE_BASE=TRUE	ENET_CLK125M_GTX	131 132
131	ENET_MDIO_R		MAKE_BASE=TRUE	ENET_MDIO	131 132

PLACE THESE SERIES TERM CLOSE TO DRIVER: VESTA

VESTA -> SHASTA

132	ENET_CLK125M_GBE_REF_R	I84	MAKE_BASE=TRUE	ENET_CLK125M_GBE_REF	131
132	ENET_CLK25M_TX_R	I70	MAKE_BASE=TRUE	ENET_CLK25M_TX	131
132	ENET_CLK125M_RX_R	I71	MAKE_BASE=TRUE	ENET_CLK125M_RX	131
132 131 9	ENET_RXD_R<0>	I72	MAKE_BASE=TRUE	ENET_RXD<0>	9 131
132 131 9	ENET_RXD_R<1>	I73	MAKE_BASE=TRUE	ENET_RXD<1>	9 131
132 131 9	ENET_RXD_R<2>	I74	MAKE_BASE=TRUE	ENET_RXD<2>	9 131
132 131 9	ENET_RXD_R<3>	I75	MAKE_BASE=TRUE	ENET_RXD<3>	9 131
132 131 9	ENET_RXD_R<4>	I76	MAKE_BASE=TRUE	ENET_RXD<4>	9 131
132 131 9	ENET_RXD_R<5>	I77	MAKE_BASE=TRUE	ENET_RXD<5>	9 131
132 131 9	ENET_RXD_R<6>	I78	MAKE_BASE=TRUE	ENET_RXD<6>	9 131
132 131 9	ENET_RXD_R<7>	I79	MAKE_BASE=TRUE	ENET_RXD<7>	9 131
132 131	ENET_RX_DV_R	I80	MAKE_BASE=TRUE	ENET_RX_DV	131
132 131	ENET_RX_ER_R	I81	MAKE_BASE=TRUE	ENET_RX_ER	131
132 131	ENET_COL_R	I82	MAKE_BASE=TRUE	ENET_COL	131
132 131	ENET_CRS_R	I83	MAKE_BASE=TRUE	ENET_CRS	131

Preliminary

ENET SERIES TERM

SYNC_MASTER=FINO-HC SYNC_DATE=05/18/2005

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D	051-6790	08
SCALE NONE	SHT 130 OF 154	

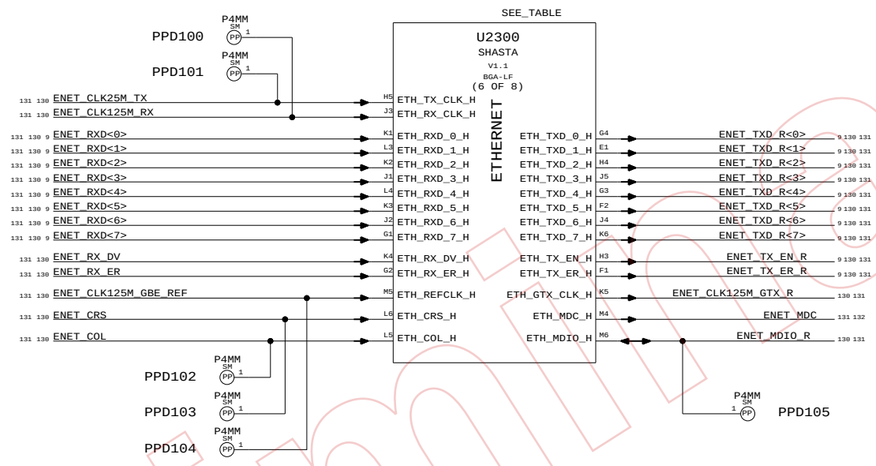
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
I47	0.38mm SPACING		ENET_CLK25M_TX	130 131
I46	0.38mm SPACING		ENET_CLK125M_RX	130 131
I48	0.38mm SPACING		ENET_CLK125M_GBE_REF	130 131
I22	0.38mm SPACING		ENET_CLK125M_GTX	130 132
I50	0.38mm SPACING		ENET_CLK125M_GTX_R	130 131
I51	ENET_FW_2X		ENET_RXD_R<7..0>	9 130 132
I52	ENET_FW_3X		ENET_RX_DV_R	130 132
I53	ENET_FW_3X		ENET_RX_ER_R	130 132
I54	ENET_FW_2X		ENET_RXD<7..0>	9 130 131
I55	ENET_FW_3X		ENET_RX_DV	130 131
I56	ENET_FW_3X		ENET_RX_ER	130 131
I58	ENET_FW_2X		ENET_TXD_R<7..0>	9 130 131
I57	ENET_FW_3X		ENET_TX_EN_R	9 130 131
I59	ENET_FW_3X		ENET_TX_ER_R	9 130 131
I60	ENET_FW_2X		ENET_TXD<7..0>	9 130 132
I61	ENET_FW_3X		ENET_TX_EN	9 130 132
I62	ENET_FW_3X		ENET_TX_ER	9 130 132
I63	ENET_FW_3X		ENET_CRS_R	130 132
I64	ENET_FW_3X		ENET_COL_R	130 132
I65	ENET_FW_3X		ENET_CRS	130 131
I66	ENET_FW_3X		ENET_COL	130 131
I68	ENET_FW_3X		ENET_MDC	131 132
I41	ENET_FW_3X		ENET_MDIO	130 131 132
I42	ENET_FW_3X		ENET_MDIO_R	130 131
I43	ENET_FW_3X		R8405_1	131
I45	ENET_FW_3X		R8405_2	131
I44	ENET_FW_3X		R8407_2	131

Page Notes

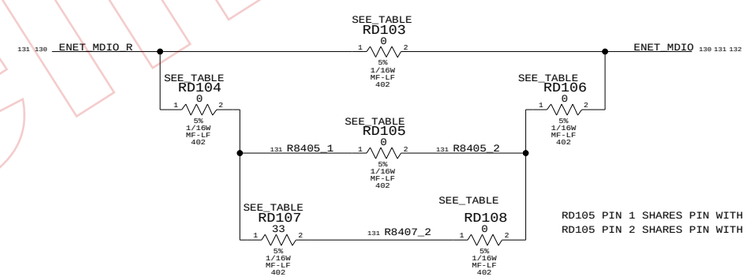
Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



RD103 PIN 1 SHARES PIN WITH RD104 PIN 1
RD103 PIN 2 SHARES PIN WITH RD106 PIN 2



RD105 PIN 1 SHARES PIN WITH RD107 PIN 1
RD105 PIN 2 SHARES PIN WITH RD108 PIN 2

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0-OHM,402,5%	RD103		ENET_MDIO_DELAY_0
116S0004	3	RES,0-OHM,402,5%	RD104,RD105,RD106		ENET_MDIO_DELAY_2NS
116S0004	3	RES,0-OHM,402,5%	RD104,RD108,RD106		ENET_MDIO_DELAY_4NS
116S0030	1	RES,33-OHM,402,5%	RD107		ENET_MDIO_DELAY_4NS

*

Shasta Ethernet

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 131 OF 154	

LAST_MODIFIED=Thu May 19 12:15:17 2005

DRAWING

TITLE=KILOWHRA

ABBREV=VDRAWING

Preliminary

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
	0.38mm SPACING		ENET_CLK125M_GBE_REF_R
	0.38mm SPACING		ENET_CLK125M_RX_R
	0.38mm SPACING		ENET_CLK25M_TX_R
	ENET	ENET_MDI0	ENET_MDI_P<0>
	ENET	ENET_MDI0	ENET_MDI_N<0>
	ENET	ENET_MDI1	ENET_MDI_P<1>
	ENET	ENET_MDI1	ENET_MDI_N<1>
	ENET	ENET_MDI2	ENET_MDI_P<2>
	ENET	ENET_MDI2	ENET_MDI_N<2>
	ENET	ENET_MDI3	ENET_MDI_P<3>
	ENET	ENET_MDI3	ENET_MDI_N<3>
	0.38mm SPACING		VESTA_CLK25M_XTALI
	0.38mm SPACING		VESTA_CLK25M_XTALO
	0.38mm SPACING		VESTA_CLK25M_XTALO_R

Page Notes

Power aliases required by this page:
- =PP3V3_ENET
- =PP2V5_ENETFW
- =PP1V2_ENETFW

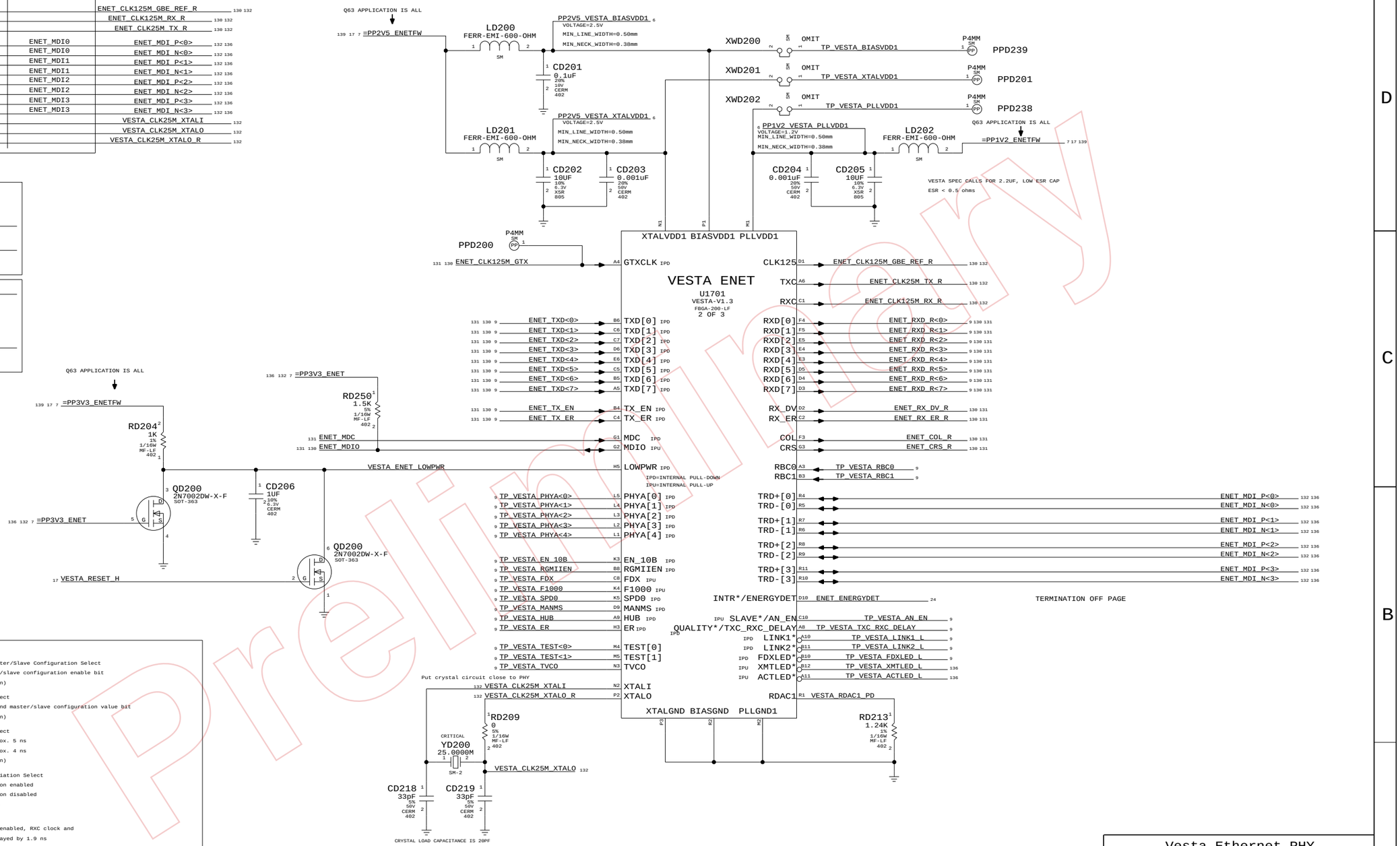
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: ENET

Line To Line: 0.38mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.13mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for ENET data pairs is 100 ohms.



Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

Preliminary

Vesta Ethernet PHY

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

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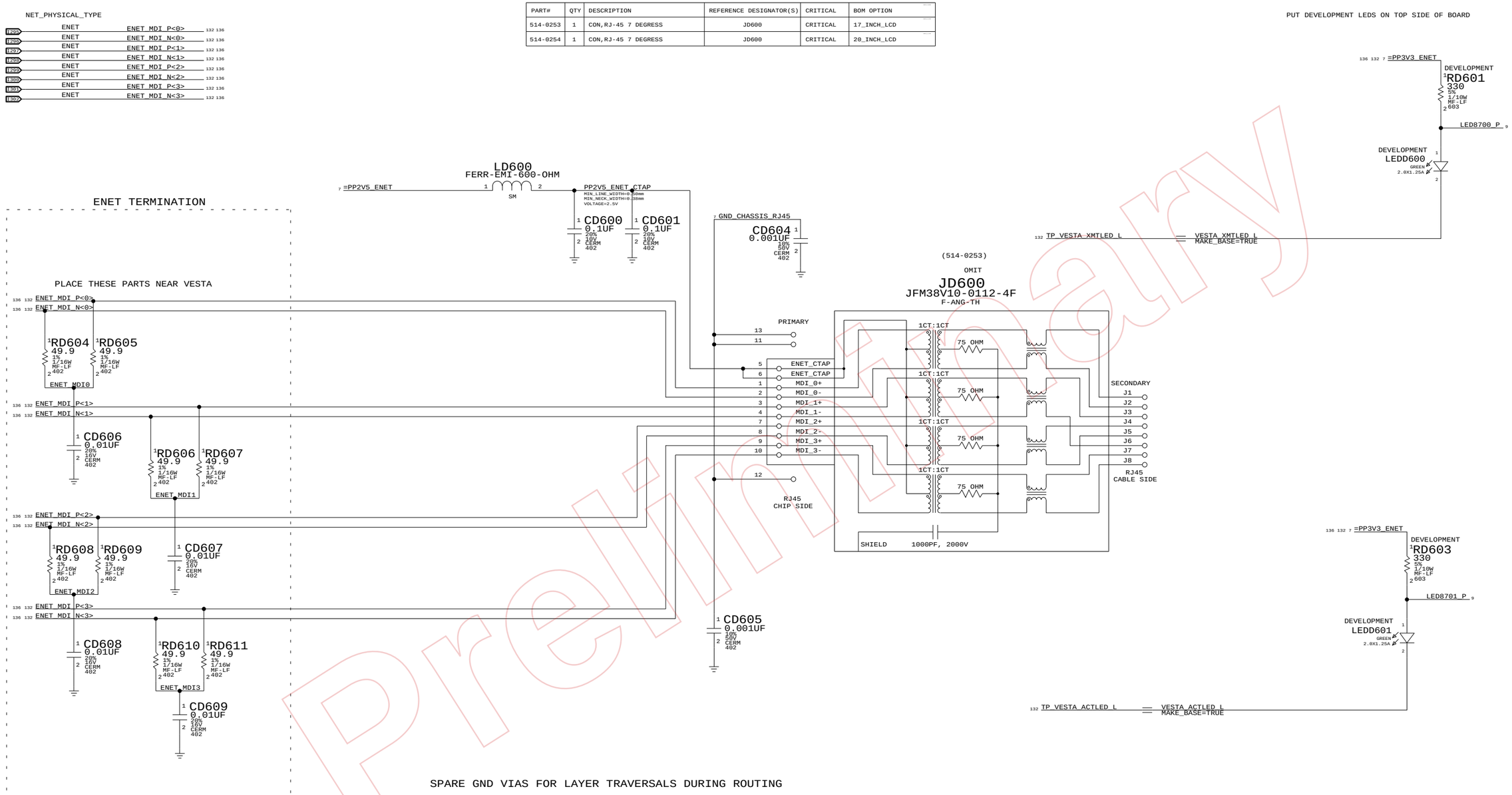
SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 132 OF 154	

LAST_MODIFIED=Thu May 19 14:08:40 2005

DRAWING

EXTRA CONSTRAINTS TO SUPPLEMENT THE THE MISSING NET PHYSICAL FROM EARLIER PAGE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0253	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0254	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD



Preliminary

ETHERNET CONNECTOR

SYNC_MASTER=FINO-HC SYNC_DATE=05/18/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 136 OF 154	

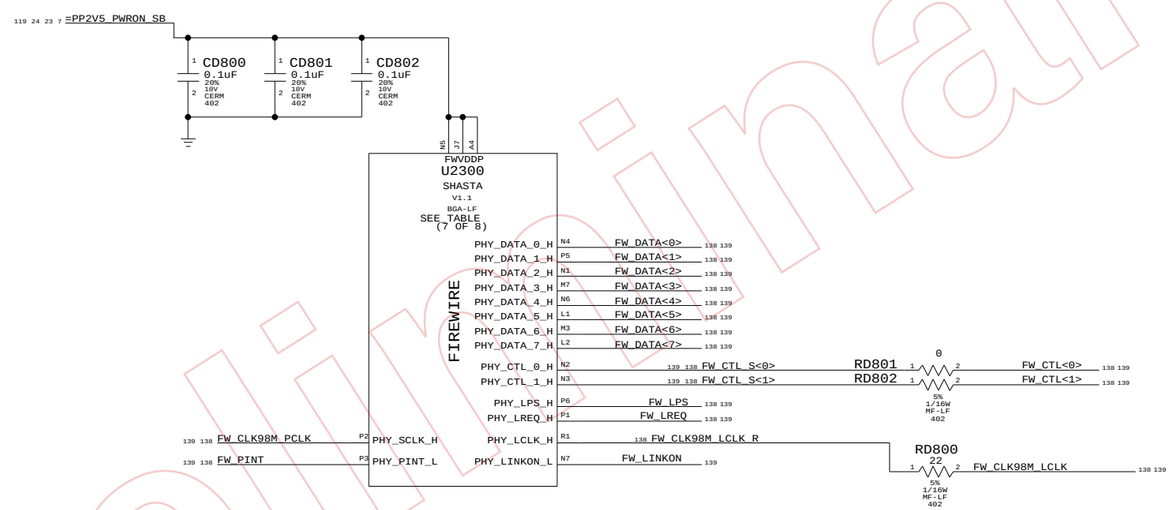
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
	ENET_FW_2X		FW_DATA<7..0>	138 139
	ENET_FW_3X		FW_CTL_S<1..0>	138 139
	ENET_FW_3X		FW_CTL<1..0>	138 139
	ENET_FW_2X		FW_DATA_R<7..0>	139
	ENET_FW_3X		FW_CTL_R<1..0>	139
	ENET_FW_3X		FW_LPS	138 139
	ENET_FW_3X		FW_LREQ	138 139
	ENET_FW_3X		FW_PINT	138 139
	0.38mm_SPACING		FW_CLK98M_LCLK	138 139
	0.38mm_SPACING		FW_CLK98M_PCLK	138 139
	0.38mm_SPACING		FW_CLK98M_LCLK_R	138

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Preliminary

Shasta FireWire

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE NONE SHT 138 OF 154

LAST_MODIFIED=Thu May 19 14:08:42 2005

DRAWING
TITLE=K11ANMAA
ABBREV=SHAACAG

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
(PROVIDED BY LINK PAGE)		0.38mm SPACING		FW_CLK98M_PCLK_R 139
	FW	FW	FW_TPA0	FW_TPA_P<0> 139 140
	FW	FW	FW_TPA0	FW_TPA_N<0> 139 140
	FW	FW	FW_TPB0	FW_TPB_P<0> 139 140
	FW	FW	FW_TPB0	FW_TPB_N<0> 139 140
	FW	FW	FW_TPA1	FW_TPA_P<1> 139 140
	FW	FW	FW_TPA1	FW_TPA_N<1> 139 140
	FW	FW	FW_TPB1	FW_TPB_P<1> 139 140
	FW	FW	FW_TPB1	FW_TPB_N<1> 139 140
ETHERNET SPACING TO ROUTE ON LAYER 8	FW	FW	FW_TPA2	FW_TPA_P<2> 139 140
	FW	FW	FW_TPA2	FW_TPA_N<2> 139 140
	FW	FW	FW_TPB2	FW_TPB_P<2> 139 140
	FW	FW	FW_TPB2	FW_TPB_N<2> 139 140
		0.38mm SPACING		VESTA_CLK24M_XTALI 139
		0.38mm SPACING		VESTA_CLK24M_XTALO 139
		0.38mm SPACING		VESTA_CLK24M_XTALO_R 139
	FW_CTL			FW_CTL_S<1..0> 138
	FW_CTL			FW_CTL<1..0> 138 139
	FW_CTL			FW_CTL_R<1..0> 138 139

Page Notes

Power aliases required by this page:
- =PPFW_PHY
- =PP3V3_FW
- =PP3V3_ENETFW
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta.
  See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta.
  See straps table for more information.

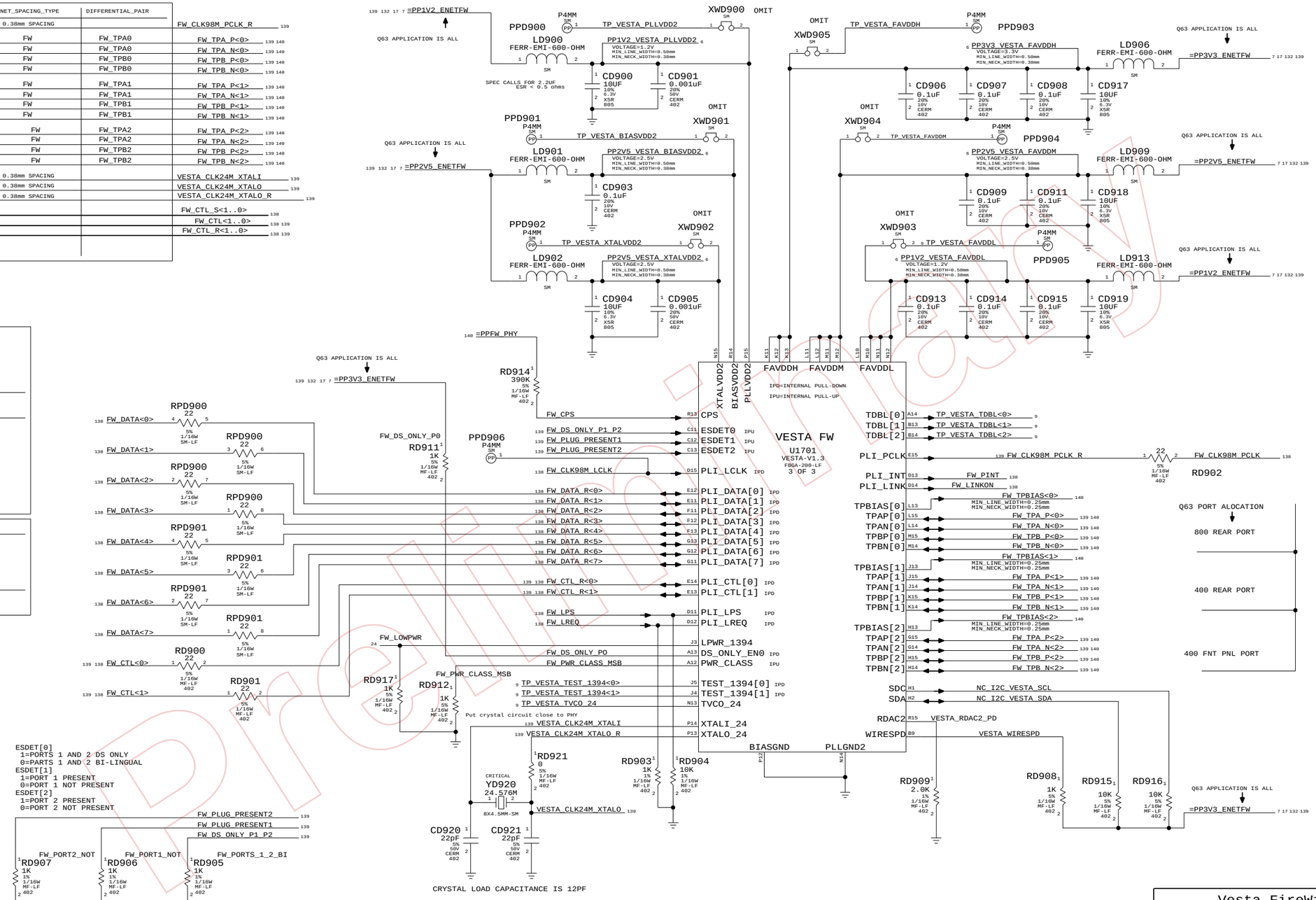
Net Spacing Type: FW

NOTE: Target differential impedance for FW data pairs is 110 ohms.

VESTA CONFIG STRAPS:

FW_PWR_CLASS_MSB - FIREWIRE POWER CLASS
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)

FW_DS_ONLY_P0 - PORT 0 DATA/STROBE
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)



Vesta FireWire PHY

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

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D	051-6790	08

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LAST_MODIFIED=Thu May 19 14:08:43 2005

DRAWING

NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
FW	FW	FW_TPA0_FL	FW_PORT0_TPA_P_FL	140
FW	FW	FW_TPA0_FL	FW_PORT0_TPA_N_FL	140
FW	FW	FW_TPB0_FL	FW_PORT0_TPB_P_FL	140
FW	FW	FW_TPB0_FL	FW_PORT0_TPB_N_FL	140
FW	FW	FW_TPA1_FL	FW_PORT1_TPA_P_FL	140
FW	FW	FW_TPA1_FL	FW_PORT1_TPA_N_FL	140
FW	FW	FW_TPB1_FL	FW_PORT1_TPB_P_FL	140
FW	FW	FW_TPB1_FL	FW_PORT1_TPB_N_FL	140

8 WATTS MAX
12 VOLTS

=PP12V_ALL_FW

RE056 1.3 20% 1W FF 2512
PP12V_FW MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM VOLTAGE=12V MAKE_BASE=TRUE

I443 =PPFW_PHY
TO FW CDS PIN (CABLE POWER DETECT)

DE000 MURS320XKG SMC
FW_VP_R MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM MAKE_BASE=TRUE VOLTAGE=24V

CE009 0.1UF 10% 50V X7R 603-1

CRITICAL
RE002 1.3 20% 1W FF 2512

FW_VP MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM VOLTAGE=24V

FW_VP MAX IS 24V

FE002 0.75AMP-13.2V MINISMD

DESIGNED WITH INTENTION TO RESIZE FUSE LIMITS EQUAL FW SPEC 1.5A LIMIT

PPFW_PORT0_VP MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=24V

FE000 1.5AMP-33V SM
PPFW_PORT1_VP MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=24V

POSSIBLE CURRENT SHARING SCENARIO
KCL = CABLE POWER + SYSTEM POWER = > 1.5 AMPS

"Snapback" & "Late VG" Protection

PP3V3_FW_ESD

DPE010 BAV99DW-X-F SOT-363
CE010 0.001UF 10% 50V CERM 402
CE011 0.001UF 10% 50V CERM 402
GND_CHASSIS_FIREWIRE

LE010 FERR-160-OHM 1206-LF

PORT 0
1394A
OMIT

FLE010 120-OHM 2012 SYM_VER-1
FLE011 120-OHM 2012 SYM_VER-1

FW_PORT0_TPA_P
FW_PORT0_TPA_N
FW_PORT0_TPB_P
FW_PORT0_TPB_N

JE000 UF01613-M33-4F F-ST-TH
TPO (TPA+)
TPO# (TPA-)
TPI (TPB+)
TPI# (TPB-)
VP
VGND

PPFW_PORT0_VP_FL VOLTAGE=24V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm

DPE011 BAV99DW-X-F SOT-363
CE012 0.001UF 10% 50V CERM 402
CE013 0.001UF 10% 50V CERM 402

FW_VP MAX IS 24V
CE015 0.1UF 10% 50V X7R 603-1
CE016 0.01UF 20% 16V CERM 402

514-0251 20_INCH_VERSION SHOWN

GND_CHASSIS_FIREWIRE

Termination

Place close to FireWire PHY

FW_TPBIAS<1> VOLTAGE=1.86V
FW_TPBIAS<0> VOLTAGE=1.86V

CE050 1uF 10% 6.3V CERM 402
CE060 1uF 10% 6.3V CERM 402

RE050 56.2 1% 1/16W MF-LF 402
RE051 56.2 1% 1/16W MF-LF 402
RE060 56.2 1% 1/16W MF-LF 402
RE061 56.2 1% 1/16W MF-LF 402

FW_TPA_P<0> — FW_PORT0_TPA_P
FW_TPA_N<0> — FW_PORT0_TPA_N
FW_TPB_P<0> — FW_PORT0_TPB_P
FW_TPB_N<0> — FW_PORT0_TPB_N
FW_TPA_P<1> — FW_PORT1_TPA_P
FW_TPA_N<1> — FW_PORT1_TPA_N
FW_TPB_P<1> — FW_PORT1_TPB_P
FW_TPB_N<1> — FW_PORT1_TPB_N
MAKE_BASE=TRUE

RE052 56.2 1% 1/16W MF-LF 402
RE053 56.2 1% 1/16W MF-LF 402
RE062 56.2 1% 1/16W MF-LF 402
RE063 56.2 1% 1/16W MF-LF 402

FW_TPA_C<0> VOLTAGE=0V
FW_TPA_C<1> VOLTAGE=0V

CE054 270pF 5% 25V CERM 402
CE064 270pF 5% 25V CERM 402

RE054 4.99K 1% 1/16W MF-LF 402
RE064 4.99K 1% 1/16W MF-LF 402

3rd TPA/TPB pair unused

FW_TPBIAS<2> — NC_FW_TPBIAS2
FW_TPA_P<2> — NC_FW_TPA_P2
FW_TPA_N<2> — NC_FW_TPA_N2
FW_TPB_P<2> — FW_TPB2_PD
FW_TPB_N<2>
MAKE_BASE=TRUE NO_TEST=YES

RE070 1K 5% 1/16W MF-LF 402

"Snapback" & "Late VG" Protection

PP3V3_FW_ESD

DPE020 BAV99DW-X-F SOT-363
CE020 0.001UF 10% 50V CERM 402
CE021 0.001UF 10% 50V CERM 402
GND_CHASSIS_FIREWIRE

FLE020 120-OHM 2012 SYM_VER-1
FLE021 120-OHM 2012 SYM_VER-1

FW_PORT1_TPA_P
FW_PORT1_TPA_N
FW_PORT1_TPB_P
FW_PORT1_TPB_N

PPFW_PORT1_VP

LE020 FERR-160-OHM 1206-LF

PORT 1
1394A
OMIT

JE001 UF01613-M33-4F F-ST-TH
TPO (TPA+)
TPO# (TPA-)
TPI (TPB+)
TPI# (TPB-)
VP
VGND

PPFW_PORT1_VP_FL MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=24V

DPE021 BAV99DW-X-F SOT-363
CE022 0.001UF 10% 50V CERM 402
CE023 0.001UF 10% 50V CERM 402

CE025 0.1UF 10% 50V X7R 603-1
CE026 0.01UF 20% 16V CERM 402

514-0251 20_INCH_VERSION SHOWN

GND_CHASSIS_FIREWIRE

ESD Rail

CALCULATION = 220 OHMS, THERE'S ALREADY A 215 IN THE DESIGN, SO I'M USING 215 INSTEAD

=PP3V3_FW — RE090 215 1% 1/16W MF-LF 402 — PP3V3_FW_ESD_F VOLTAGE=3.3V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm

LE090 400-OHM-EMI SM-1

PP3V3_FW_ESD VOLTAGE=3.3V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm

DE090 SOT23 BZX84C2V7-X-F

[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

ZHE090 HOLE-VIA
ZHE091 HOLE-VIA
ZHE092 HOLE-VIA
ZHE093 HOLE-VIA

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0248	1	CON,1394A 7 DEGREES	JE000	CRITICAL	17_INCH_LCD
514-0248	1	CON,1394A 7 DEGREES	JE001	CRITICAL	17_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE000	CRITICAL	20_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE001	CRITICAL	20_INCH_LCD

FIREWIRE CONNECTORS

SYNC_MASTER=FINO-HC SYNC_DATE=05/18/2005

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	USB2	USB2_S	USB2_0	USB2_P<0>
	USB2	USB2_S	USB2_0	USB2_N<0>
	USB2	USB2_S	USB2_1	USB2_P<1>
	USB2	USB2_S	USB2_1	USB2_N<1>
	USB2	USB2_S	USB2_2	USB2_P<2>
	USB2	USB2_S	USB2_2	USB2_N<2>
	USB2	USB2	USB2_3	USB2_P<3>
	USB2	USB2	USB2_3	USB2_N<3>
	USB2	USB2	USB2_4	USB2_P<4>
	USB2	USB2	USB2_4	USB2_N<4>
	0.38mm SPACING			NEC_CLK30M_XT1
	0.38mm SPACING			NEC_CLK30M_XT2
	0.38mm SPACING			NEC_CLK30M_XT2_R

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_USB

Signal aliases required by this page:
(NONE)

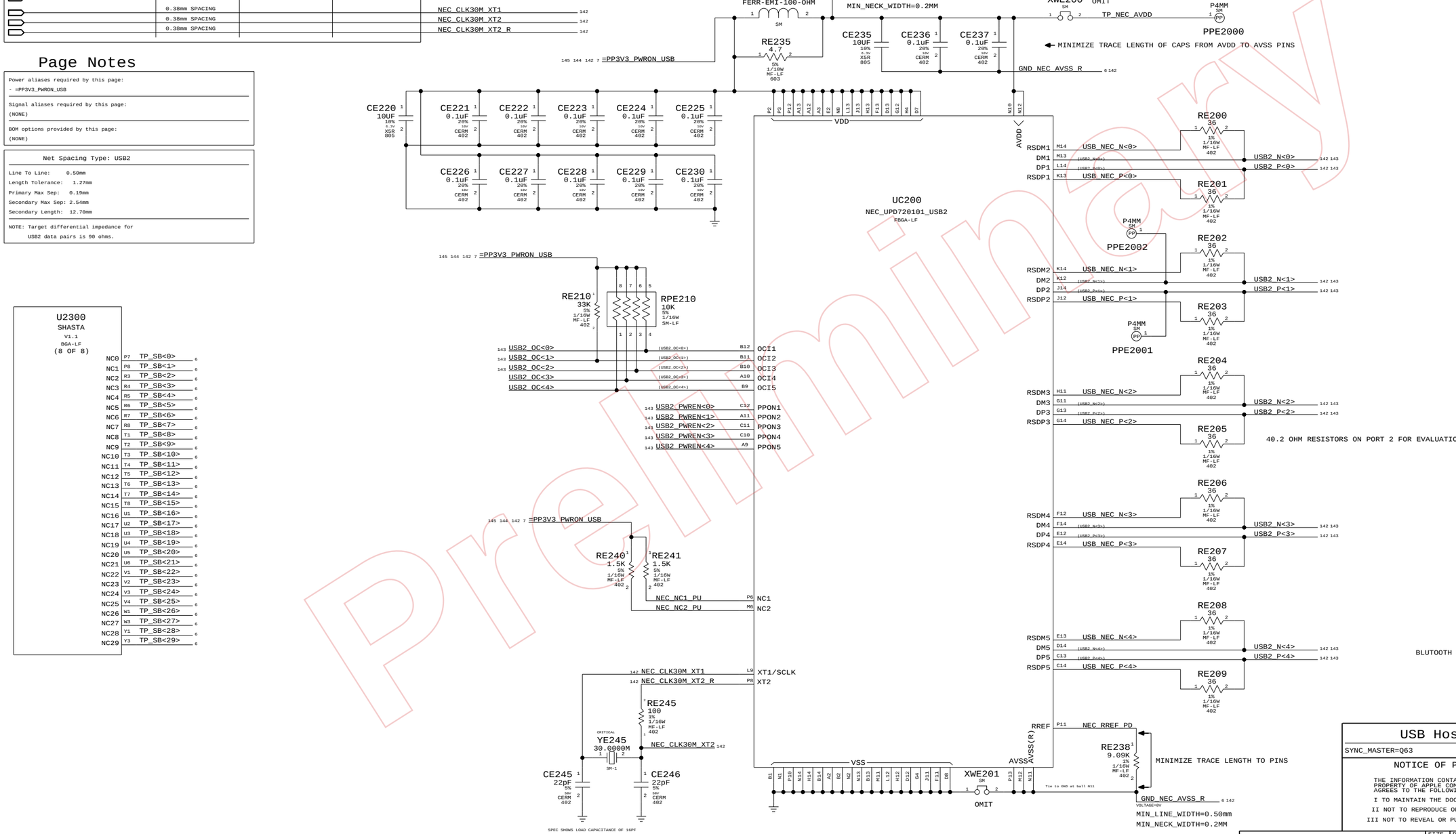
BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 0.50mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.19mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

Q63 USB PORT ALLOCATION
REAR USB (PORT #0)
FRONT PANEL USB (PORT #1)
REAR USB (PORT #2)
REAR USB (PORT #3)



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USB Host Interfaces

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

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LAST_MODIFIED=Thu May 19 14:08:45 2005
DRAWING
TITLE=KILOWHRA
ABBREV=DRAWING

Page Notes

Power aliases required by this page:
- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

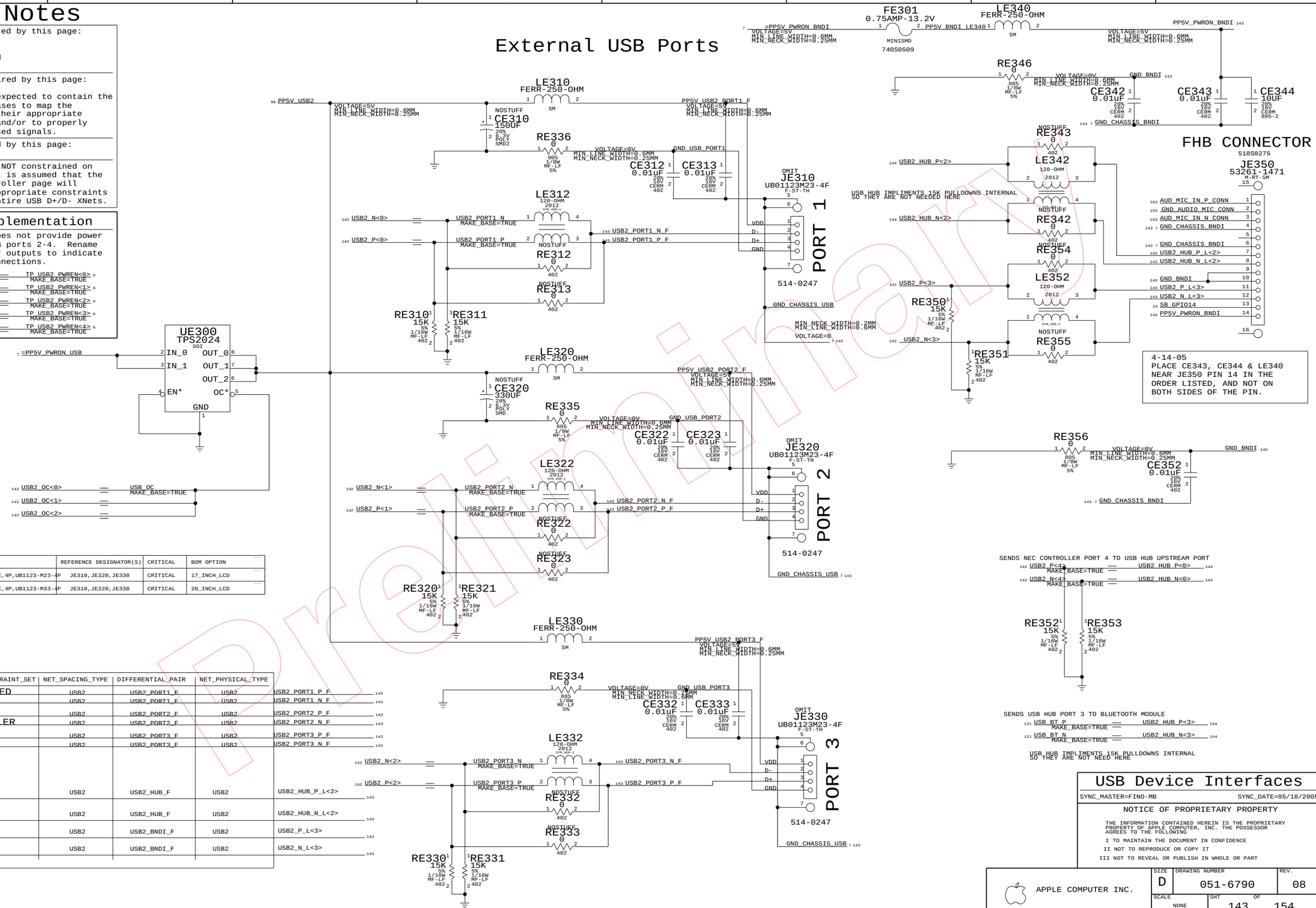
NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

142 USB2_PWREN<0> — TP_USB2_PWREN<0> 6 (MAKE_BASE=TRUE)
142 USB2_PWREN<1> — TP_USB2_PWREN<1> 6 (MAKE_BASE=TRUE)
142 USB2_PWREN<2> — TP_USB2_PWREN<2> 6 (MAKE_BASE=TRUE)
142 USB2_PWREN<3> — TP_USB2_PWREN<3> 6 (MAKE_BASE=TRUE)
142 USB2_PWREN<4> — TP_USB2_PWREN<4> 6 (MAKE_BASE=TRUE)

External USB Ports



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0247	3	USB RECEPTACLE,4P,UB1123-M23-4F	JE310,JE320,JE330	CRITICAL	17_INCH_LCD
514-0250	3	USB RECEPTACLE,4P,UB1123-M33-4F	JE310,JE320,JE330	CRITICAL	20_INCH_LCD

	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	
I602	PROVIDED BY USB CONTROLLER	USB2	USB2_PORT1_F	USB2	USB2_PORT1_P_F 143
I603		USB2	USB2_PORT1_F	USB2	USB2_PORT1_N_F 143
I604		USB2	USB2_PORT2_F	USB2	USB2_PORT2_P_F 143
I605		USB2	USB2_PORT2_F	USB2	USB2_PORT2_N_F 143
I606		USB2	USB2_PORT3_F	USB2	USB2_PORT3_P_F 143
I607		USB2	USB2_PORT3_F	USB2	USB2_PORT3_N_F 143
I608		USB2	USB2_HUB_F	USB2	USB2_HUB_P_L<2> 143
I609		USB2	USB2_HUB_F	USB2	USB2_HUB_N_L<2> 143
I610		USB2	USB2_BNDI_F	USB2	USB2_P_L<3> 143
I611		USB2	USB2_BNDI_F	USB2	USB2_N_L<3> 143

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USB Device Interfaces

SYNC_MASTER=FINO-MB SYNC_DATE=05/18/2005

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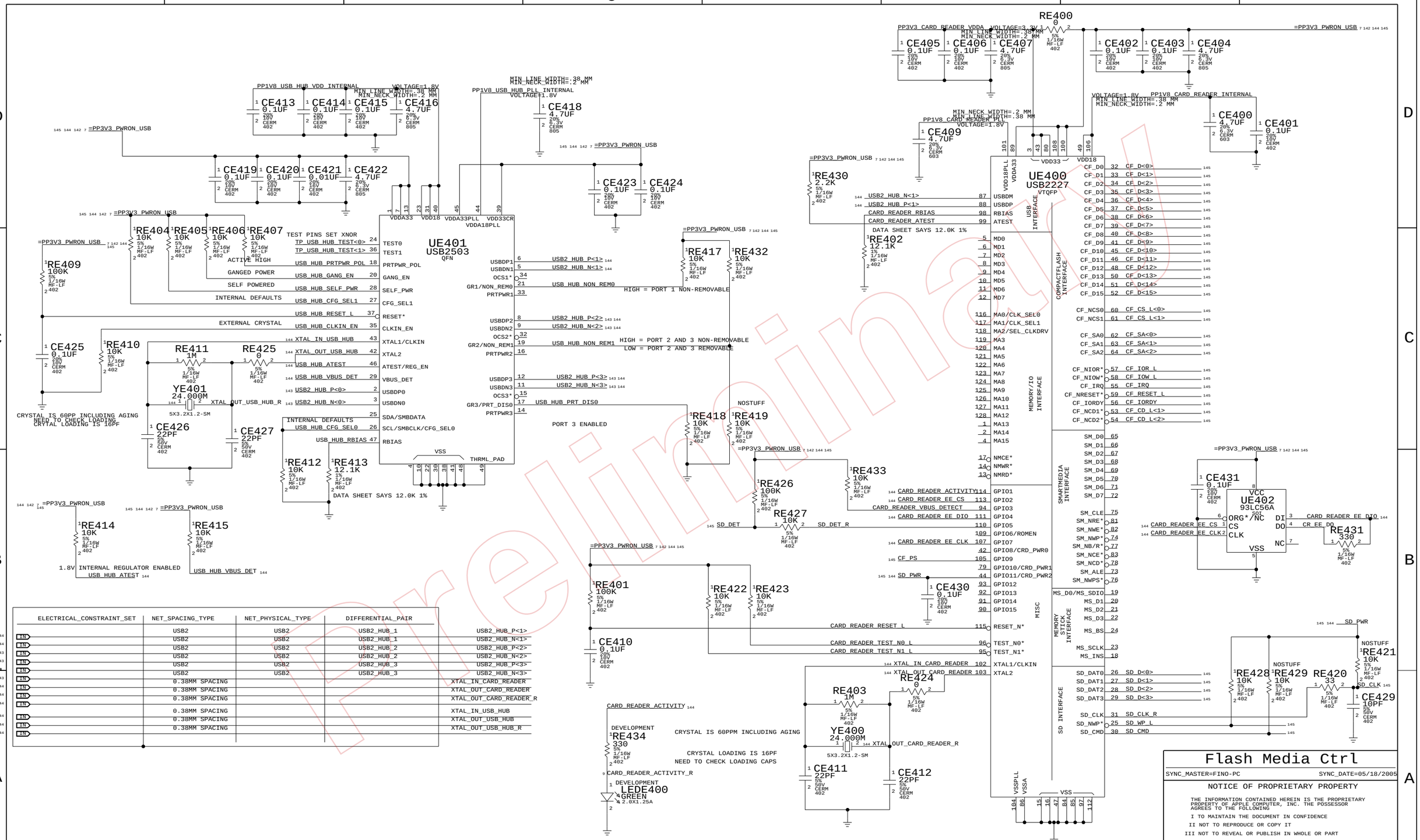

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	USB2	USB2	USB2_HUB_1	USB2_HUB_P<1>
	USB2	USB2	USB2_HUB_1	USB2_HUB_N<1>
	USB2	USB2	USB2_HUB_2	USB2_HUB_P<2>
	USB2	USB2	USB2_HUB_2	USB2_HUB_N<2>
	USB2	USB2	USB2_HUB_3	USB2_HUB_P<3>
	USB2	USB2	USB2_HUB_3	USB2_HUB_N<3>
	0.38MM SPACING			XTAL_IN_CARD_READER
	0.38MM SPACING			XTAL_OUT_CARD_READER
	0.38MM SPACING			XTAL_OUT_CARD_READER_R
	0.38MM SPACING			XTAL_IN_USB_HUB
	0.38MM SPACING			XTAL_OUT_USB_HUB
	0.38MM SPACING			XTAL_OUT_USB_HUB_R

Flash Media Ctrl

SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

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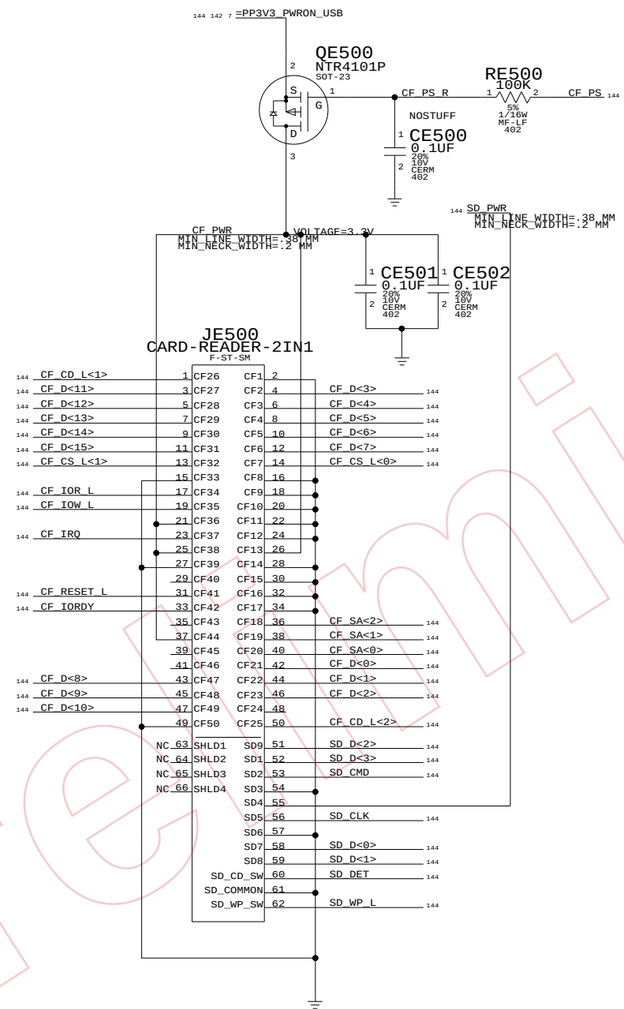

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Flash Connector

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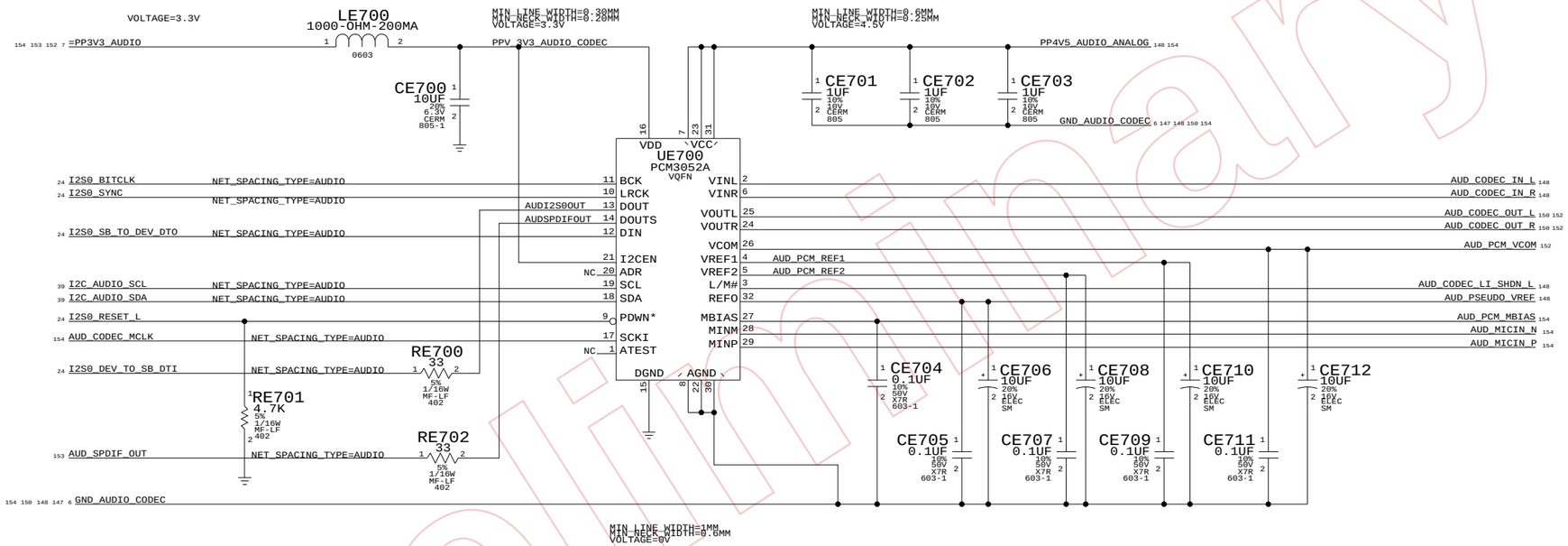
AUDIO CODEC
APPLE P/N 353S0933



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AUDIO: CODEC

SYNC_MASTER=FINO-SO SYNC_DATE=05/18/2005

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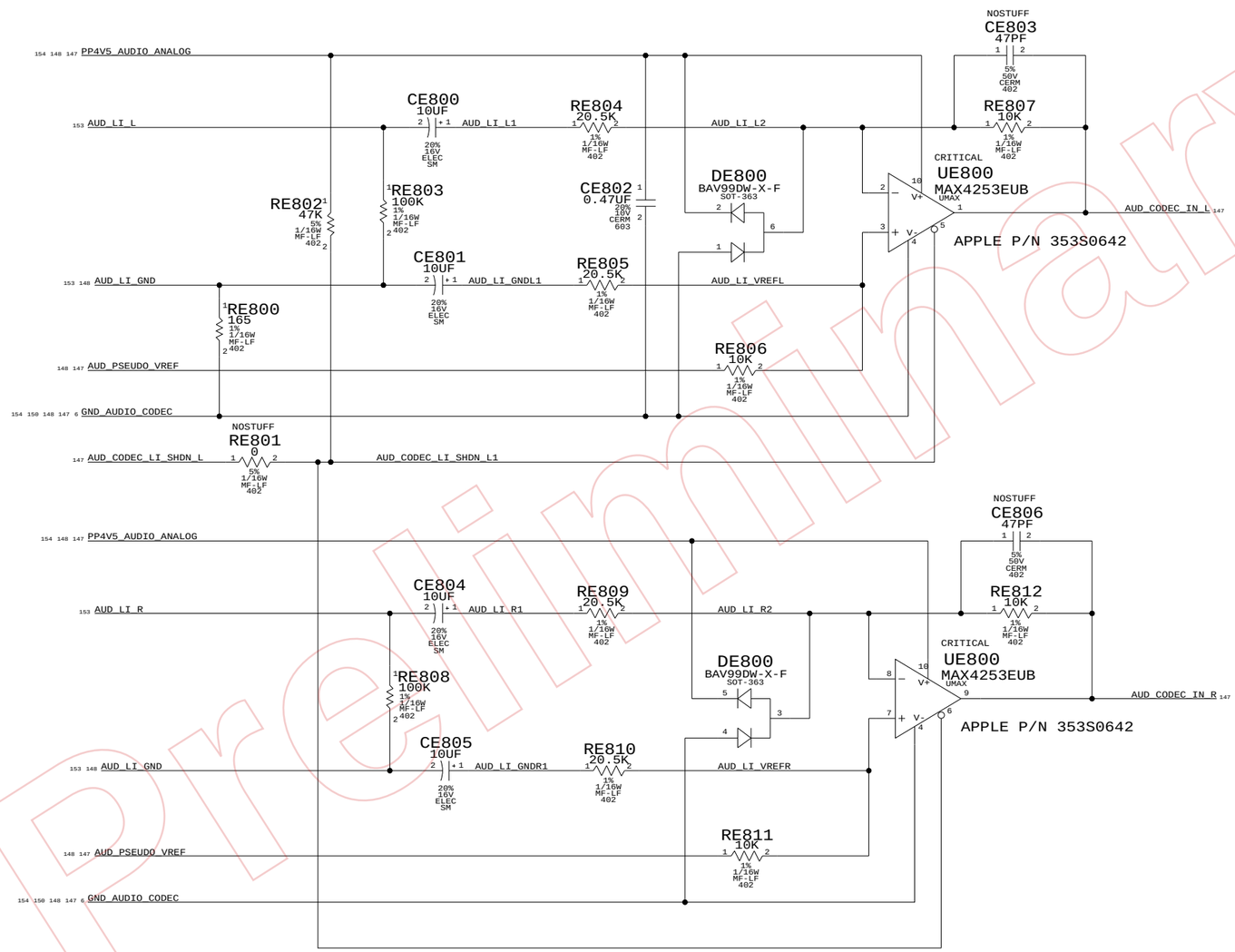
LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49



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AUDIO: LINE INPUT AMP

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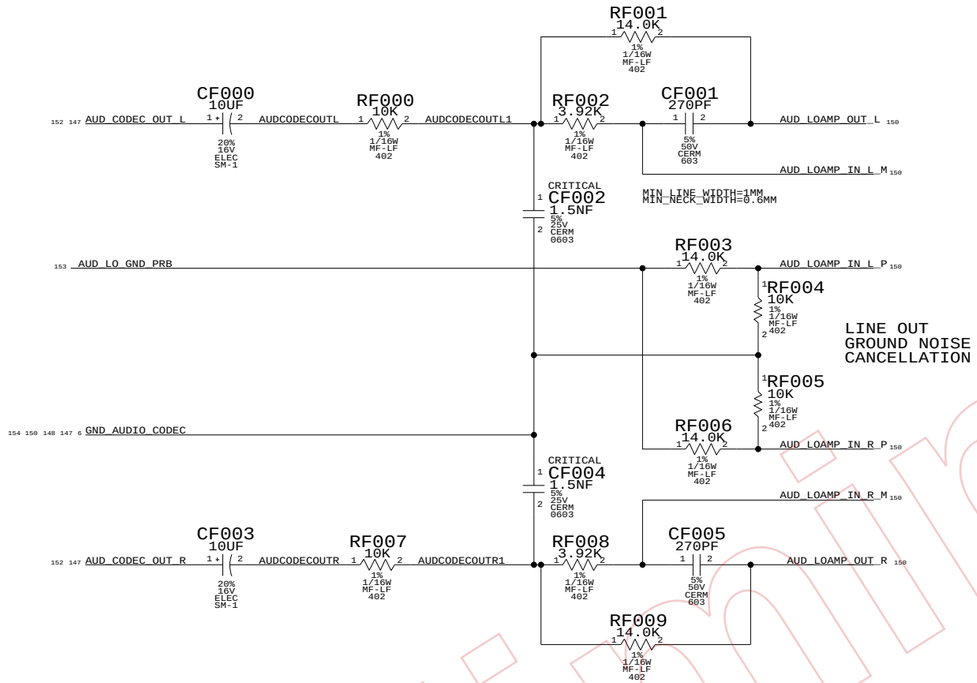
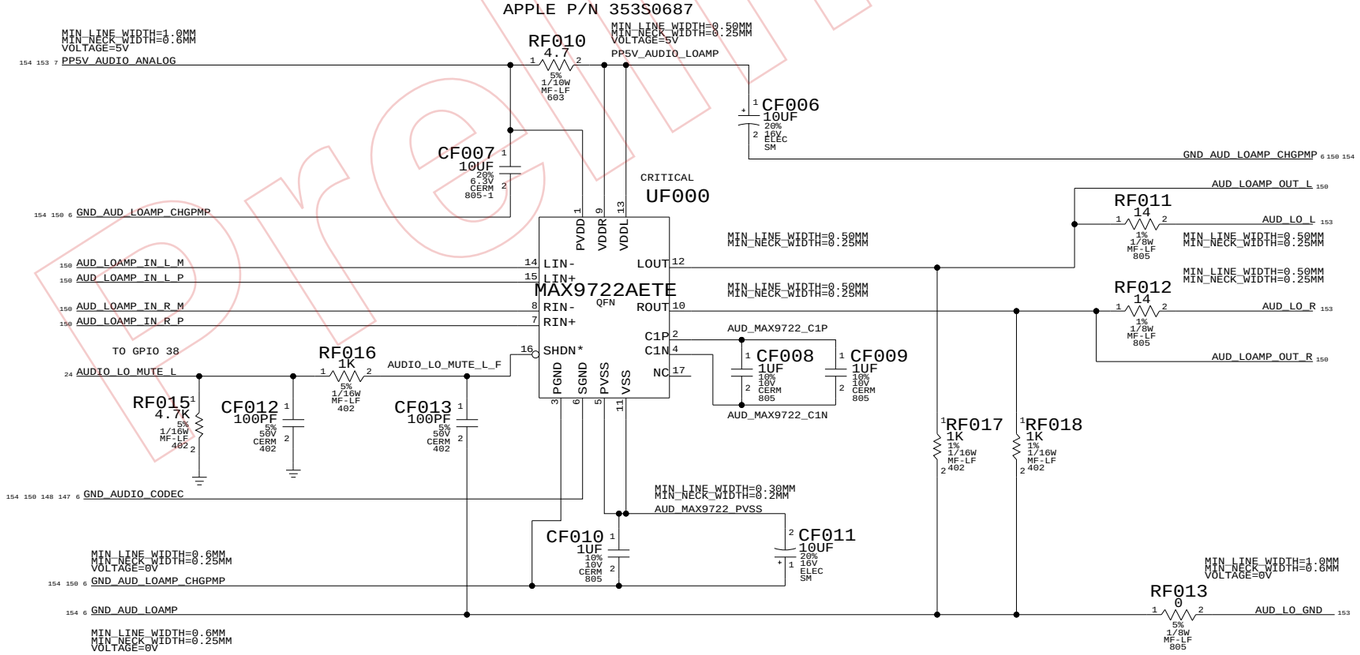
LINE OUT LOW-PASS FILTER

FC = 37 KHZ, HO = -1.4



LINE OUT AMP

APPLE P/N 353S0687



AUDIO: LINE OUT AMP

SYNC_MASTER=FINO-SO SYNC_DATE=05/18/2005

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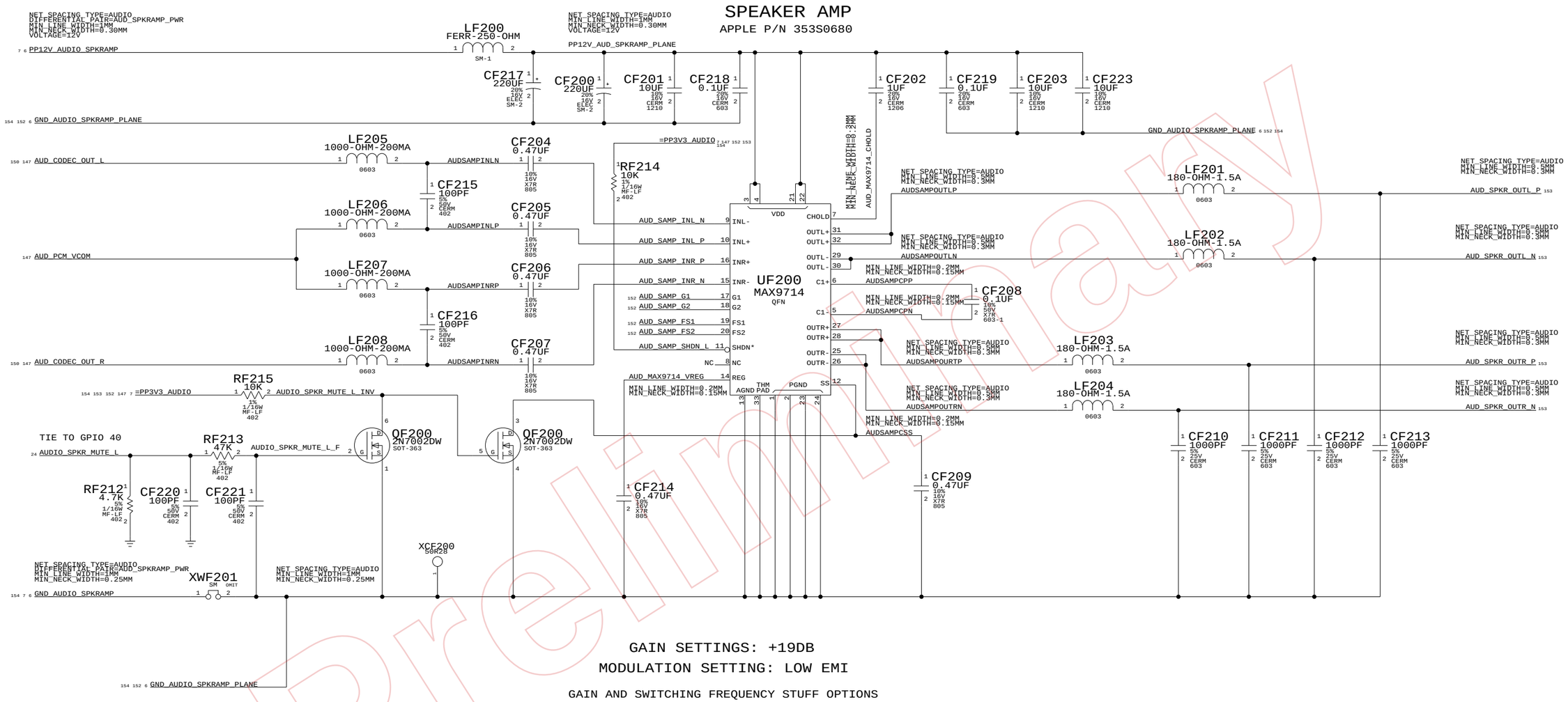

AUDIO: SPEAKER AMP

SYNC_MASTER=FINO-SO SYNC_DATE=05/18/2005

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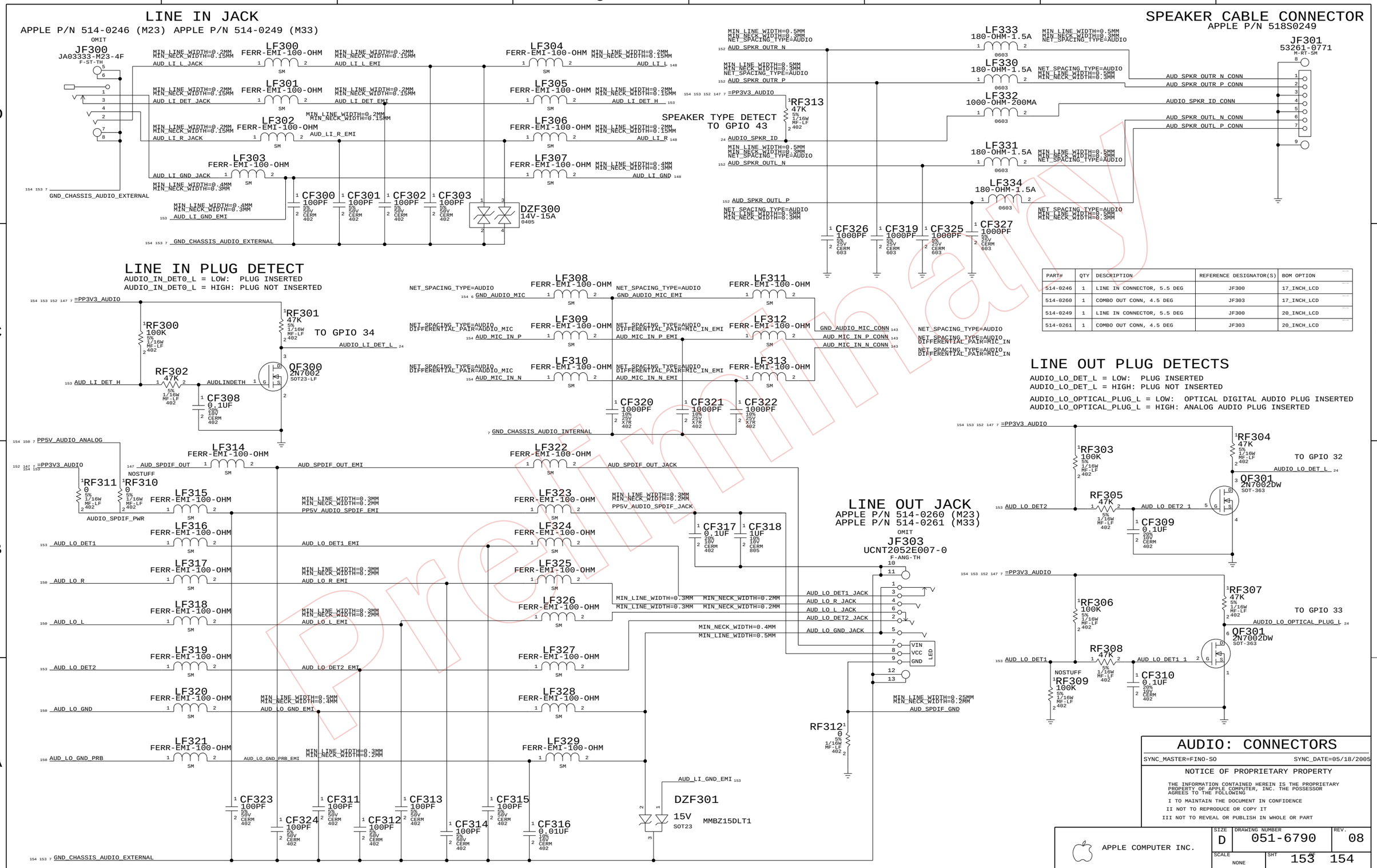

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
514-0246	1	LINE IN CONNECTOR, 5.5 DEG	JF300	17_INCH_LCD
514-0260	1	COMBO OUT CONN, 4.5 DEG	JF303	17_INCH_LCD
514-0249	1	LINE IN CONNECTOR, 5.5 DEG	JF300	20_INCH_LCD
514-0261	1	COMBO OUT CONN, 4.5 DEG	JF303	20_INCH_LCD

AUDIO: CONNECTORS

SYNC_MASTER=FINO-SO SYNC_DATE=05/18/2005

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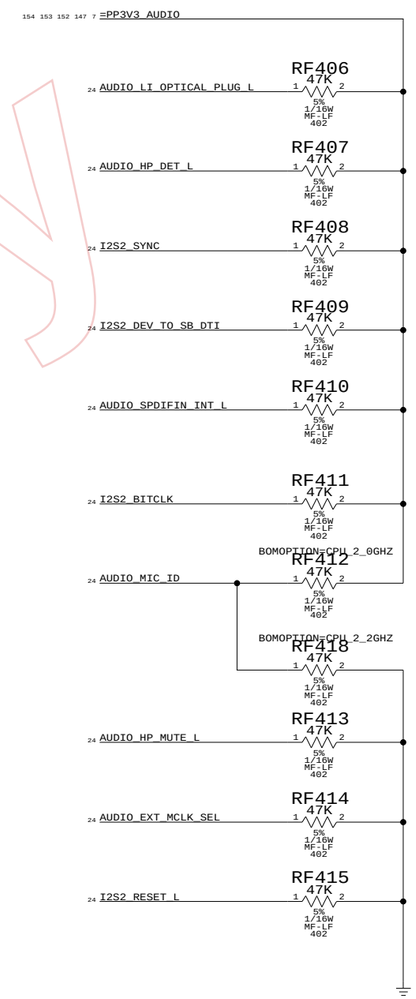
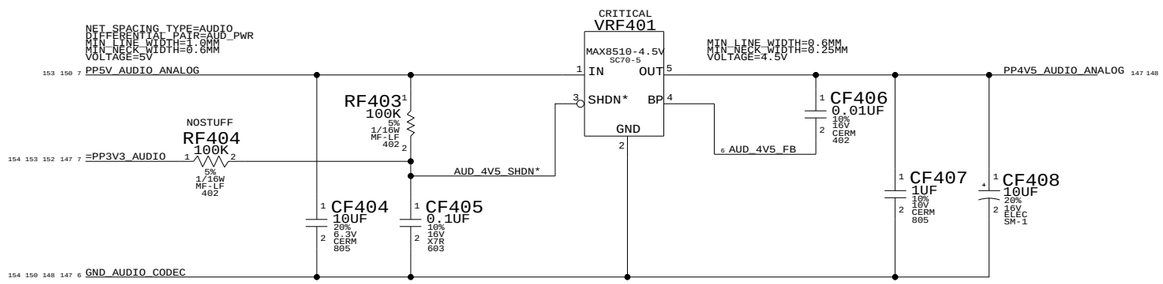
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0655	353S0933		U9500	PCM3052

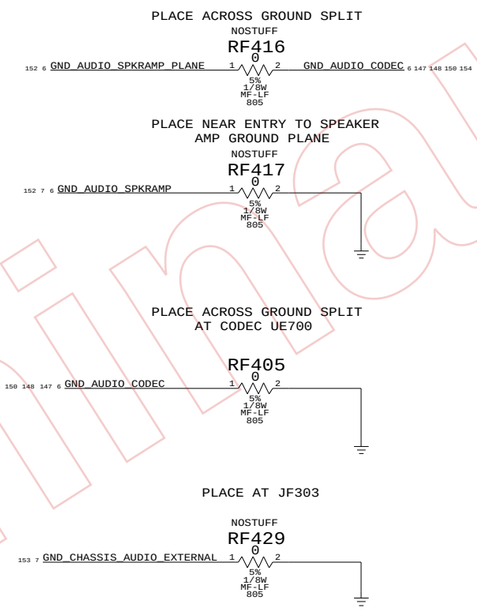
UNUSED GPIO TERMINATIONS



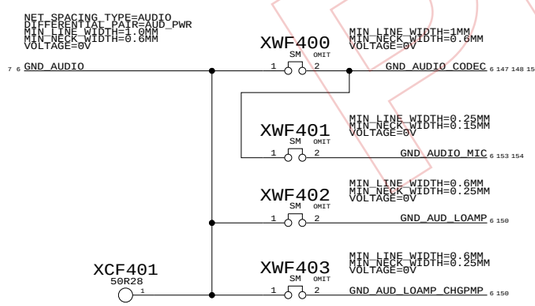
4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

APPLE P/N 353S0733

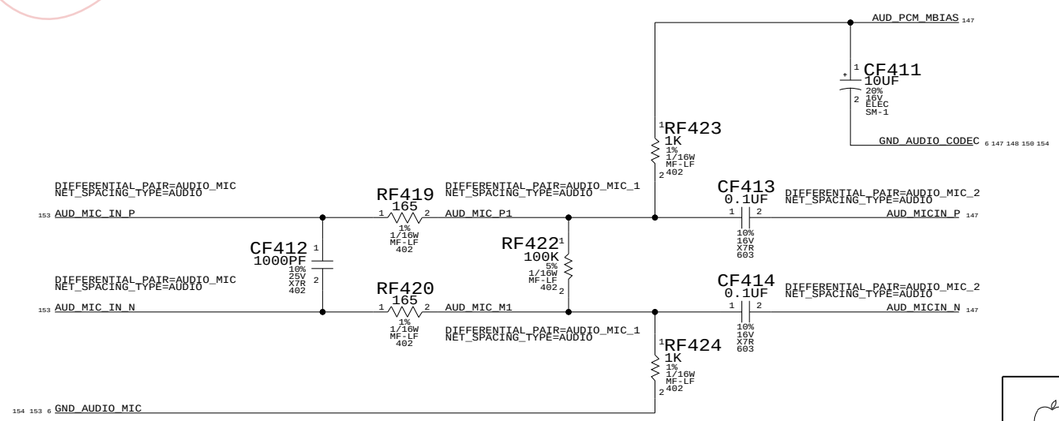




AUDIO GROUND RETURNS



MICROPHONE IMPEDANCE MATCHING CIRCUIT



MAKE_BASE=TRUE I88
9 TP_I2S2_SB_TO_DEV_DTO — I2S2_SB_TO_DEV_DTO 24

MAKE_BASE=TRUE I89
6 NC_I2S2_MCLK — I2S2_MCLK 24

MAKE_BASE=TRUE I116
24 I2S0_MCLK — AUD_CODEC_MCLK 147

AUDIO: POWER SUPPLIES

SYNC_MASTER=FINO-SO SYNC_DATE=05/18/2005

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