

V03A DIS/UMA BLOCK DIAGRAM

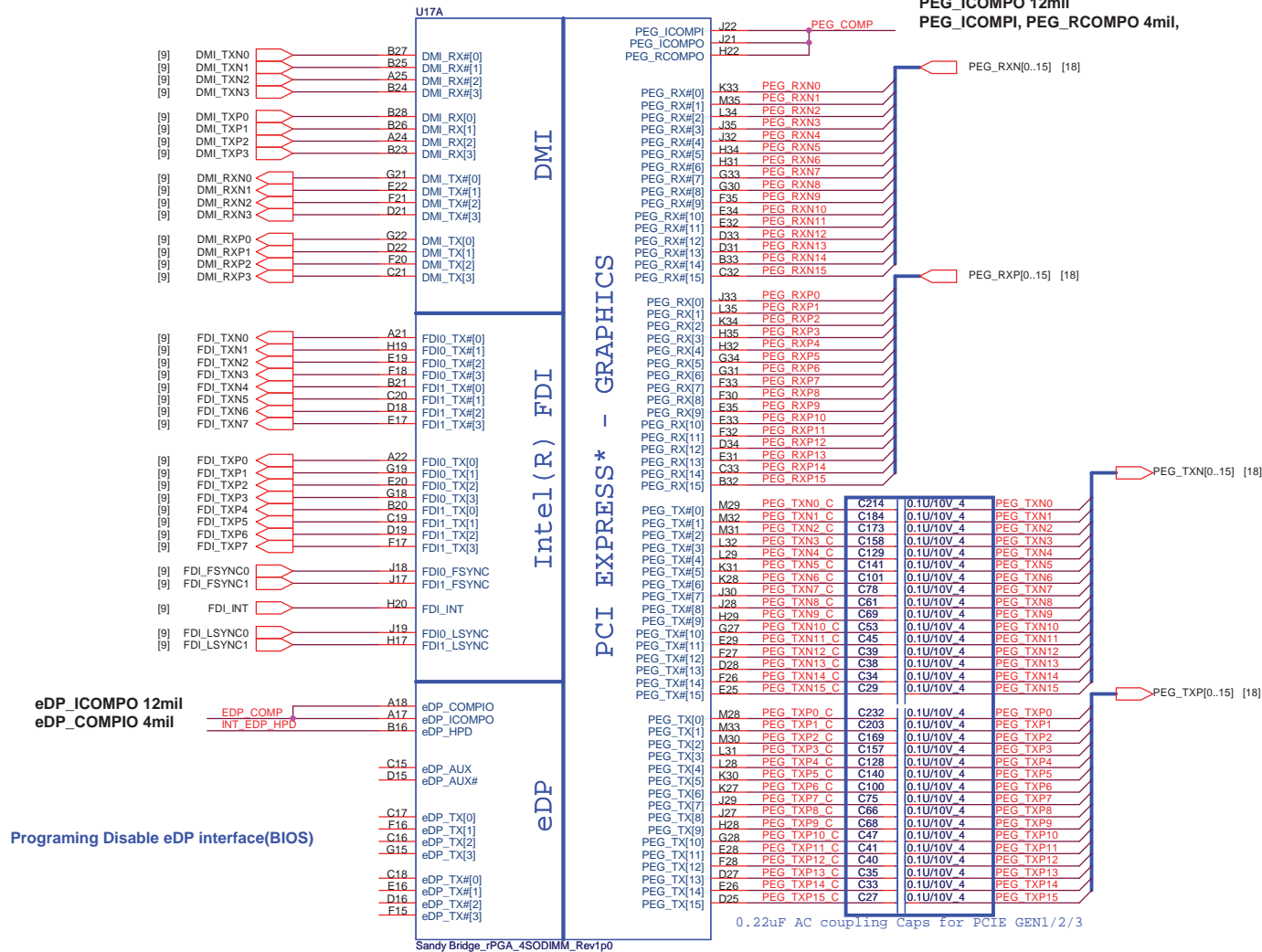
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power State	+RTC_CELL	+DC_IN +DC_IN_SS +PWR_SRC +5V_ALW_2 +3.3V_ALW +5V_ALW +15V_ALW +3.3V_LAN (for V03)	+VCHGR +PWR_SRC +5V_ALW_2 +3.3V_ALW +5V_ALW +15V_ALW +3.3V_LAN (for V03)	+5V_SUS +3.3V_SUS +1.5V_SUS +1.5V_CPU +DDR_VTTREF +3.3V_LAN (for R03)	+VCC_CORE +VCC_GFX_CORE +1.05V_PCH +5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +VCCSA +0.75V_DDR_VTT +LCDVCC +VCC_DGFX_CORE	
S0	ON	ON	ON	ON	ON	
S1						
S3	ON	ON	ON	ON	OFF	
S4/S5 AC	ON	ON				
S4/S5 DC Only	ON		ON	OFF	OFF	
AC/DC No Exist	ON	OFF	OFF	OFF	OFF	

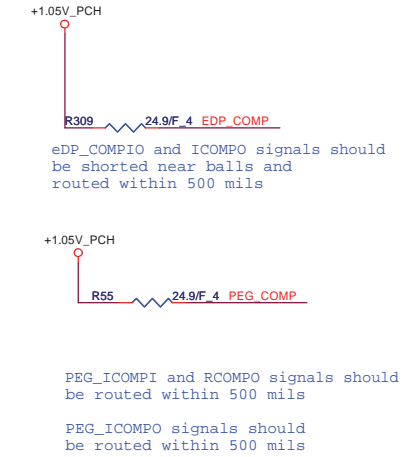
SMBCLK SMBDATA								
SMB_CLK_ME1 SMB_DAT_ME1								
AB1A_CLK AB1A_DATA								



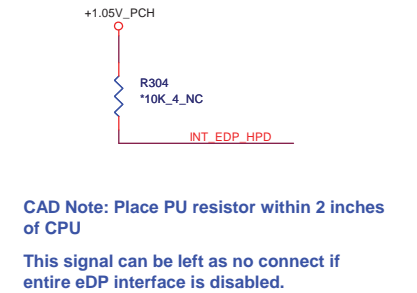
Sandy Bridge Processor (DMI, PEG, FDI)



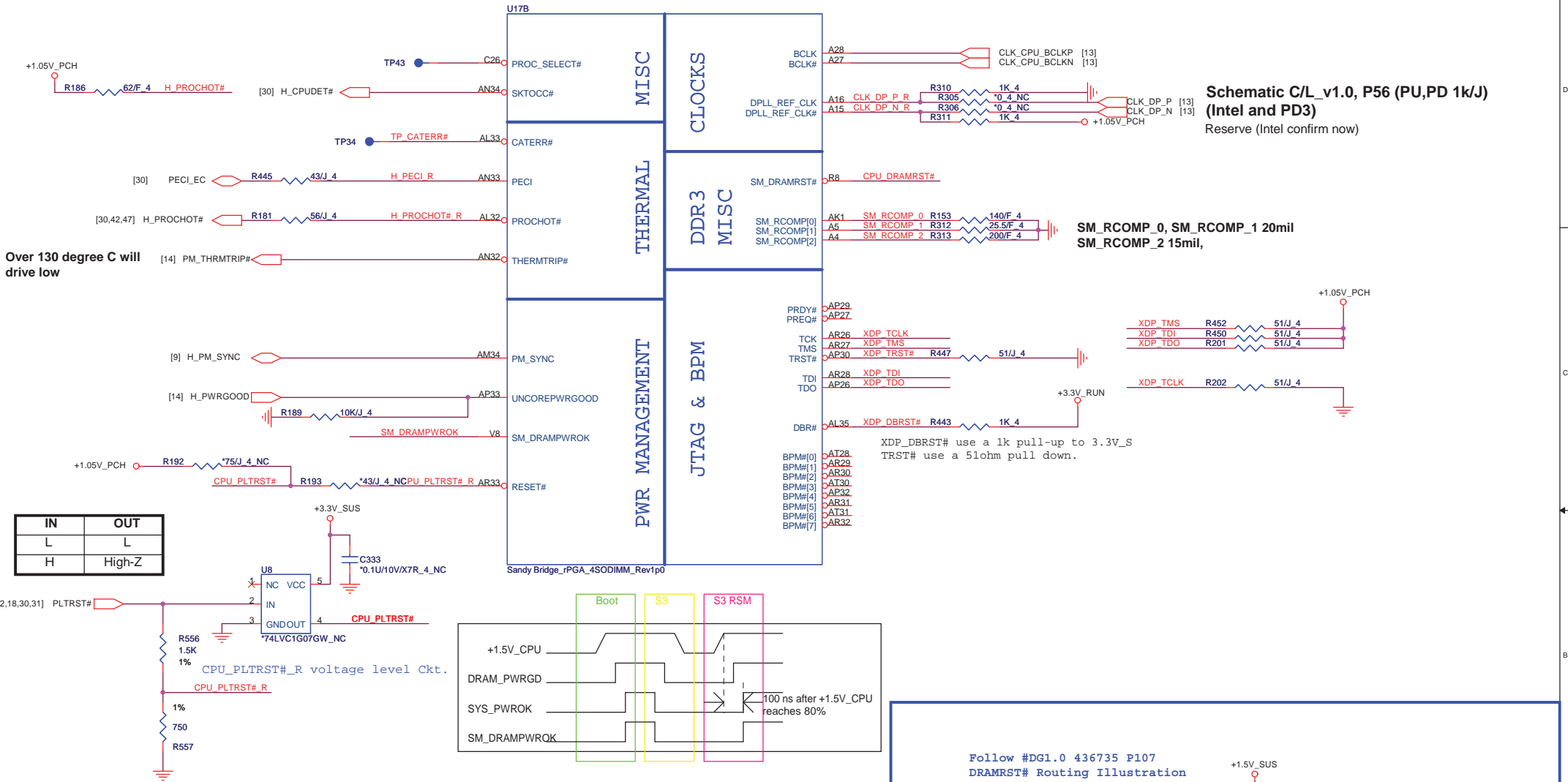
DP & PEG Compensation



eDP Hot-plug (Disable)

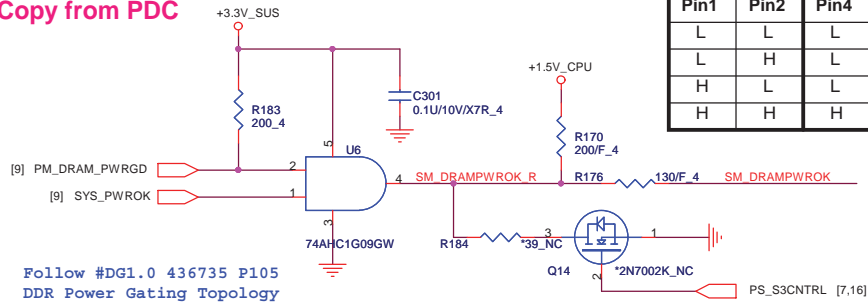


Sandy Bridge Processor (CLK,MISC,JTAG)



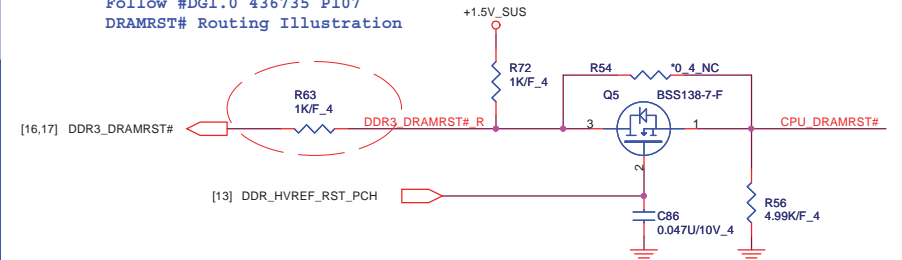
Change OD part same with PDC

Copy from PDC



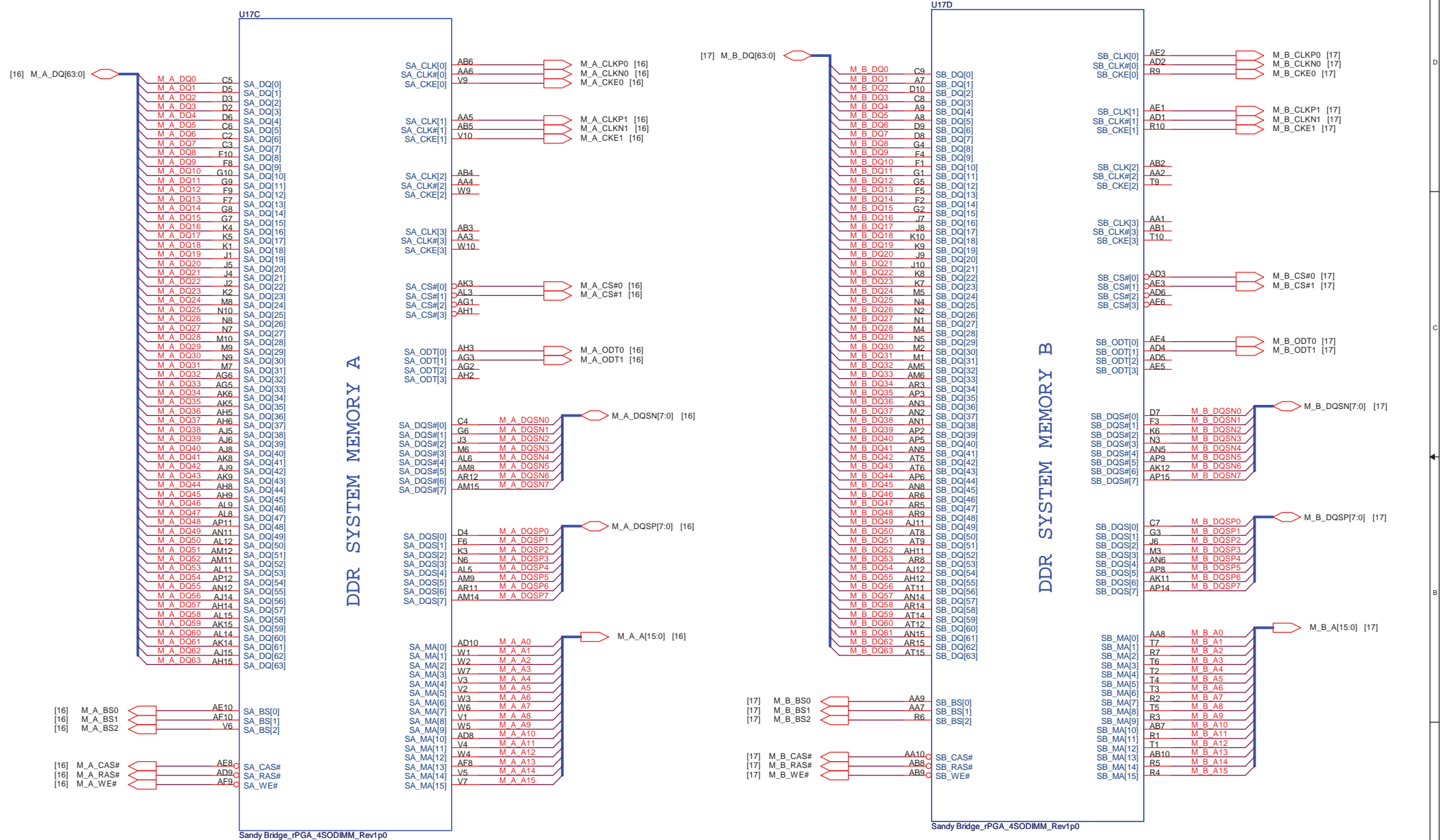
Follow #DG1.0 436735 P107

DRAMRST# Routing Illustration



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PROJECT : R03A/V03A

Sandy Bridge Processor (DDR3)



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Sandy Bridge Processor (GRAPHIC POWER)

POWER

CPU MCH
SNB 45W: 5A
330uF/6mohm
10uF x 6

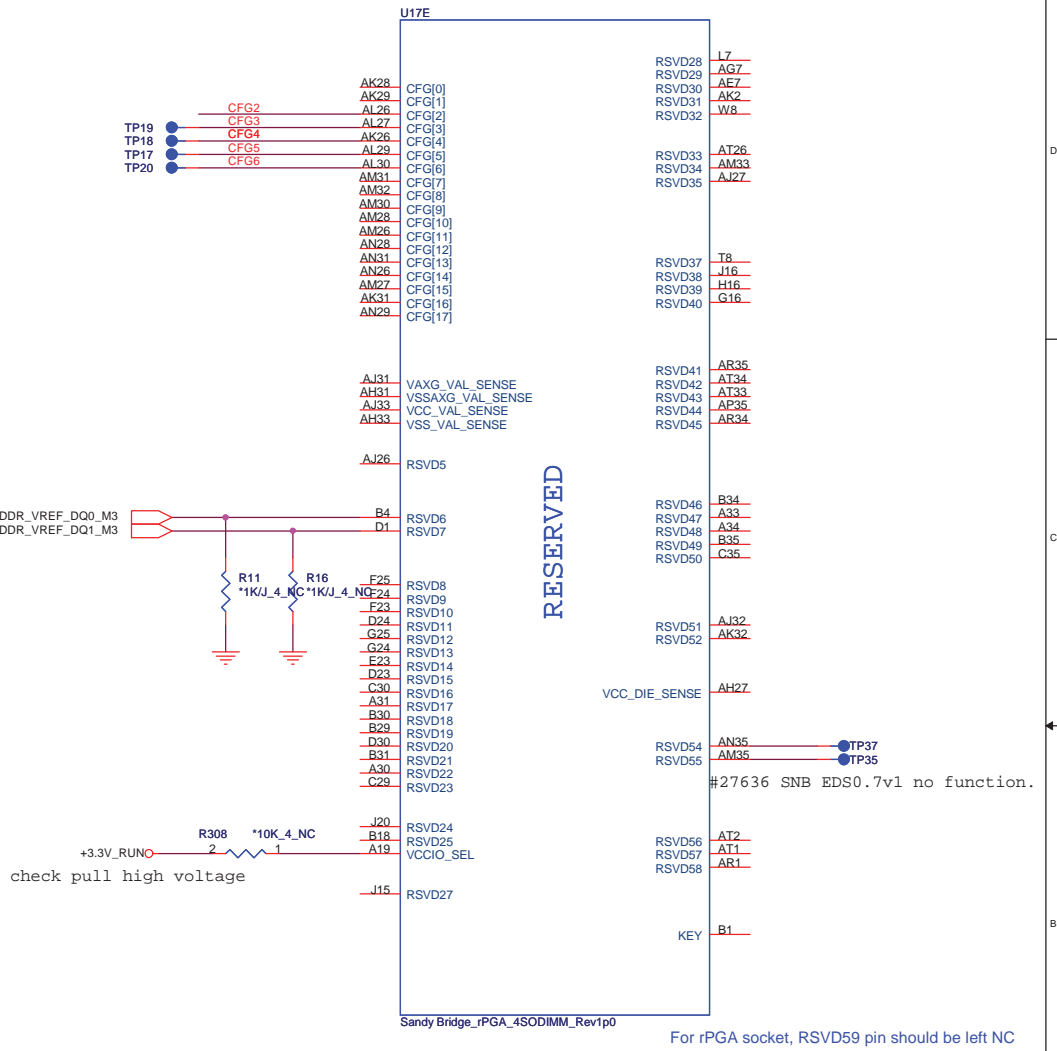
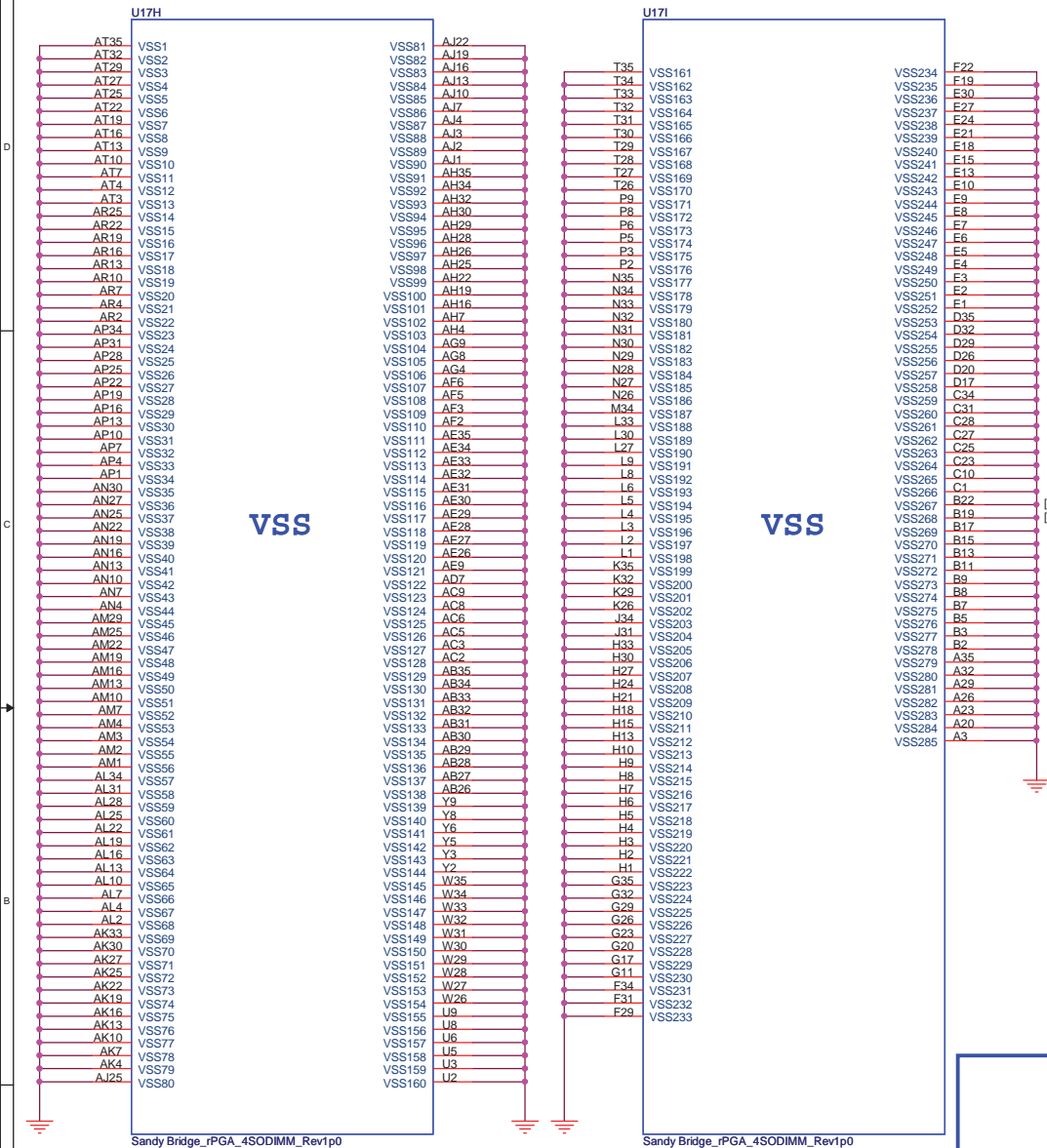
CPU SA
SNB 45W: 6A
330uF/7mohm x 1
10uF x 3

Take care Q3509 $V_{gs}(MAX)=2.5$

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Sandy Bridge Processor (GND)

Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

CFG2 R199 1K/F 4



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Cougar Point (DMI, FDI, PM)

DMI

FDI

PM

System Power Management

PCH Pull-high/low (CLG)

System PWR_OK (CLG)

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Cougar Point 1/7

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Cougar Point (DMI, FDI, PM)

DMI/FDI Interface

PM/FDI Interface

System Power Management

PCH Pull-high/low (CLG)

System PWR_OK (CLG)

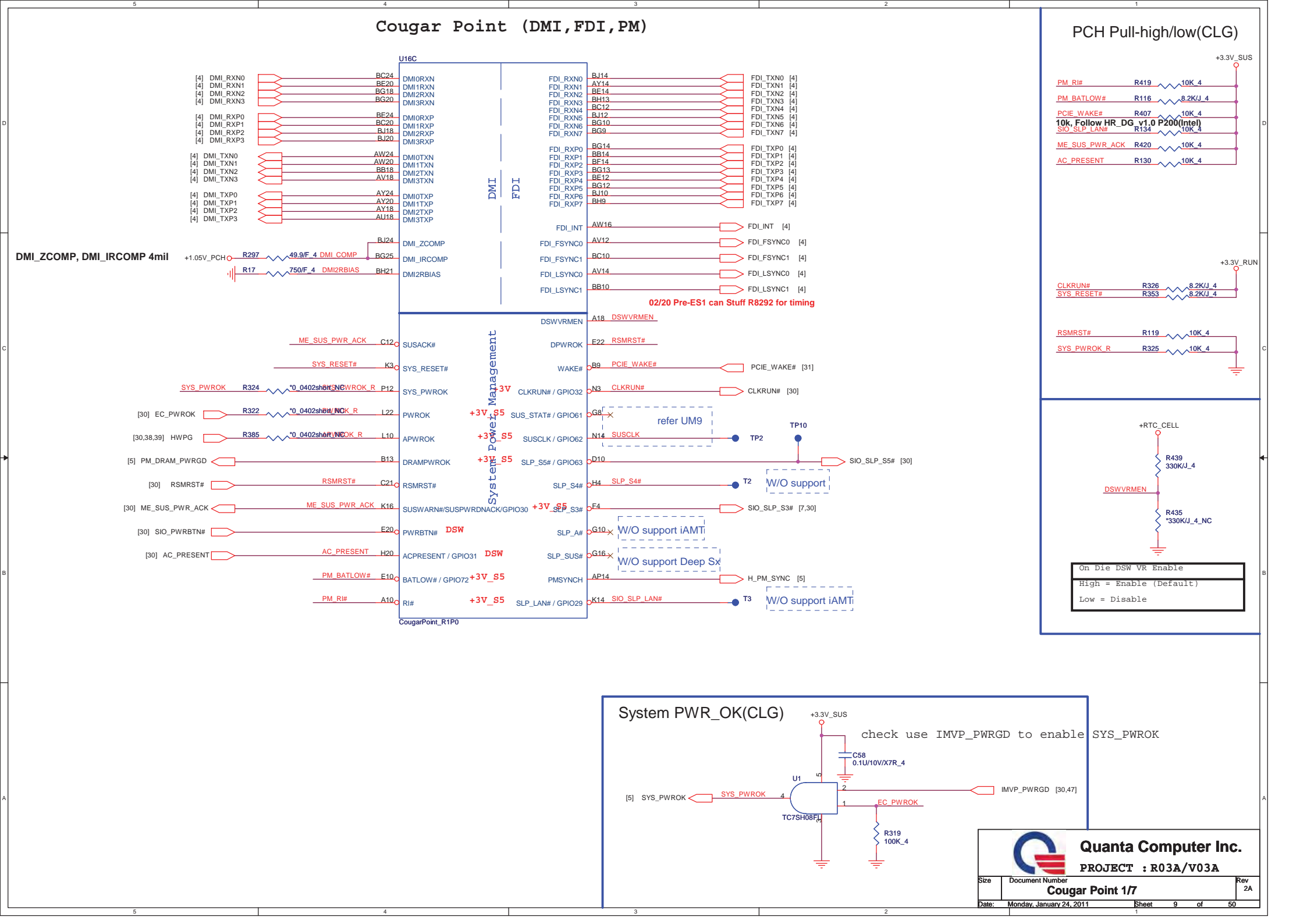
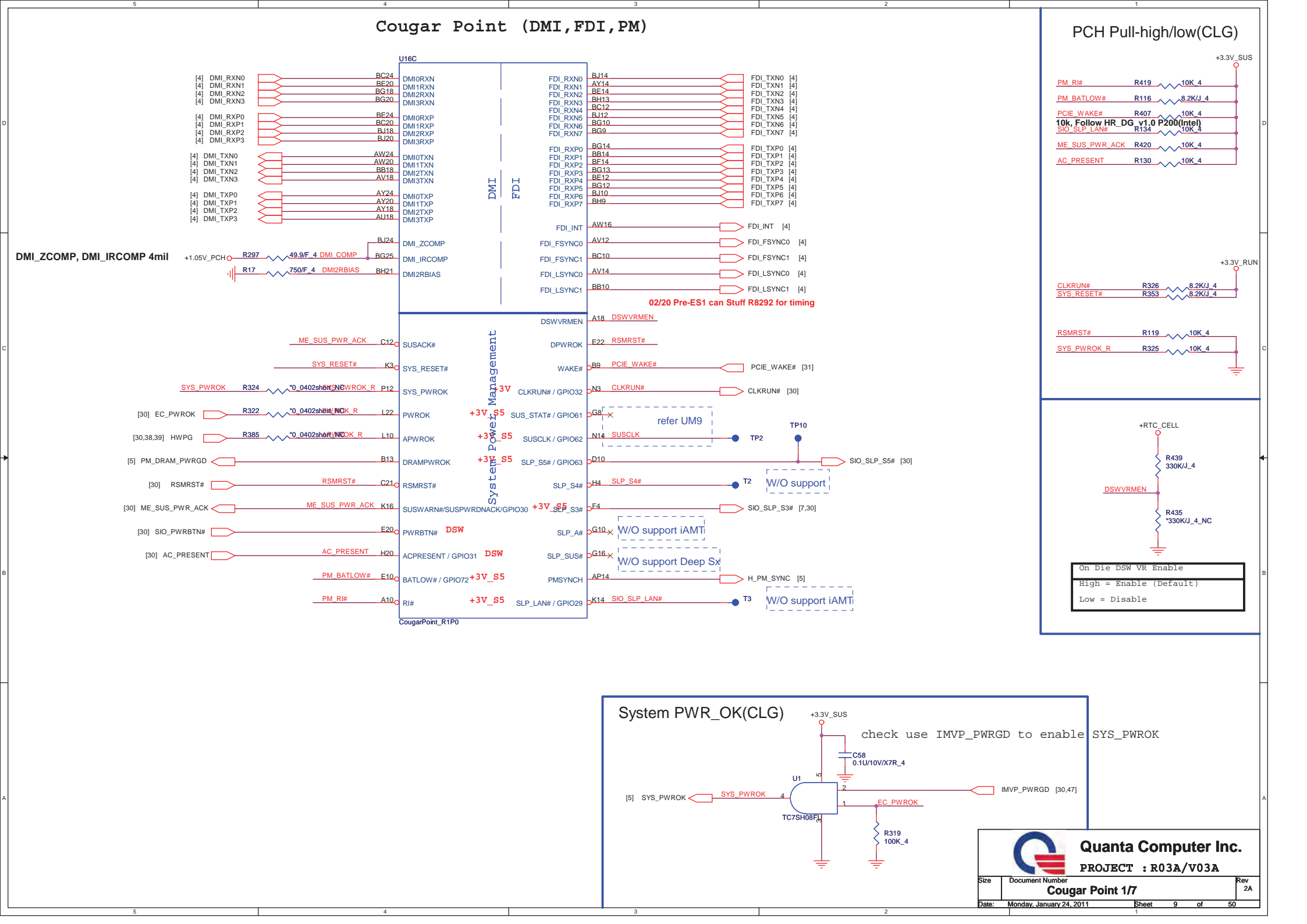
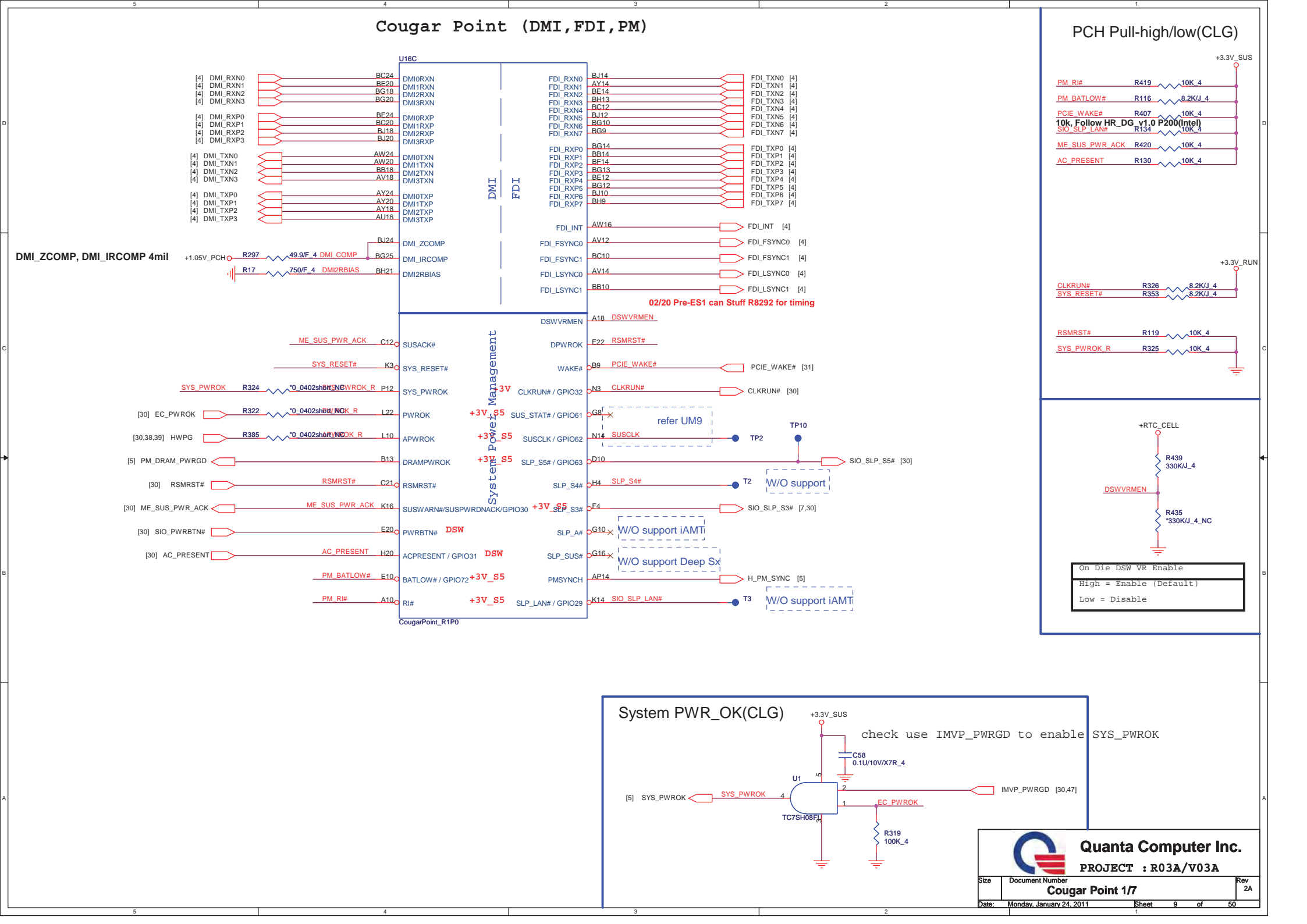
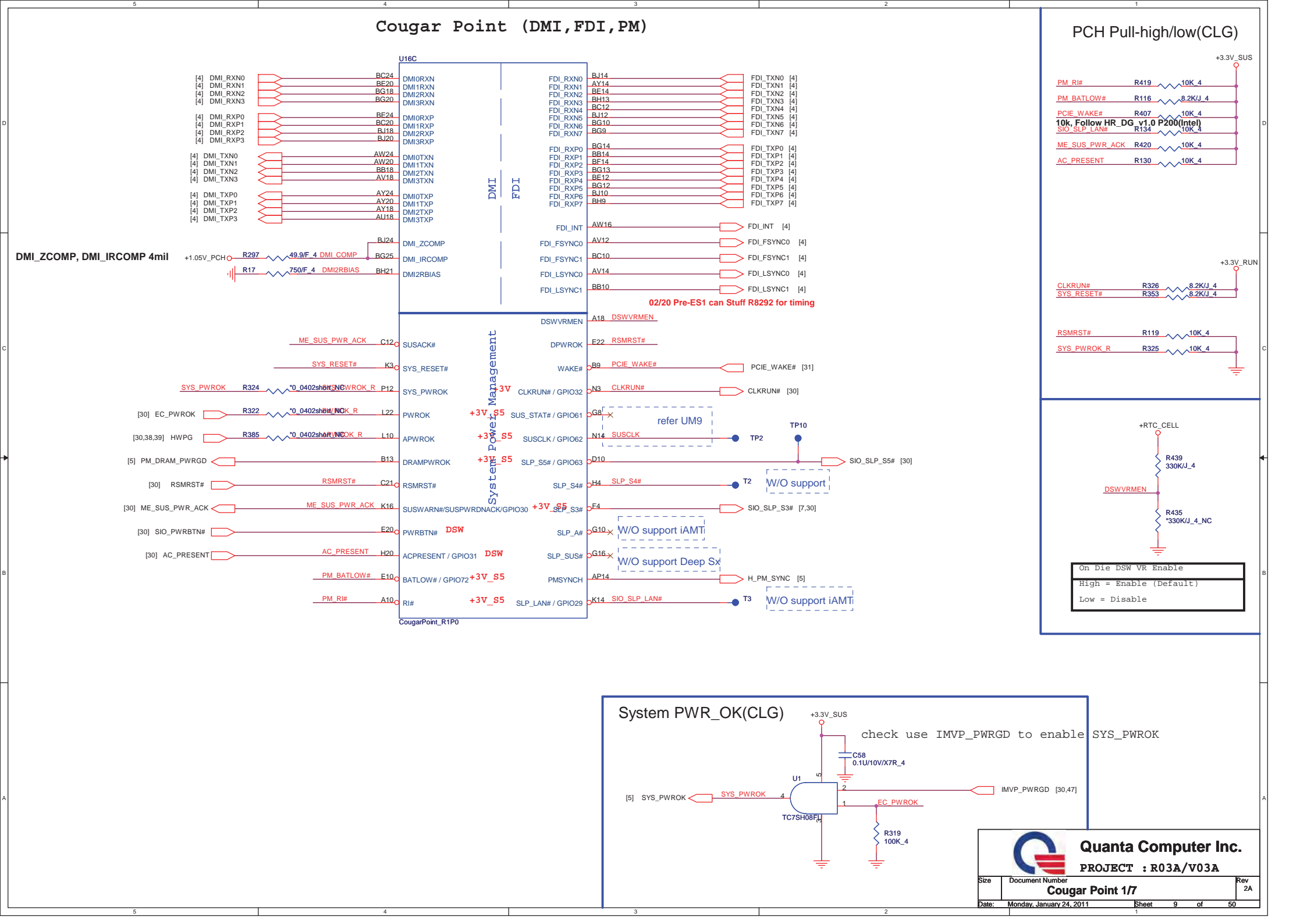
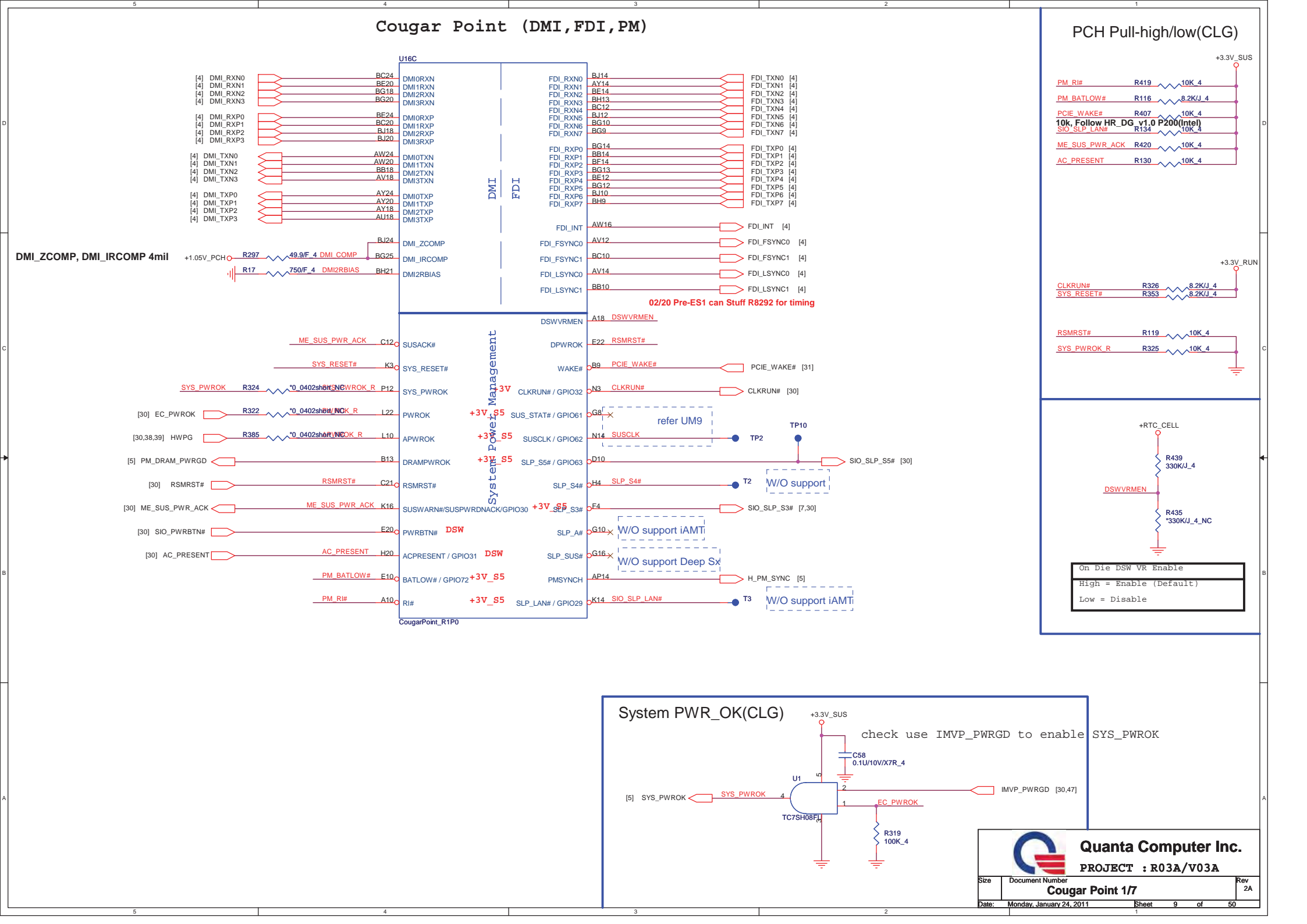
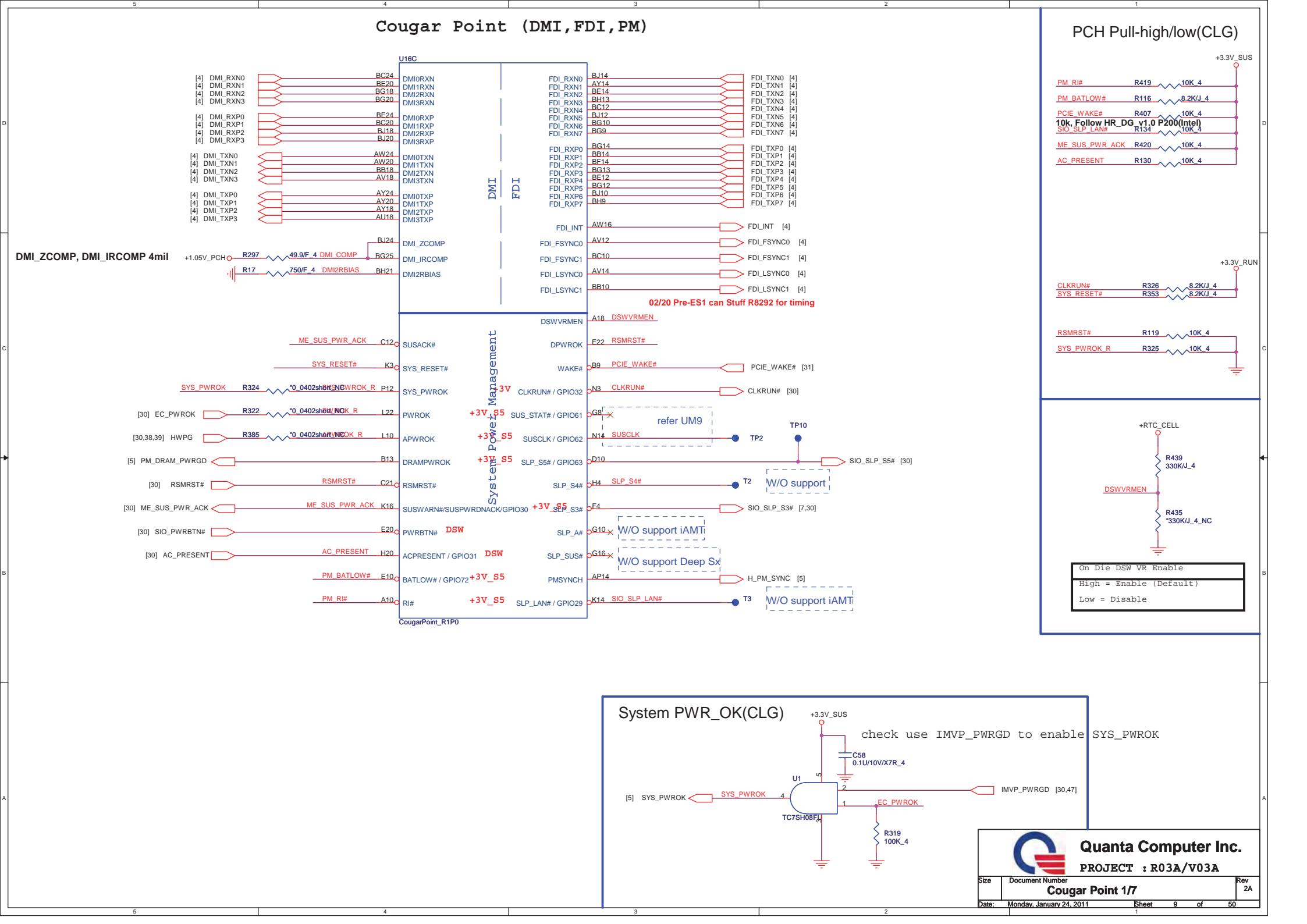
Signal	Value	Unit
PM_R#	10K	4
PM_BATLOW#	8.2K	4
PCIE_WAKE#	10K	4
SIO_SLP_LAN#	10K	4
ME_SUS_PWR_ACK	10K	4
AC_PRESENT	10K	4

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

check use IMVP_PWRGD to enable SYS_PWROK

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Cougar Point 1/7
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[illegible][illegible]

Cougar Point (DMI, FDI, PM)

U16C

DMI

FDI

PM

System Power Management

DSWVRMEN

System PWR_OK (CLG)

PCH Pull-high/low (CLG)

Notes:

- 02/20 Pre-ES1 can Stuff R8292 for timing
- 0.0402shoh/NOK R
- 0.0402shoh/NOK R

Legend:

On Die DSW VR Enable	
High	= Enable (Default)
Low	= Disable

Footer:

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Cougar Point (DMI, FDI, PM)

U16C

DMI

FDI

PM

System Power Management

DSWVRMEN

System PWR_OK (CLG)

PCH Pull-high/low (CLG)

Notes:

- 02/20 Pre-ES1 can Stuff R8292 for timing
- 0.0402shoh/NOK R
- 0.0402shoh/NOK R

Legend:

On Die DSW VR Enable	
High	= Enable (Default)
Low	= Disable

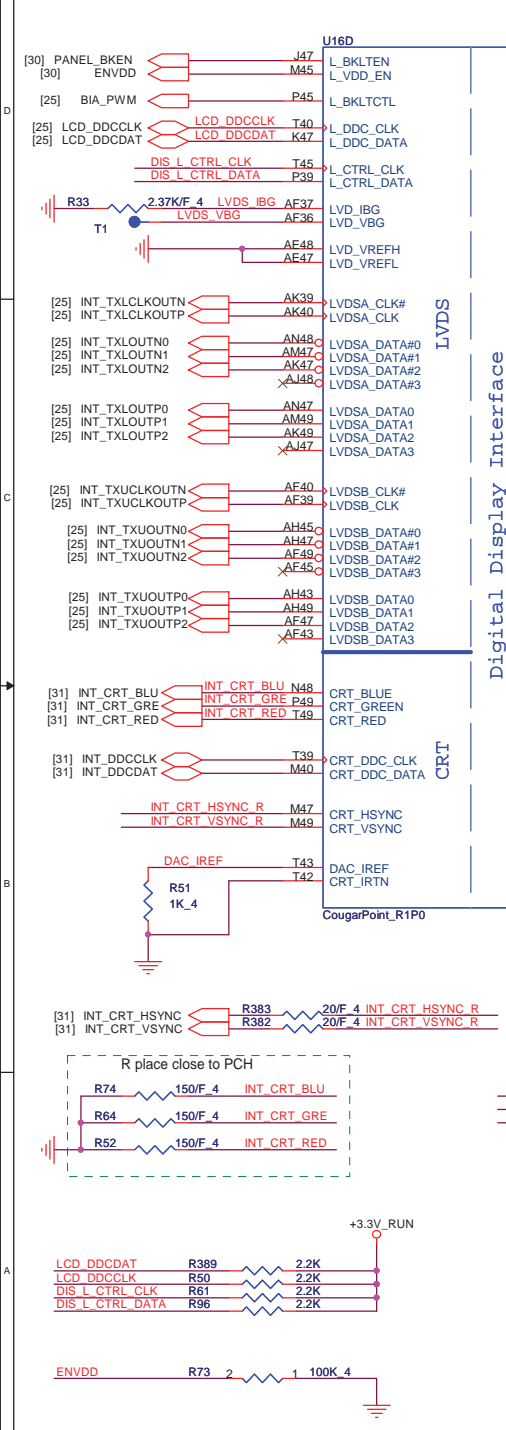
Footer:

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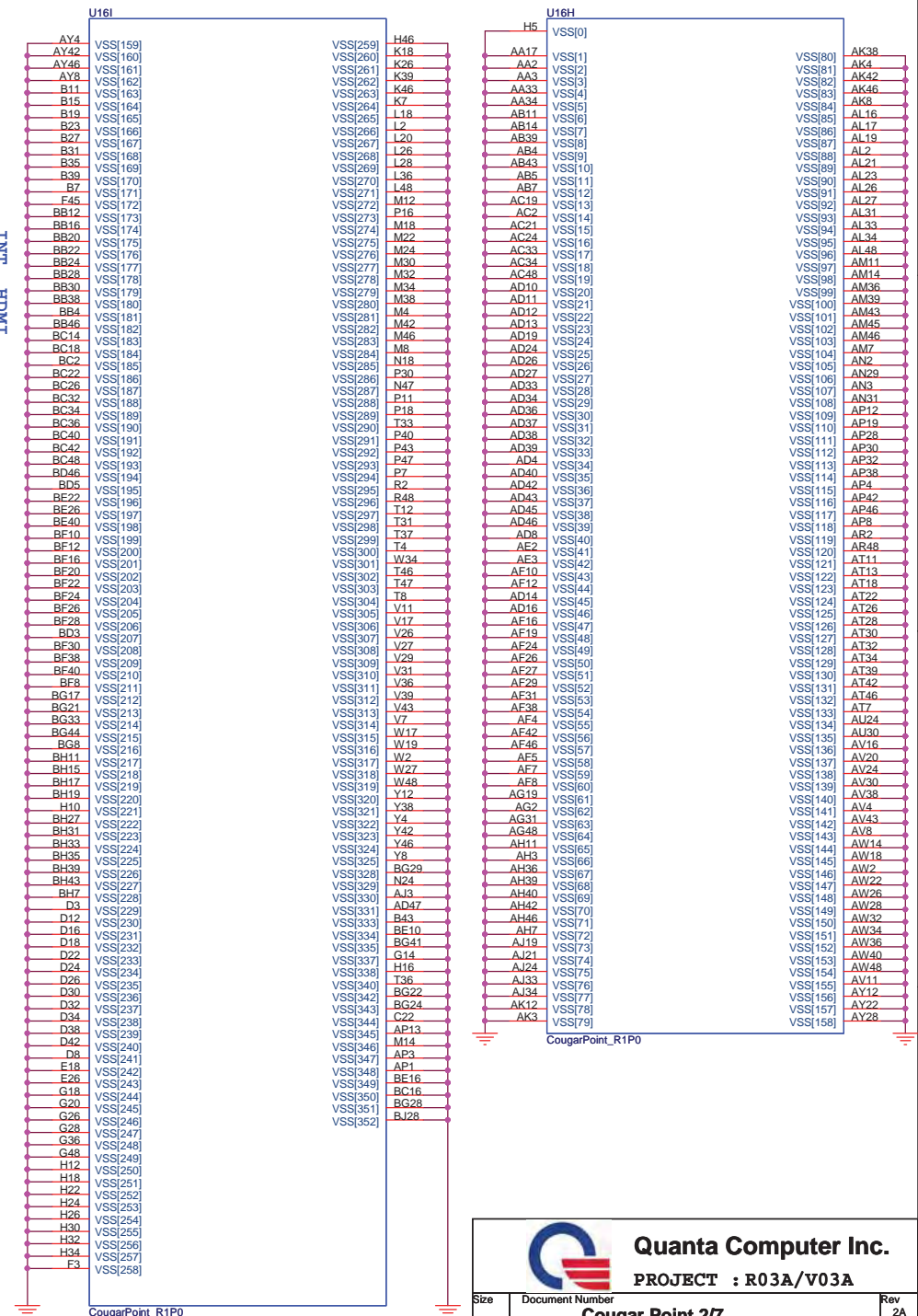
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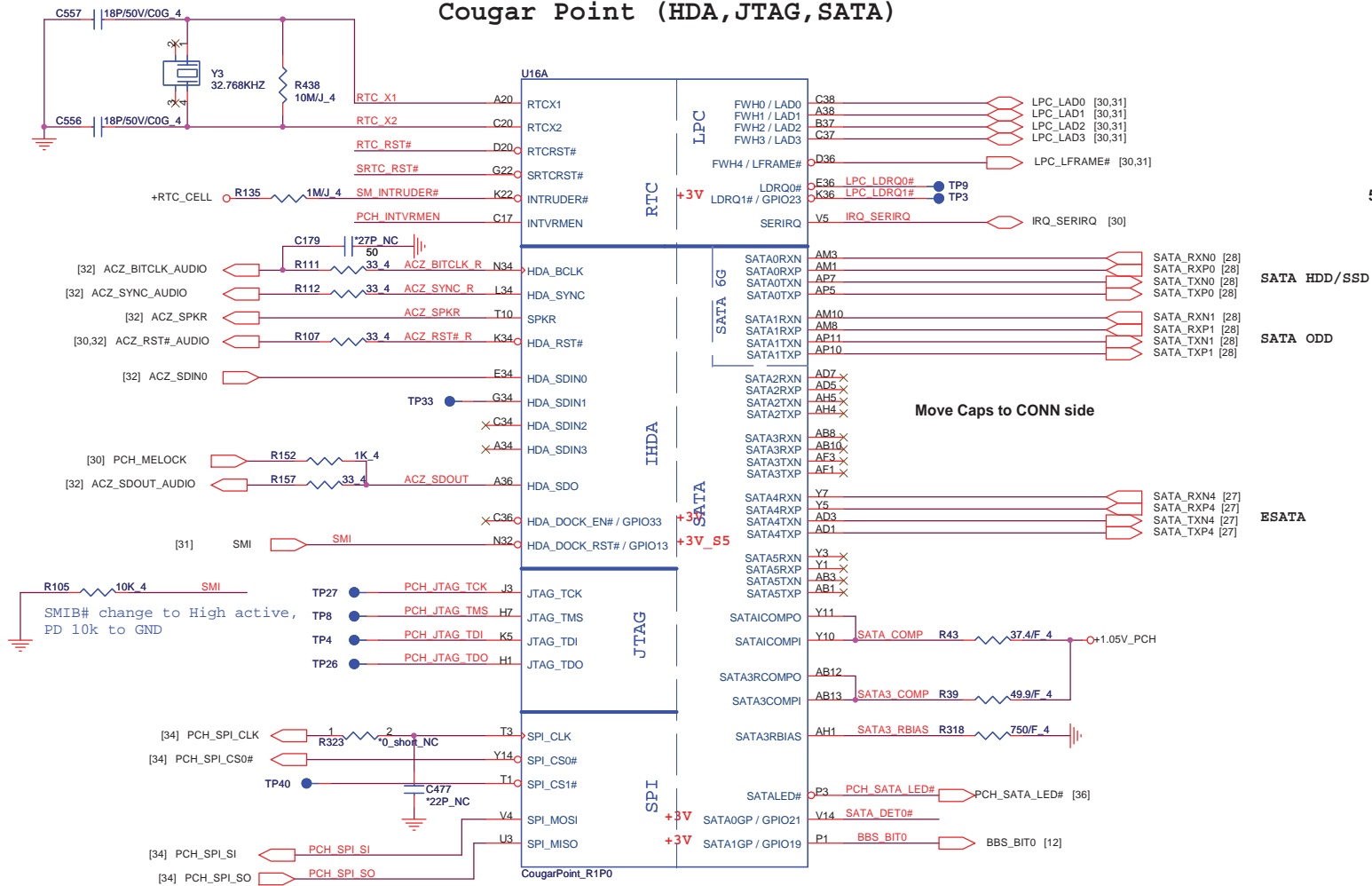
Cougar Point (LVDS, DDI)



Cougar Point (GND)

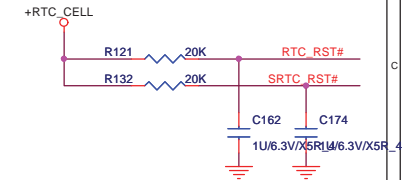
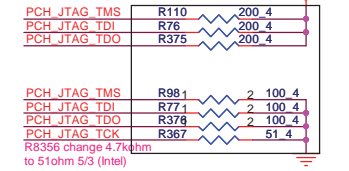


Cougar Point (HDA, JTAG, SATA)



PCH JTAG Debug (CLG)

5% fine (Intel), 210->200 (PDDG, Intel) MP remove(Intel)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_SUS R41 *1K 4 NC ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS R146 *1K 4 NC ACZ_SDOUT
Del 0510			Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R434 330K/J_4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS R118 1K 4 ACZ_SYNC_R



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Cougar Point-M (PCI,USB,NVRAM)

U16B



Controller
Link

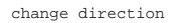
CLOCKS

add test point for XDP

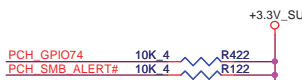
XDP

CougarPoint_R1P0

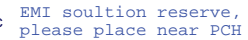
```
0727 add 22ohm resistor
```



PCIE CLK REQ0#	10K 4	R89
PCIE CLK REQ3#	10K 4	R399
PCIE CLK REQ4#	10K 4	R100
PCIE CLK REQ5#	10K 4	R123
PCIE CLK REQ6#	10K 4	R117
PCIE CLK REQ7#	10K 4	R101
PCIE CLK REQ2#	10K 4	R42
PEG B CLKRQ#	10K 4	R99



CLK_DMIN	R25	10K 4
CLK_DMIP	R29	10K 4
CLK_GND1 N		
CLK_GND1 P	R302 1	2 10K 4
CLK_BUF DREFCLKN	R126	10K 4
CLK_BUF DREFCLKP	R125	10K 4
CLK_BUF DREFSSCLKN	R31	10K 4
CLK_BUF DREFSSCLKP	R30	10K 4
CLK_PCH_14M	R78	10K 4



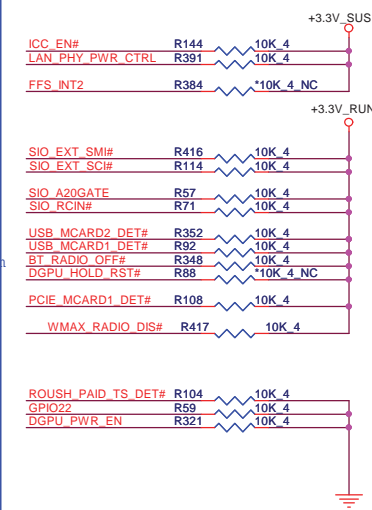
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Cougar Point (GPIO,VSS_NCTF,RSVD)

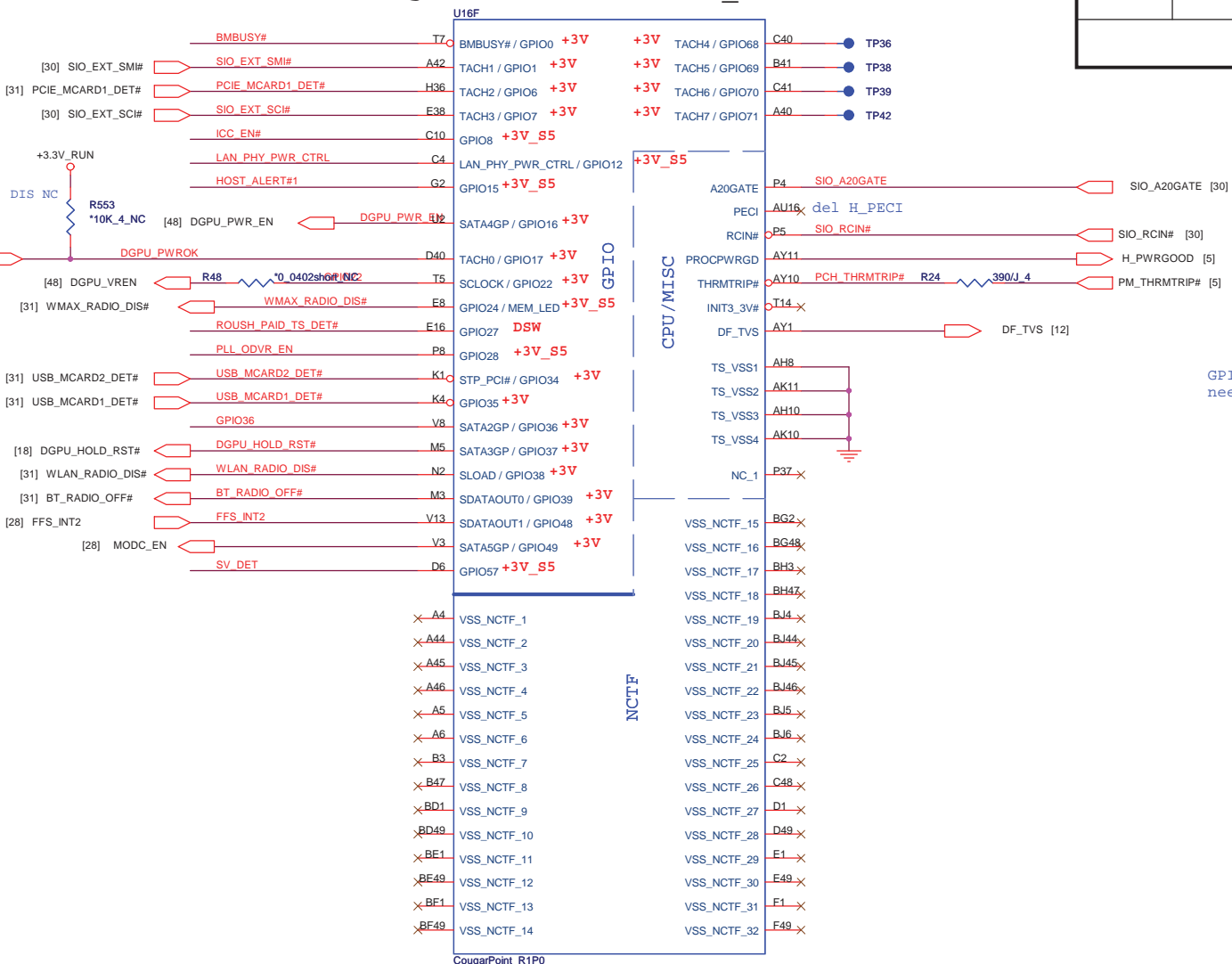
Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)



GPIO Pull-up/Pull-down(CLG)



GPIO37 follow 14" team
need INTEL confirm



CougarPoint_R1P0

DMI TERMINATION
VOLTAGE OVERRIDE

Low = Tx, Rx terminated to
same voltage (DC Coupling Mode)
(DEFAULT)

SGPIO Confirm with Intel

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is
for intel BIOS validation purpose.

BMBUSY#:
If not used, require a weak pull-up
(8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and
100 ohm on this net for validation purpose.

Intel ME Crypto Transport Layer
Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

MFG-TEST

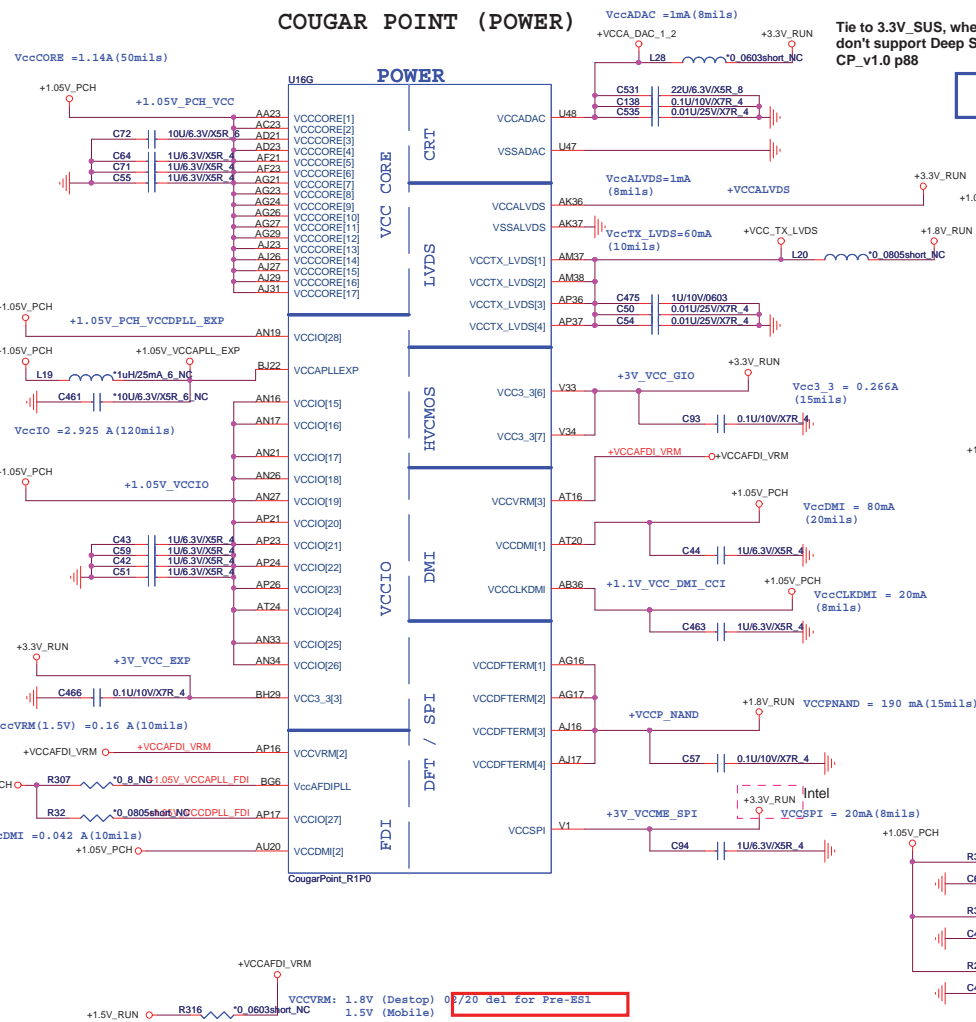
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Cougar Point 6/7

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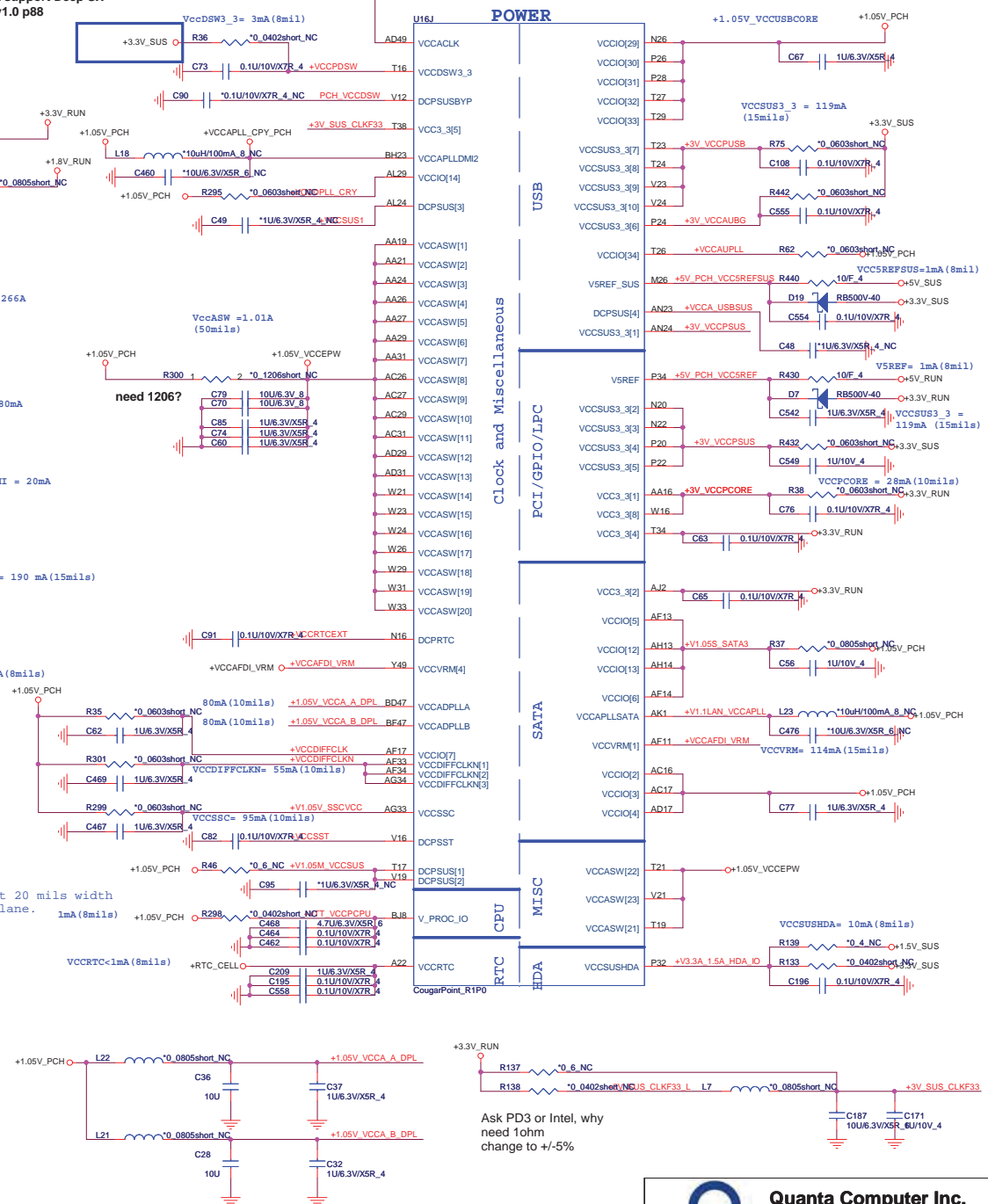
COUGAR POINT (POWER)



the trace needs to be at least 20 mils width
with full VSS/VCC reference plane. 1mA(8mils)

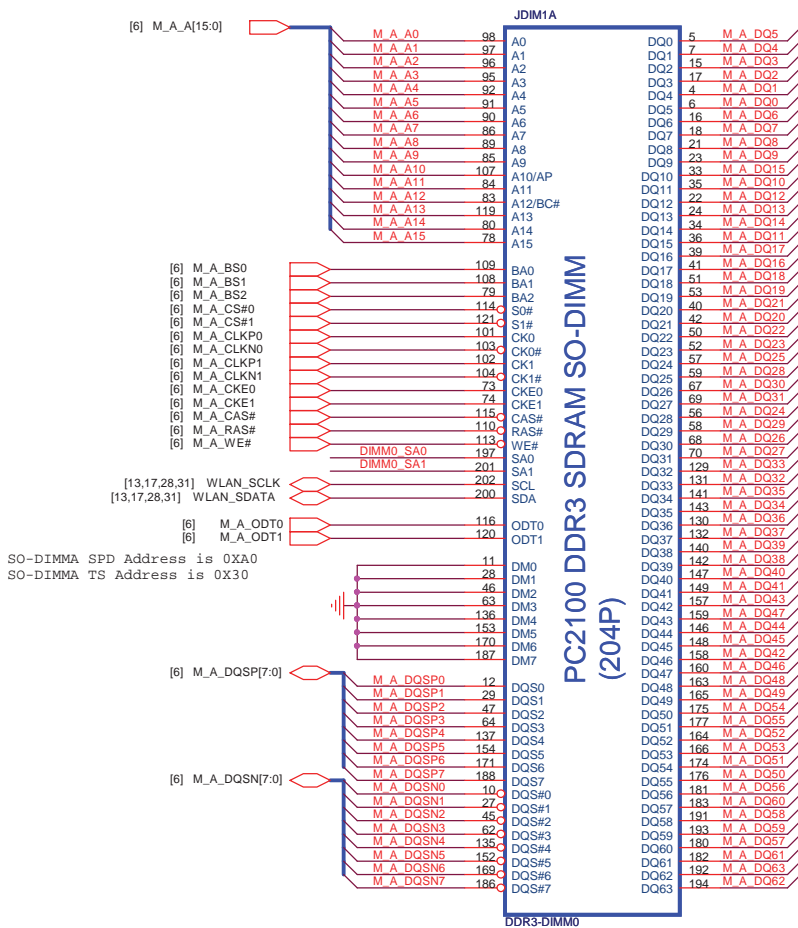
Tie to 3.3V_SUS, when
don't support Deep S
CP_v1.0 p88

Cougar Point (POWER)

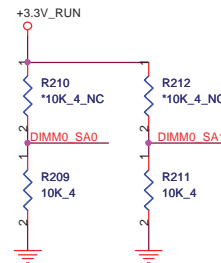


Ask PD3 or Intel, why
need 1ohm
change to +/-5%

H=8.0mm,RVS

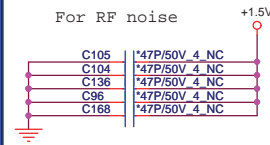
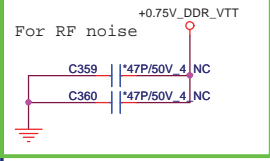
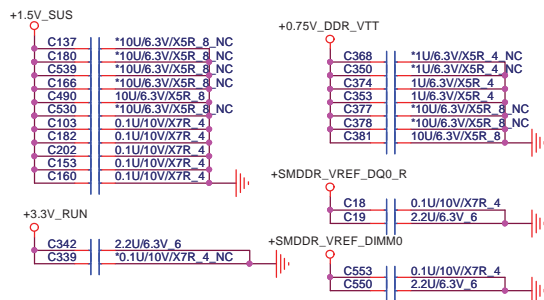


M3 reserve

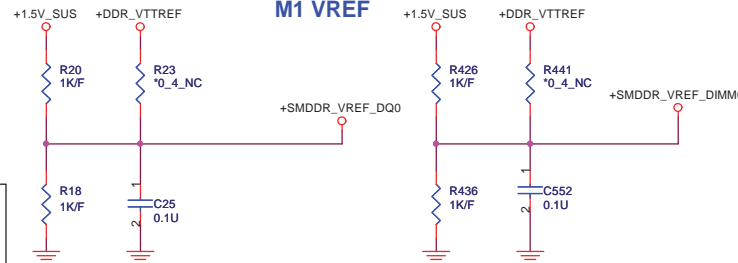


	DIMM0_SA0	DIMM0_SA1
DOMM0	0	0
DOMM1	0	1

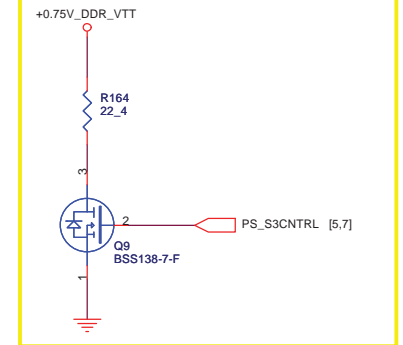
Place these Caps near So-Dimm0.



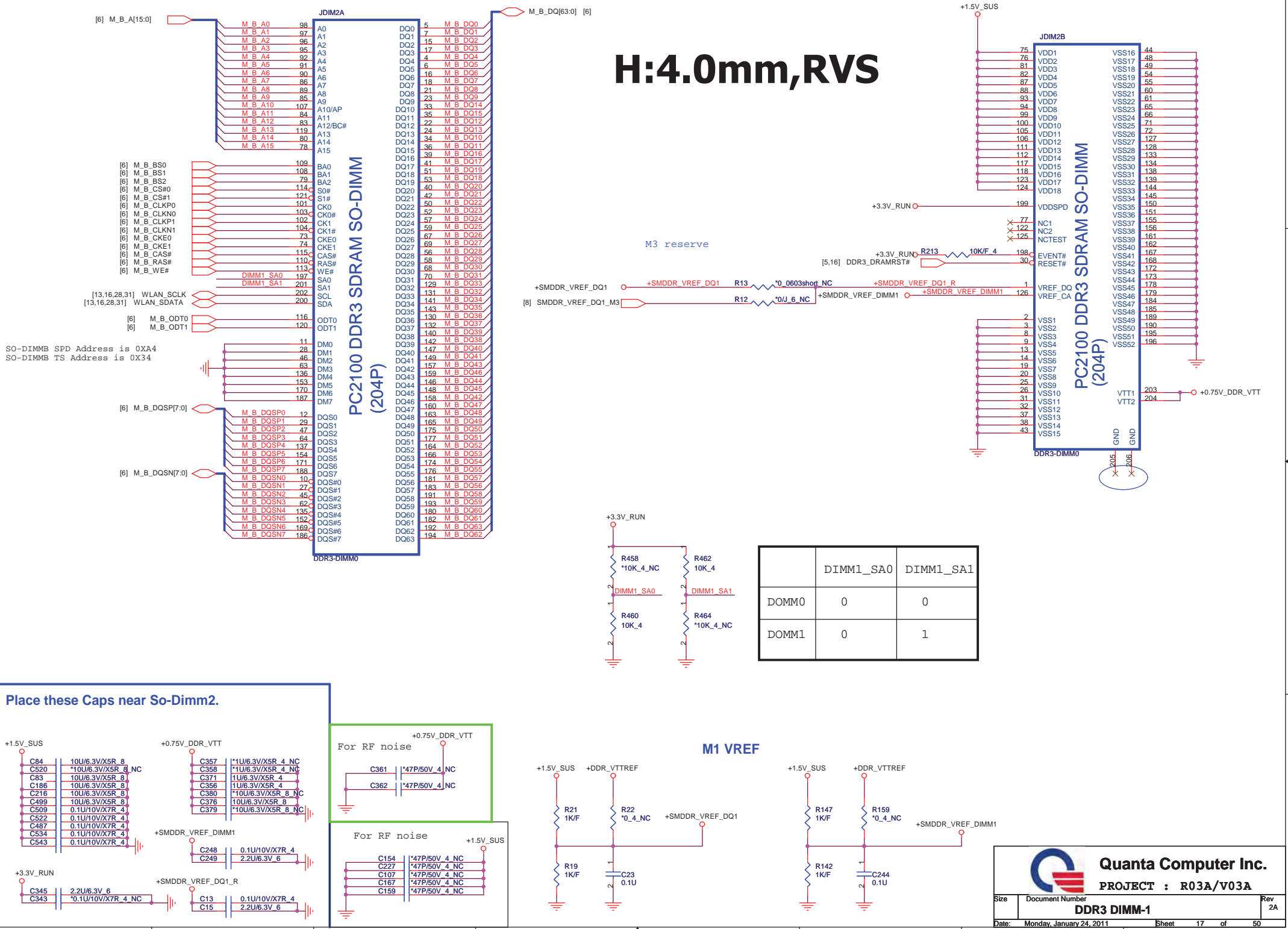
M1 VREF



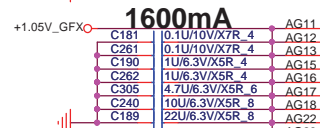
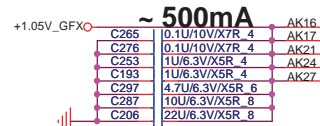
S3 Power reduce



H:4.0mm,RVS



PEX_IOVDD+PEX_IOVDDQ >2.2A



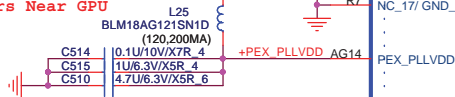
0.1u *4 under GPU
Others Near GPU

0.1u under GPU
Others Near GPU

confirm with FAE
should change power rail

12~16 mils width
120mA

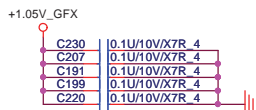
0.1u under GPU
Others Near GPU



120mA 12~16 mils width



0.1u under GPU
Others Near GPU
add 1u near GPU as FAE confirm



1211 for Nvidia request
add transition cap

U20A
N12P-GE-A1

PEX_IOVDD_1
PEX_IOVDD_2
PEX_IOVDD_3
PEX_IOVDD_4
PEX_IOVDD_5

PEX_IOVDDQ_1
PEX_IOVDDQ_2
PEX_IOVDDQ_3
PEX_IOVDDQ_4
PEX_IOVDDQ_5
PEX_IOVDDQ_6
PEX_IOVDDQ_7
PEX_IOVDDQ_8
PEX_IOVDDQ_9
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
PEX_IOVDDQ_13
PEX_IOVDDQ_14
PEX_IOVDDQ_15
PEX_IOVDDQ_16
PEX_IOVDDQ_17
PEX_IOVDDQ_18
PEX_IOVDDQ_19
PEX_IOVDDQ_20
PEX_IOVDDQ_21
PEX_IOVDDQ_22
PEX_IOVDDQ_23
PEX_IOVDDQ_24
PEX_IOVDDQ_25

PCI EXPRESS

AG20 PEX_PLL_HVDD_NC
A2 NC.1
AB7 NC.2
AD6 NC.3
AF6 NC.4
AG6 NC.5
AJ5 NC.6
AK5 NC.7
AL7 NC.8
AM7 NC.11
AP6 NC.13
AU7 NC.15
AV6 NC.18
AW6 NC.19

PEX_RX0
PEX_RX1
PEX_RX11
PEX_RX2
PEX_RX3
PEX_RX31
PEX_RX4
PEX_RX41
PEX_RX5
PEX_RX51
PEX_RX6
PEX_RX61
PEX_RX7
PEX_RX71
PEX_RX8
PEX_RX81
PEX_RX9
PEX_RX91
PEX_RX10
PEX_RX11
PEX_RX111
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PEX_RX131
PEX_RX14
PEX_RX141
PEX_RX15
PEX_RX151

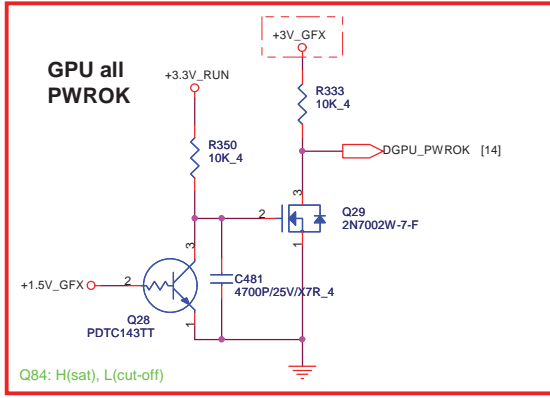
PEX_TX0
PEX_TX01
PEX_TX1
PEX_TX11
PEX_TX2
PEX_TX21
PEX_TX3
PEX_TX31
PEX_TX4
PEX_TX41
PEX_TX5
PEX_TX51
PEX_TX6
PEX_TX61
PEX_TX7
PEX_TX71
PEX_TX8
PEX_TX81
PEX_TX9
PEX_TX91
PEX_TX10
PEX_TX101
PEX_TX11
PEX_TX111
PEX_TX12
PEX_TX121
PEX_TX13
PEX_TX131
PEX_TX14
PEX_TX141
PEX_TX15
PEX_TX151

PEX_REFCLK
PEX_REFCLK1
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT1
PEX_RST#
PEX_CLKREQ#
PEX_TERM#
TESTMODE

AP17 PEG_TXP15
AN17 PEG_TXP15
AN19 PEG_TXP14
AN19 PEG_TXP14
AN19 PEG_TXP14
AN19 PEG_TXP14
AN20 PEG_TXP13
AN20 PEG_TXP13
AN20 PEG_TXP13
AN20 PEG_TXP13
AN22 PEG_TXP11
AR22 PEG_TXP10
AR22 PEG_TXP10
AR22 PEG_TXP10
AR22 PEG_TXP10
AR23 PEG_TXP10
AP23 PEG_TXP9
AN23 PEG_TXP9
AN25 PEG_TXP8
AR25 PEG_TXP8
AR25 PEG_TXP7
AR26 PEG_TXP7
AR26 PEG_TXP7
AR26 PEG_TXP7
AR26 PEG_TXP7
AR26 PEG_TXP6
AN26 PEG_TXP6
AN28 PEG_TXP5
AP28 PEG_TXP5
AR28 PEG_TXP4
AR29 PEG_TXP4
AN29 PEG_TXP3
AN29 PEG_TXP3
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AP31 PEG_TXP2
AR31 PEG_TXP1
AR32 PEG_TXP1
AR34 PEG_TXP0
AP34 PEG_TXP0

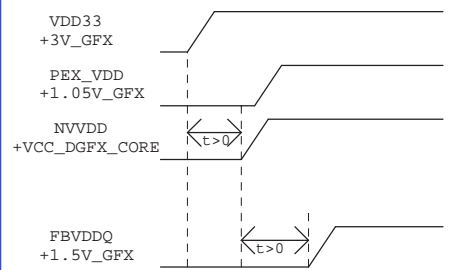
AL17 PEG_RXP15 C
AM17 PEG_RXP15 C
AM18 PEG_RXP14 C
AM18 PEG_RXP14 C
AM18 PEG_RXP14 C
AM18 PEG_RXP14 C
AL19 PEG_RXP13 C
AK19 PEG_RXP13 C
AL20 PEG_RXP12 C
AM20 PEG_RXP12 C
AM21 PEG_RXP11 C
AM22 PEG_RXP11 C
AL22 PEG_RXP10 C
AK22 PEG_RXP10 C
AL23 PEG_RXP9 C
AM23 PEG_RXP9 C
AM24 PEG_RXP8 C
AM25 PEG_RXP8 C
AL25 PEG_RXP7 C
AK25 PEG_RXP7 C
AL26 PEG_RXP6 C
AM26 PEG_RXP6 C
AM27 PEG_RXP5 C
AM28 PEG_RXP5 C
AL28 PEG_RXP4 C
AK28 PEG_RXP4 C
AL29 PEG_RXP3 C
AM29 PEG_RXP3 C
AM30 PEG_RXP2 C
AM31 PEG_RXP2 C
AM32 PEG_RXP1 C
AN32 PEG_RXP0 C
AP32 PEG_RXP0 C

AR16 CLK_PCIE_VGAP
AR17 CLK_PCIE_VGAN
AJ17 PEX_TSTCLK R158
AJ18 PEX_TSTCLK#
AM16 GPU_RST#
AR13 PEX_CLKREQ# R403
AG21 PEX_TERM# R169
AP35 TESTMODE R456

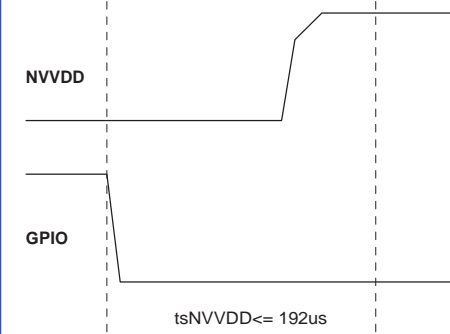


Q84: H(sat), L(cut-off)

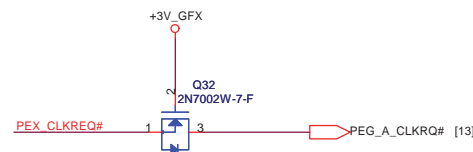
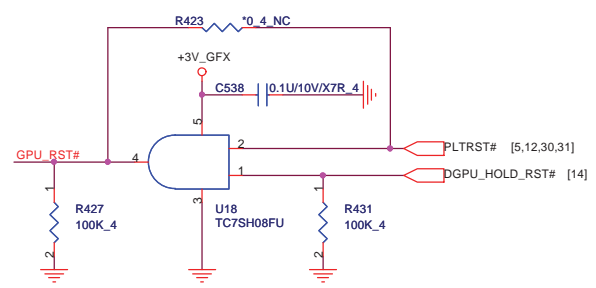
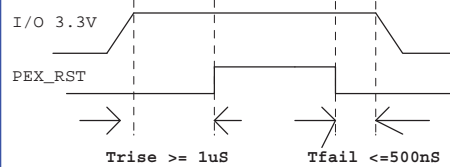
Power up sequence



NB9M: VGACORE +0.90V (Normal) , +1.09V
NVVDD Maximum Settling Time



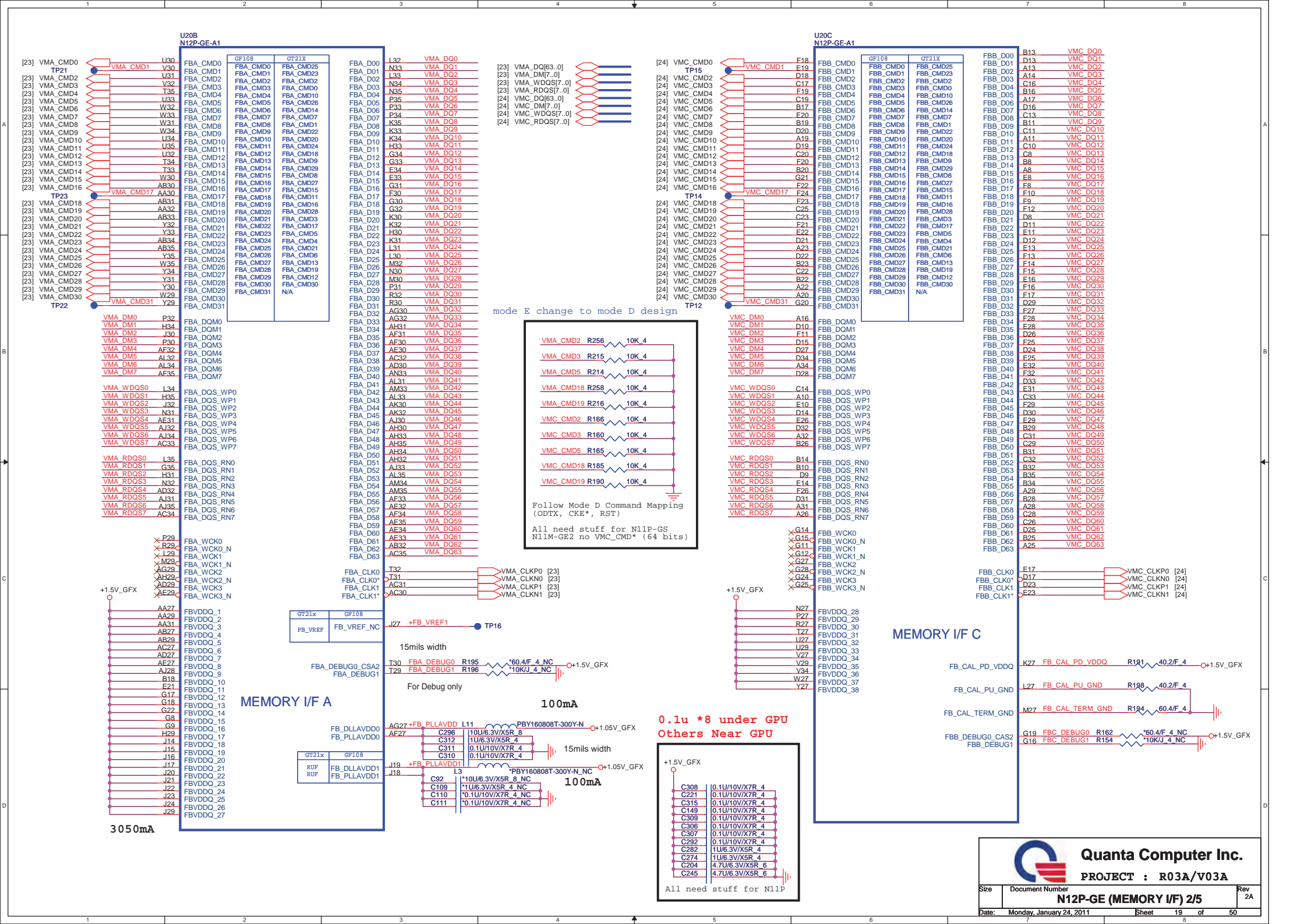
PEX_RST timing



Add MOS for preventing leakage.

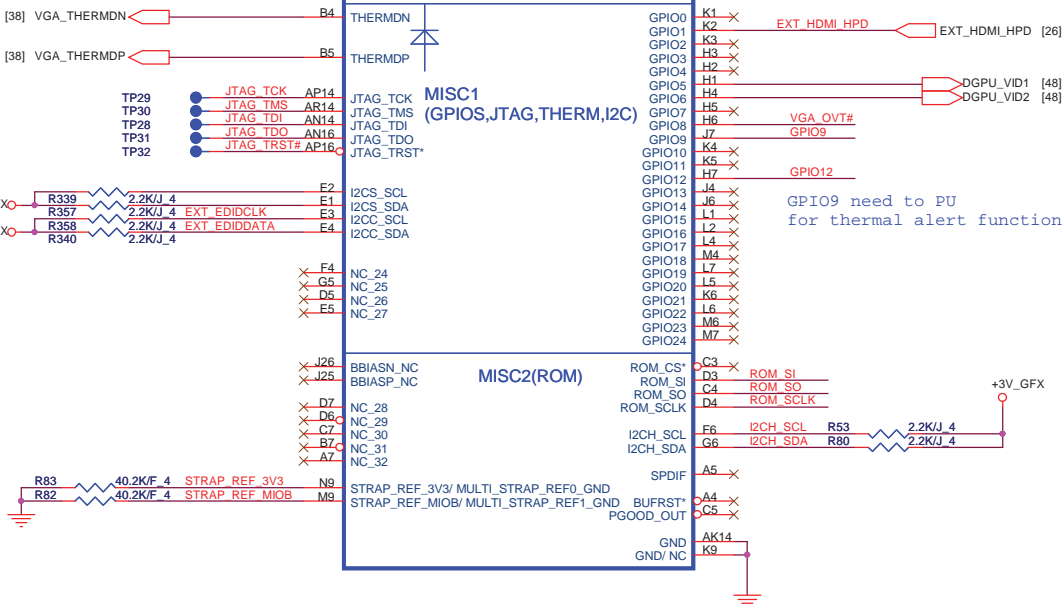


Quanta Computer Inc.
PROJECT : R03A/V03A



N11P-GS	N12P-GE
floating	floating

FAE confirm N11P could be floating



CHIP	PCI_DEVID:	STRAP2	ROM_SCLK
N11P-GS	0xDF0	0000 PD 5K	1010 PU 15K
N12P-GE	0xDF5	0101 PD 30K	1010 PU 15K

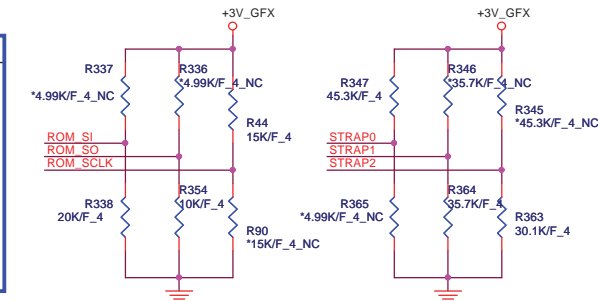
Default: N12P-GE

AJ0N11M0T24
70=0111 0000(device ID:10000)
FE=1111 1110(device ID:11110)
AJ0N11P0T22

Check N11P-GS and N12P-GE

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1%(0402)]
4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1%(0402)]
20K/F 4: CS32002FB29 [RES CHIP 20K 1/16W +1%(0402)]
30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1%(0402)]
35.7K/F 4: CS33572FB13 [RES CHIP 35.7K 1/16W +1%(0402)]
45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1%(0402)]

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PL_LN_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0010
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

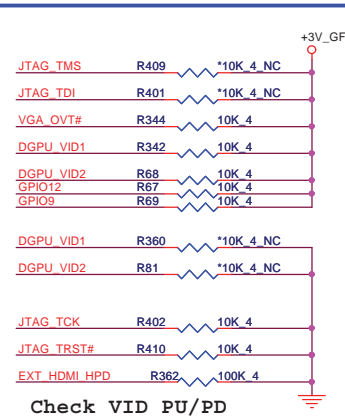
Default: Hynix VRAM 1G (0110)

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000	Reserved	Reserved		PD 5K
0001	Reserved	Reserved		PD 10K
0010	DDR3 64Mx16, 900MHz	Hynix	H5TQ1G63DFR-11C	PD 15K
0011	DDR3 64Mx16, 900MHz	Samsung	K4W1G1646E-HC11	PD 20K
0110	DDR3 128Mx16, 900MHz	Hynix	H5TQ2G63BFR-11C	PD 35K
0111	DDR3 128Mx16, 900MHz	Samsung	K4W2G1646C-HC11	PD 45K

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVD VID0
6	OUT	N/A	NVVD VID1
7	OUT	N/A	NVVD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL



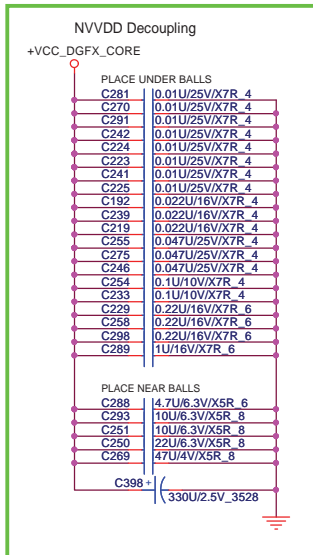
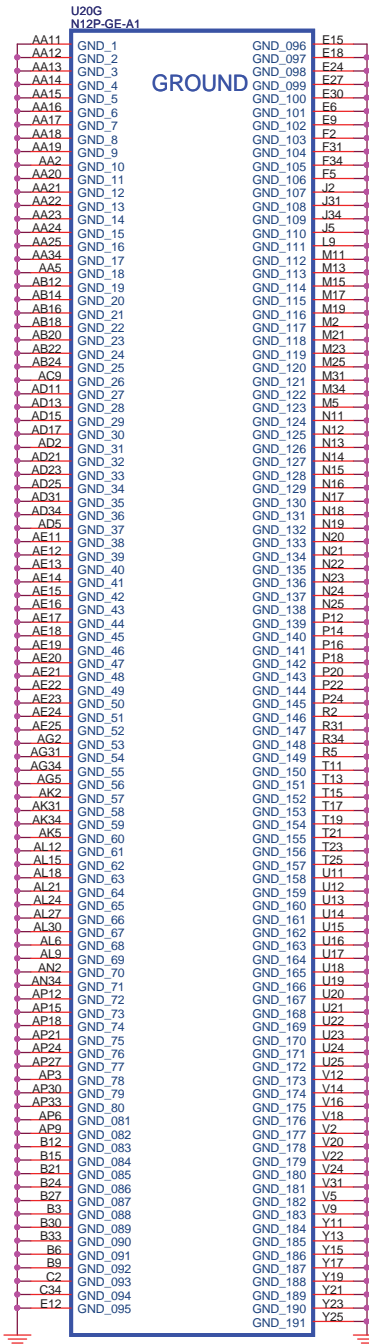
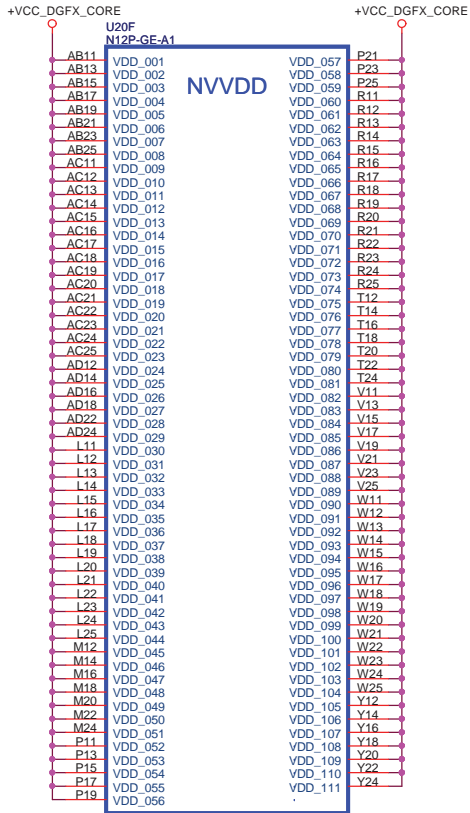
Check VID PU/PD



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PROJECT : R03A/V03A

Size	Document Number	Rev
	N12P-GE (GPIO&STRAPS) 4/5	2A
Date:	Friday, January 07, 2011	Sheet 21 of 50



Quanta Computer Inc.

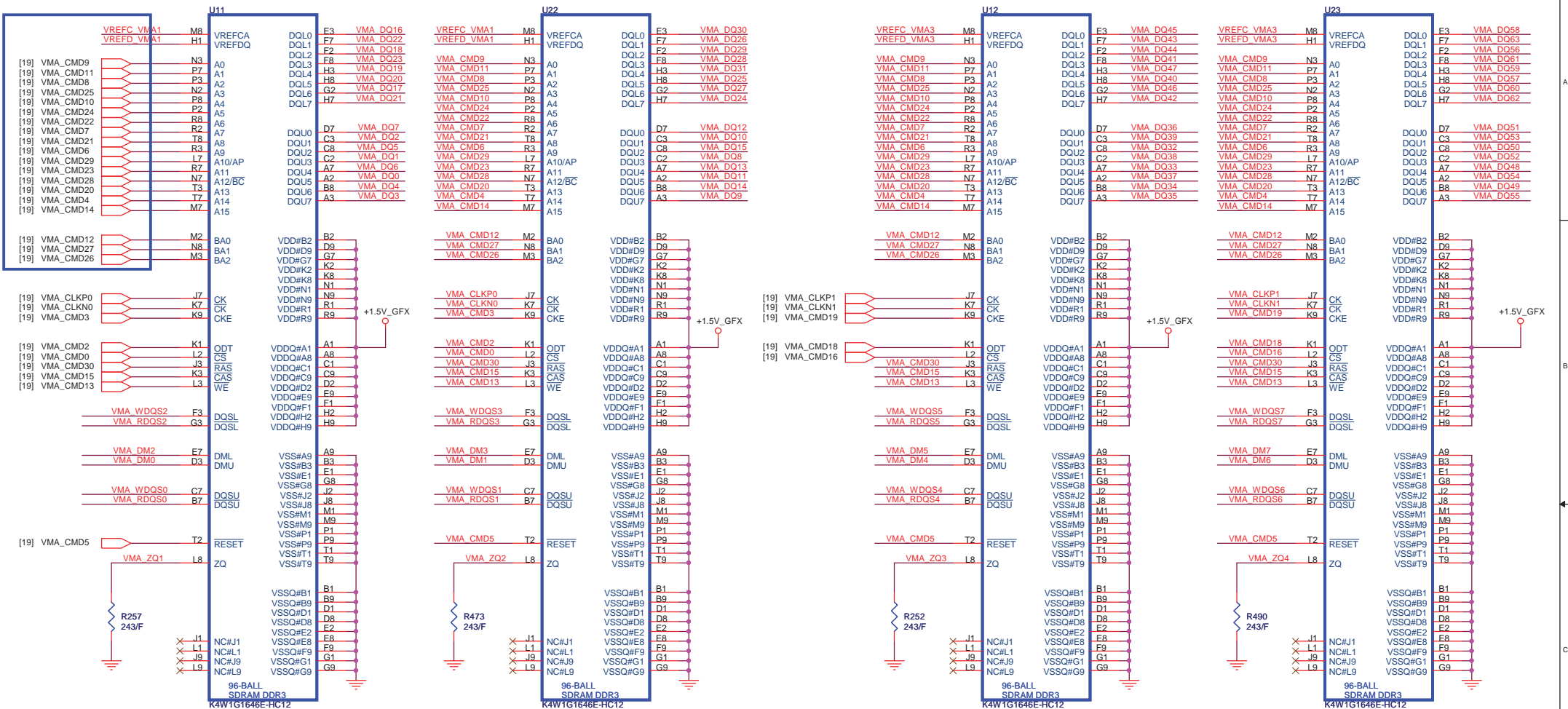
PROJECT : R03A/V03A

SWAP CMD NET
modify Mode E to Mode D


[19] VMA_DQ[63..0]
[19] VMA_DM[7..0]
[19] VMA_WDQS[7..0]
[19] VMA_RDQS[7..0]

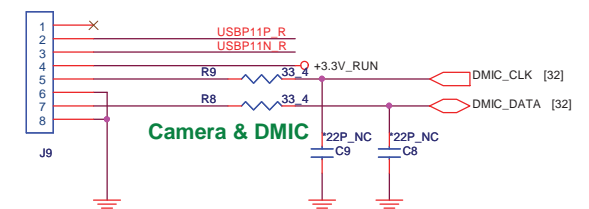
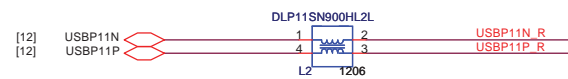
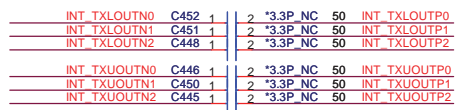
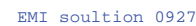
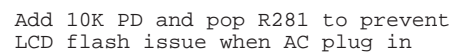
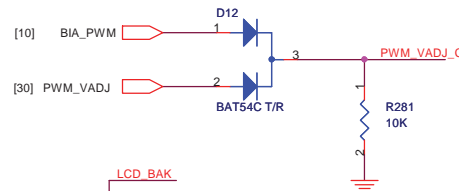
CHANNEL A: 512MB/1024MB DDR3

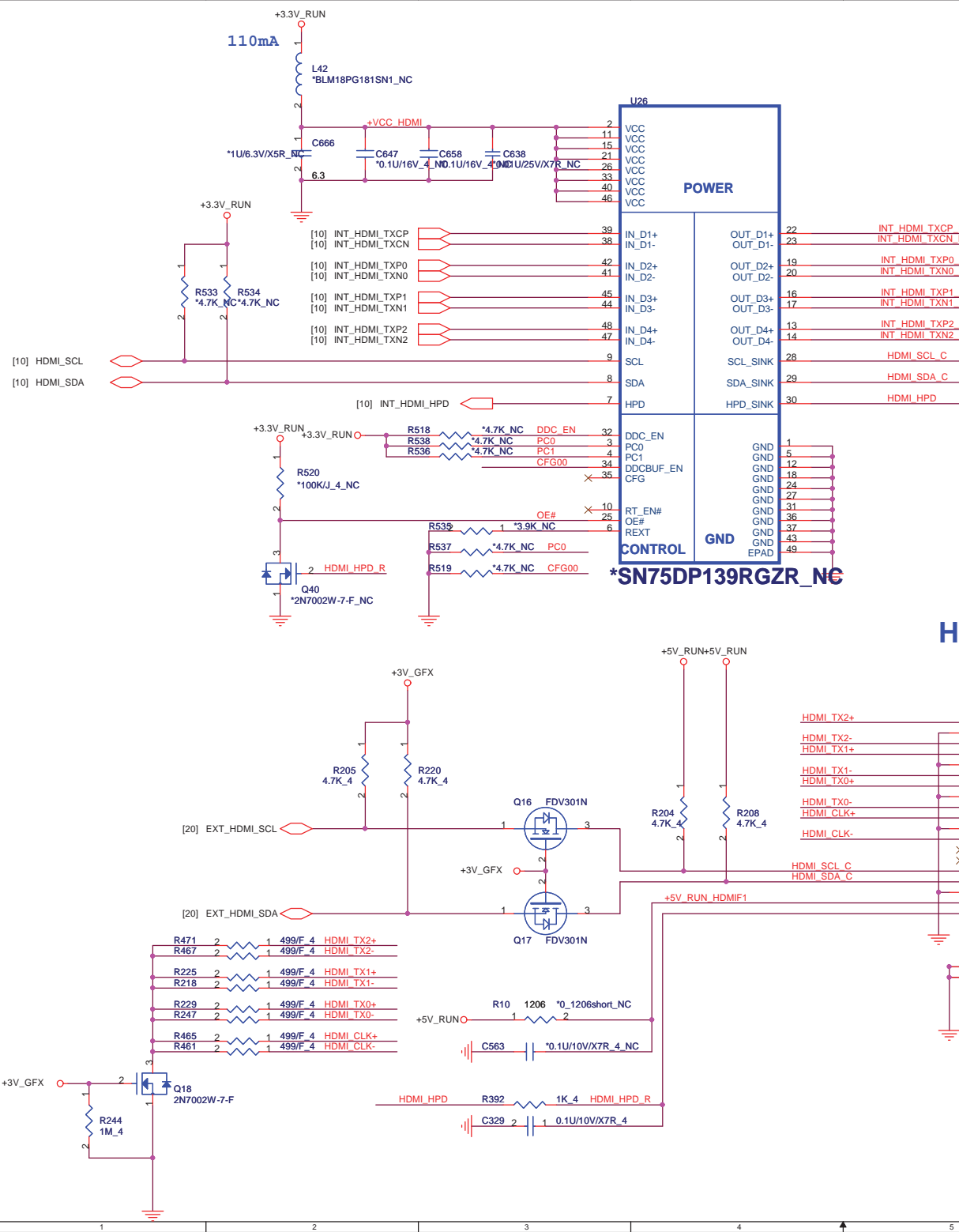
change VRAM footprint to hynix 2G(the package is bigger)



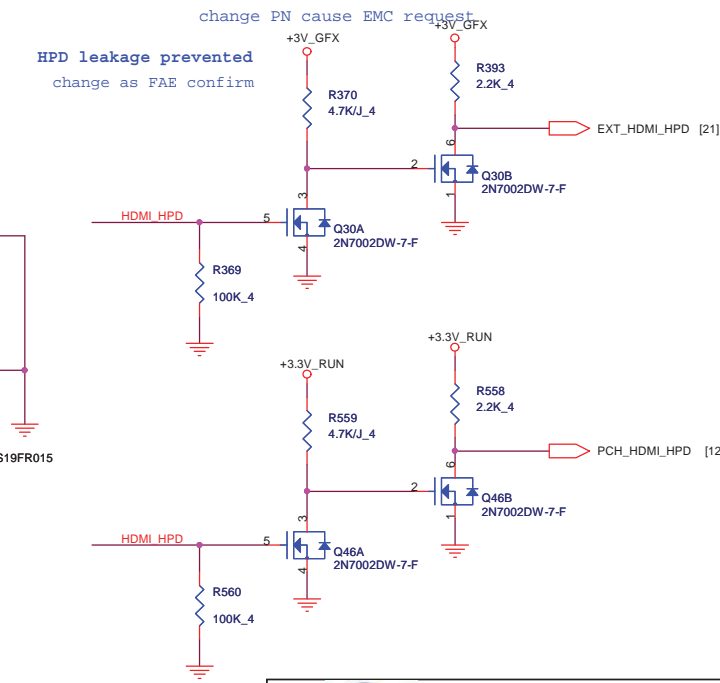
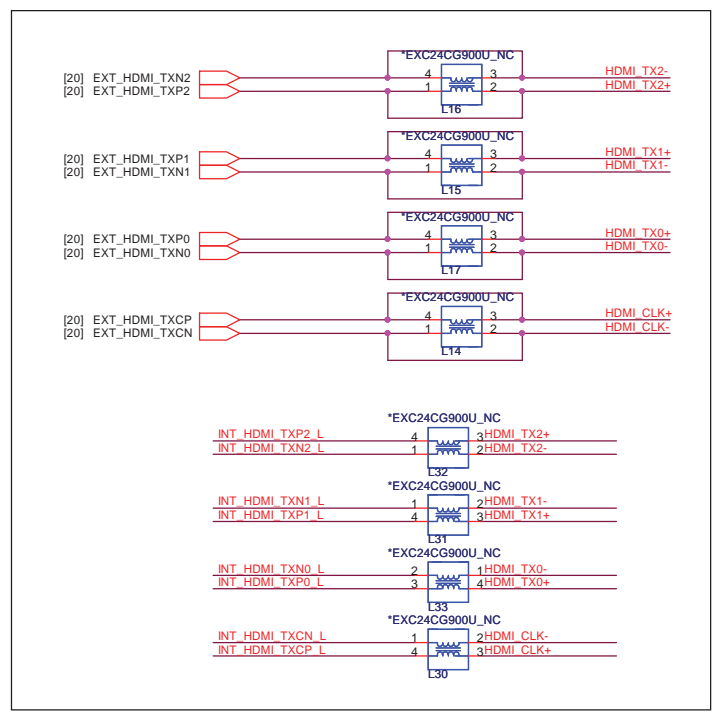
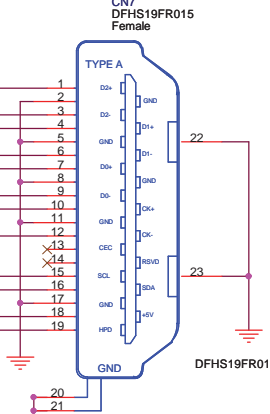
change VRAM footprint to hynix 2G(the package is bigger)

 Quanta Computer Inc. PROJECT : R03A/V03A	
Size	Document Number
N12P-GE VRAM-2(DDR3 BGA96)	
Date:	Friday, January 07, 2011
Sheet	24 of 50
Rev 2A	



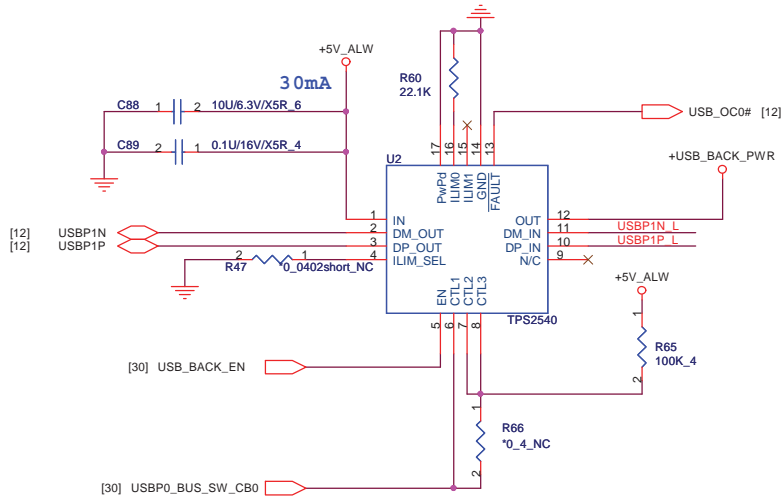


HDMI Conn.



ESATA + USB Conn + Power share

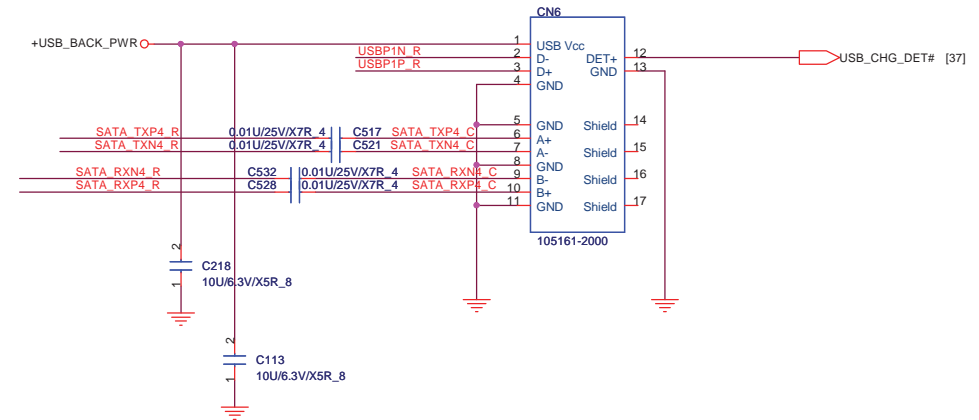
S3/S5 USB charging circuit



USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

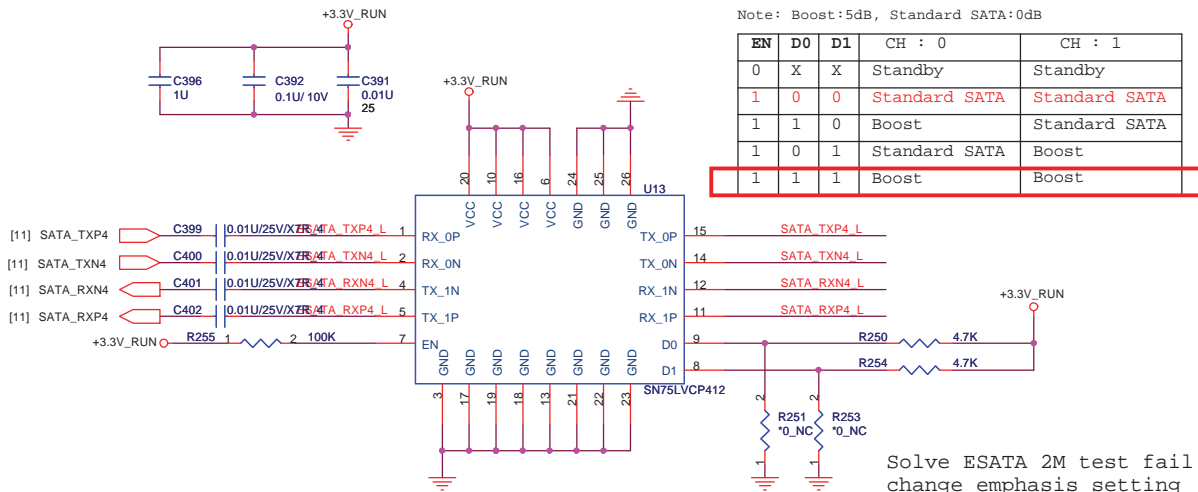
ES(PG1.0): Stuff R66, Remove R65
MP(PG1.1): Remove R66 Stuff R65

	R8224	mA
OC limitation	100k ohm	480
	22.1k ohm	2171
		Applied Now

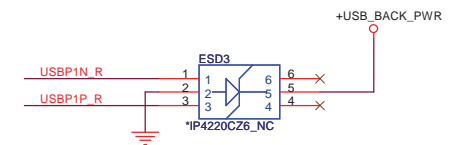
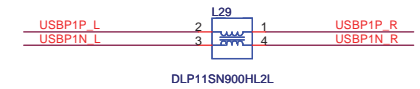
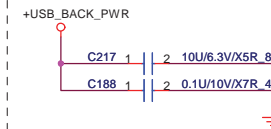


E-SATA Re-driver

Layout Note: Please put those on the same side of MB PCB



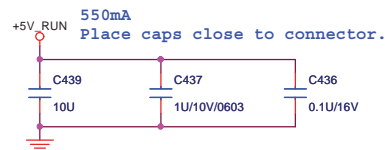
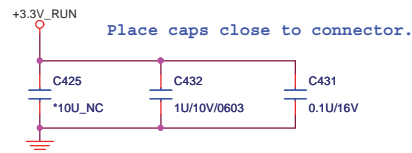
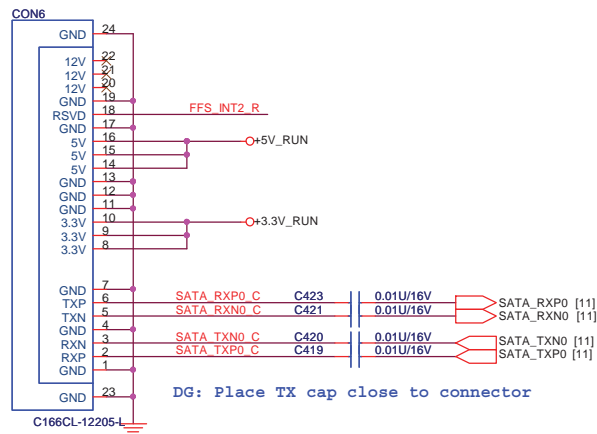
Solve ESATA 2M test fail issue,
change emphasis setting



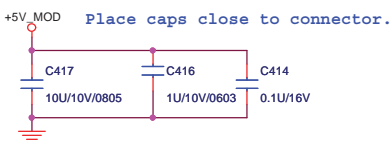
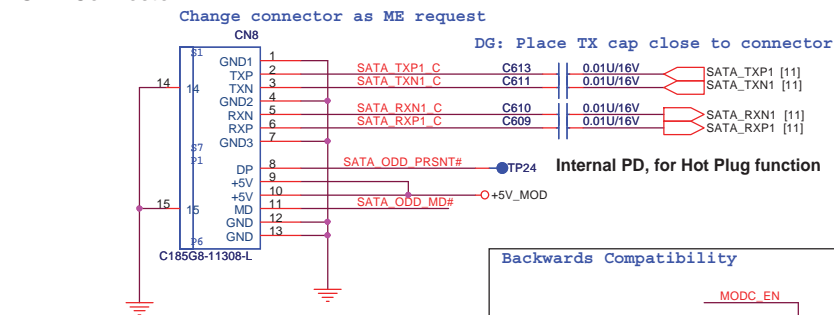
Quanta Computer Inc.
PROJECT : R03A/V03A

Size	Document Number	Rev
	PUSB / ESATA	2A
Date:	Monday, January 24, 2011	Sheet 27 of 50

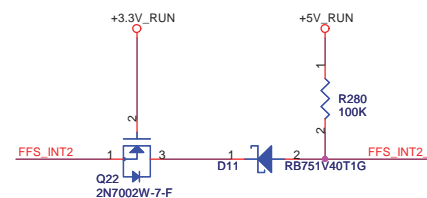
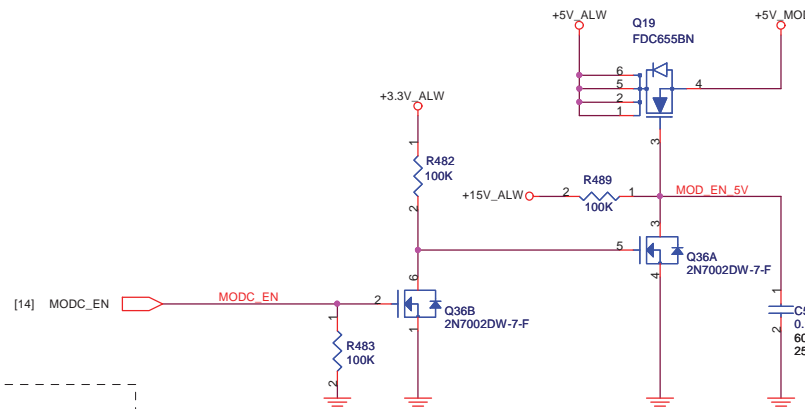
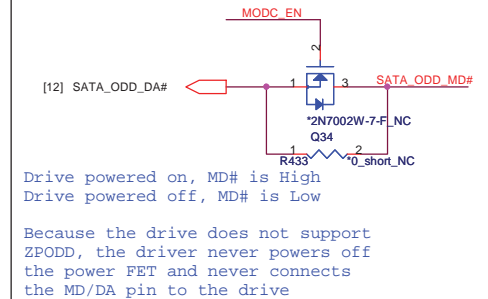
SATA Connector



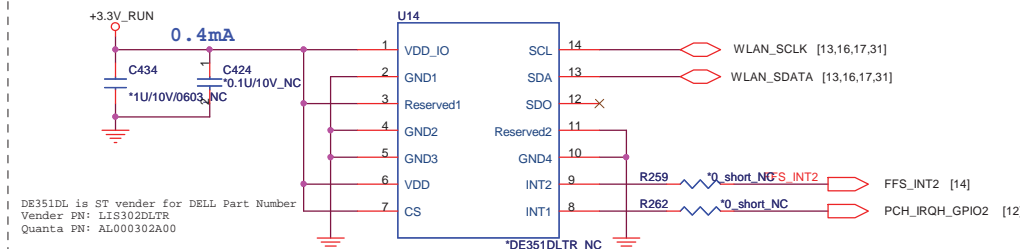
ODD Connector



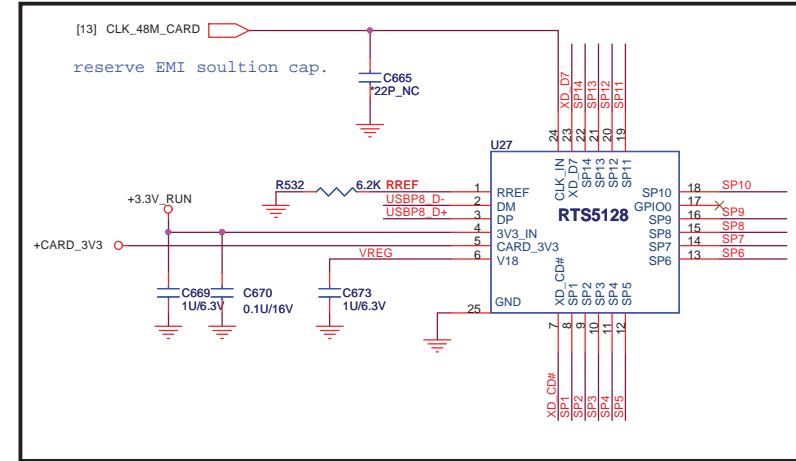
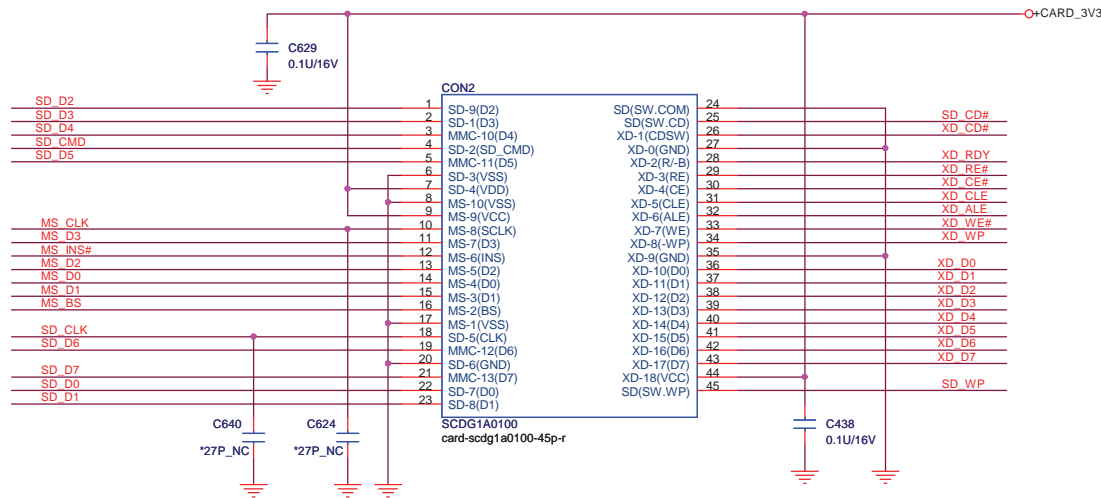
Backwards Compatibility



3-axis Fall Sensor (HDD data protector)

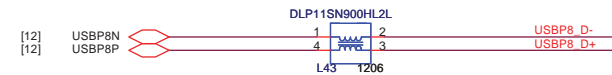


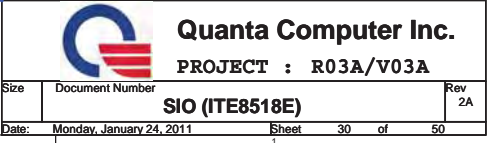
RTS5128-QFN24

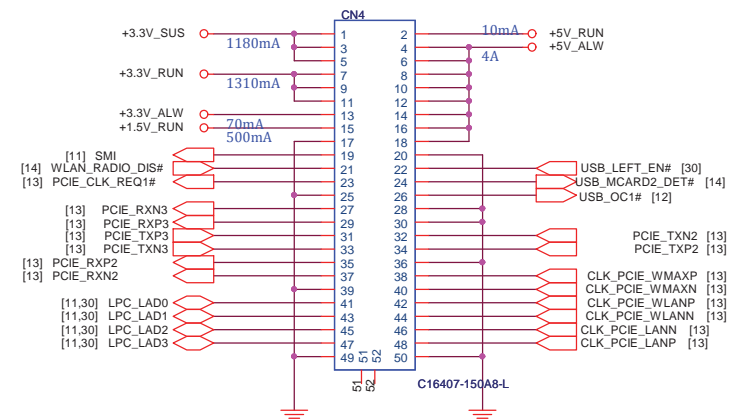
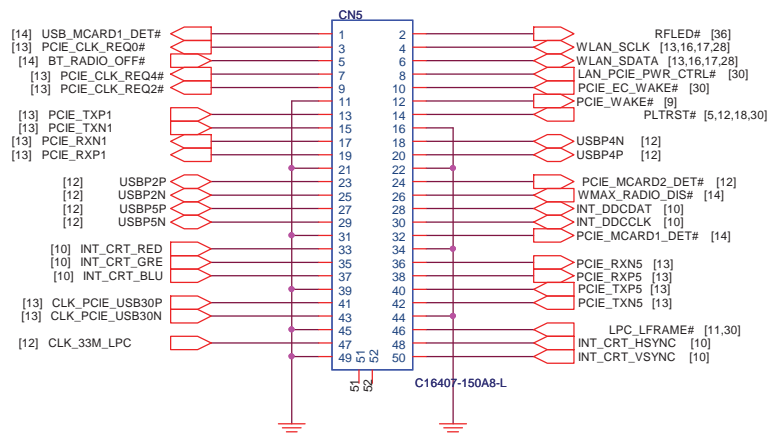


SP1	XD RDY	SD_WP	MS_CLK
SP2	XD RE#	SD_D1	MS_INS#
SP3	XD CE#	SD_D0	MS_D7
SP4	XD CLE	SD_D7	MS_D3
SP5	XD ALE	SD_CD#	MS_D6
SP6	XD WE#	SD_CD#	MS_D6
SP7	XD WP	SD_CLK	MS_D2
SP8	XD D0	SD_D5	MS_D0
SP9	XD D1	SD_CMD	MS_D4
SP10	XD D2	SD_D3	MS_D1
SP11	XD D3	SD_D2	MS_D5
SP12	XD D4	SD_D1	MS_BS
SP13	XD D5	SD_D0	
SP14	XD D6	SD_D7	

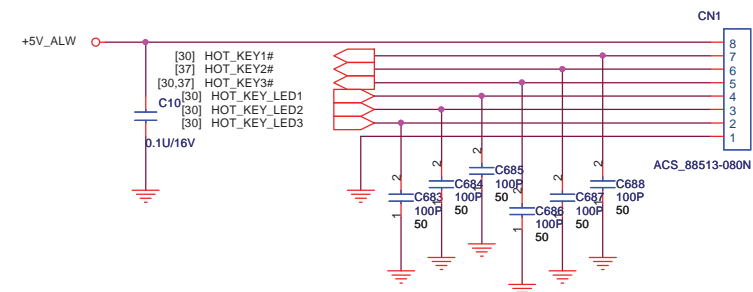
Share Pin



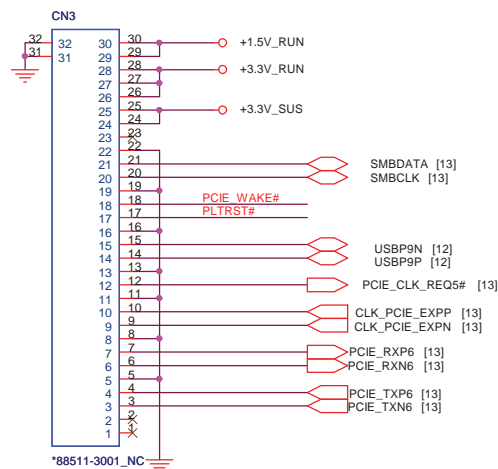




HOTKEY CON

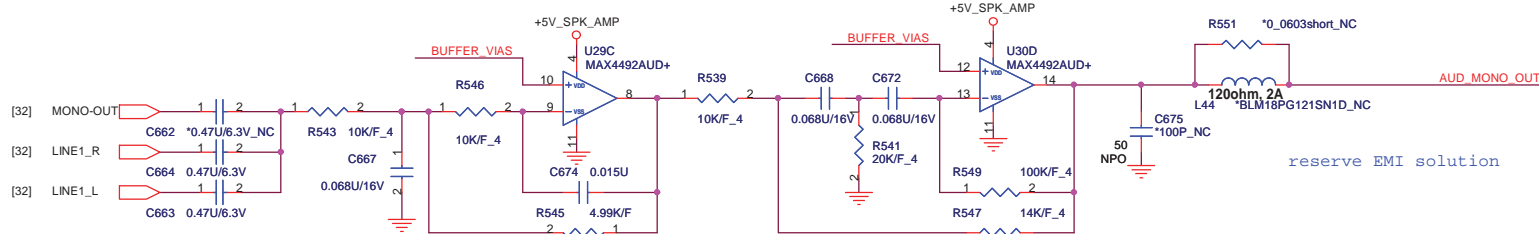
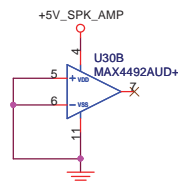
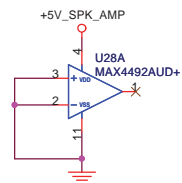
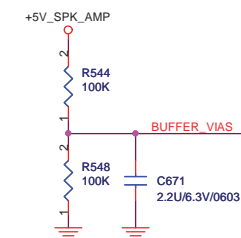


MB to Express Card Board

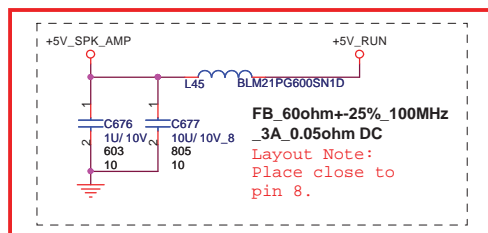


INTERNAL SUBWOOFER AMP Only for 17''

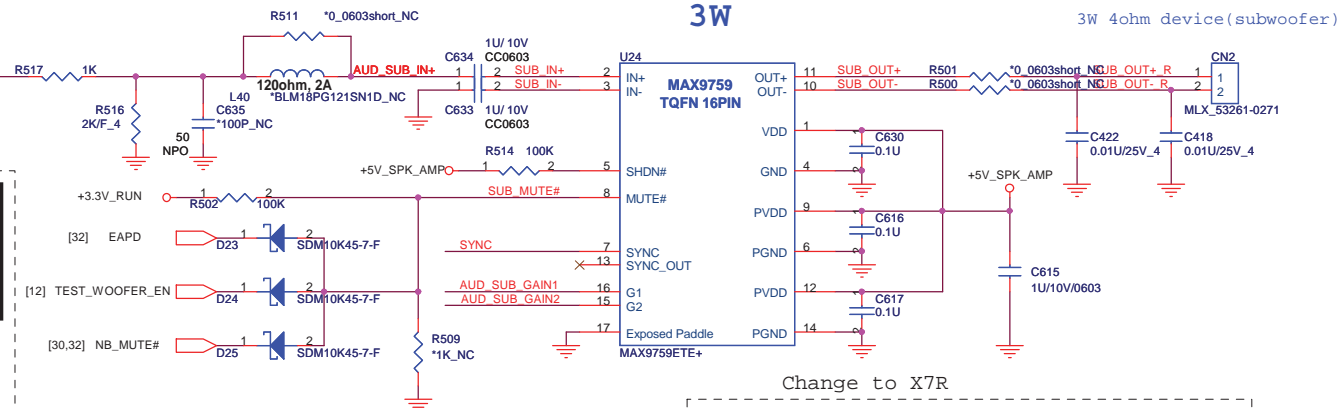
SYNC	Condition
VDD	Spread-spectrum mode with $f_S = 1200\text{kHz} \pm 70\text{kHz}$.
GND	Fixed-frequency mode with $f_S = 1100\text{kHz}$.
FLOAT	Fixed-frequency mode with $f_S = 1500\text{kHz}$.
Clocked	Fixed-frequency mode with $f_S = \text{external clock frequency}$.



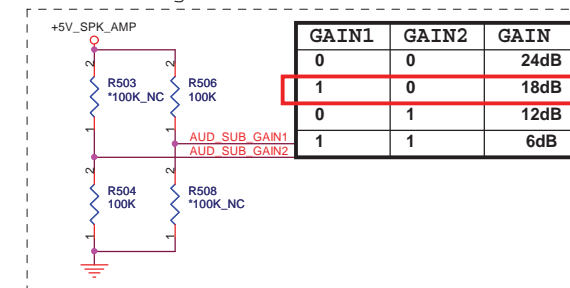
check modify to MONO-OUT PIN



place close to connector side

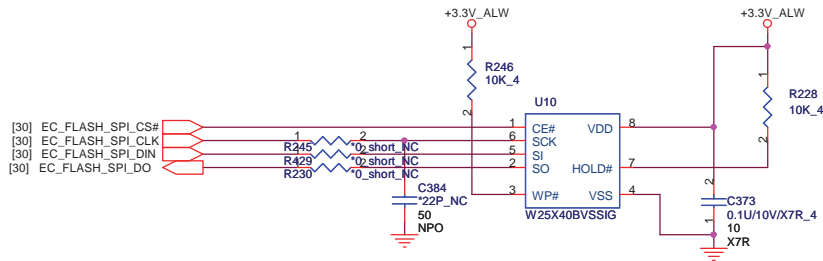


Change to X7R

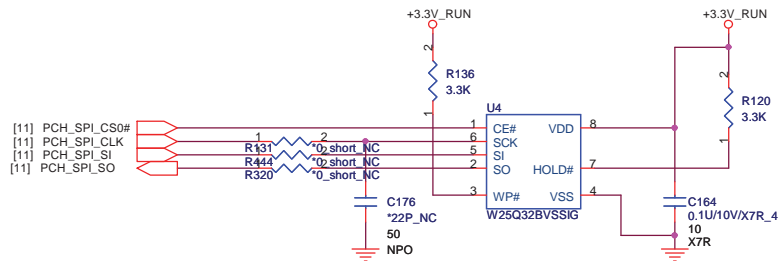


GAIN1	GAIN2	GAIN
0	0	24dB
1	0	18dB
0	1	12dB
1	1	6dB

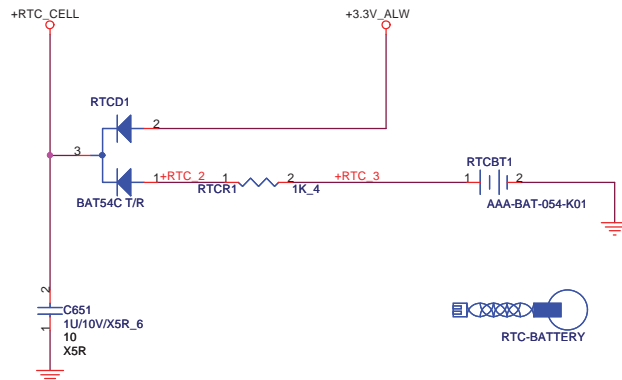
For EC 4Mbit (512K Byte)



For PCH 32Mbit (4M Byte)



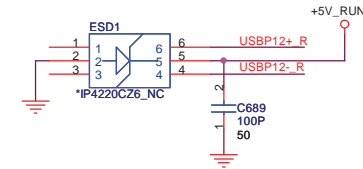
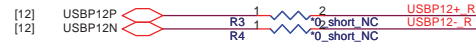
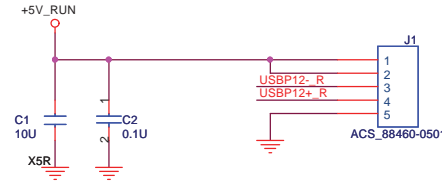
RTC



Touch Screen Module

Note:

1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect according to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
2. Maximum cable resistance on VCC, GND should be 150m ohm.
3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.



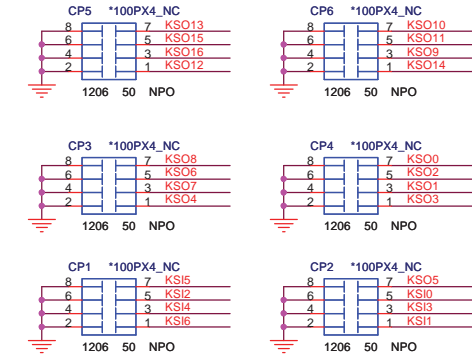
Quanta Computer Inc.

PROJECT : R03A/V03A

Size	Document Number	Rev
		2A
FLASH / RTC		
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Touch Pad

The schematic diagram illustrates the Touch Pad circuit. It features a +3.3V_RUN supply connected to a 4.7K resistor (RP1) and a +3.3V_SUS supply connected to a 100K resistor (R182). The TP_CLK signal is connected to pin 1 of L9 and L8, which are both shorted to ground. The TP_DATA signal is connected to pin 2 of L9 and L8, which are both shorted to ground. The TP_LED2_AMBER signal is connected to pin 1 of the ACS_88513-080N LED driver. The LED driver is connected to the TP_LED2 signal, which is connected to the anode of the 2N7002-7-F MOSFET (Q13). The MOSFET is connected to the TP_LED2 signal, which is connected to the anode of the 2N7002-7-F MOSFET (Q13). The MOSFET is connected to the TP_LED2 signal, which is connected to the anode of the 2N7002-7-F MOSFET (Q13).



Key board illumination

+KB_LED power trace width >10 mil

Del fuse FS1

[30] KB_BACKLITE_EN

Q35
SI2304
DDS-T1-GE3

LED_PWM

1
2
3
4

J5
1
2
3
4

91504-0401

+5V_RUN

R140 100K

R143 200K

[12] KB_LED_DET

C231
0.1U

16

Biometric Finger Printer

ESD by EMC request

Pin 6 => GND(for detect pin)

Components and Connections:

- Power Source:** +3.3V_RUN
- Capacitor:** C280, *12P/50V_NC
- Connector:** J6 (pins 1-6)
- ESD Protection:** ESD2, *IP4220CZ6_NC
- USB Lines:** USBP10P, USBP10N
- Grounding:** Pins 1, 2, 3 of ESD2 and Pin 1 of J6 are connected to ground.

KEYBOARD CONNECTOR

KEYBOARD CONNECTOR

51510-03041-001

30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

GND2

GND1

CON1

[36] CAP_LED

[30] KSO[0..16]

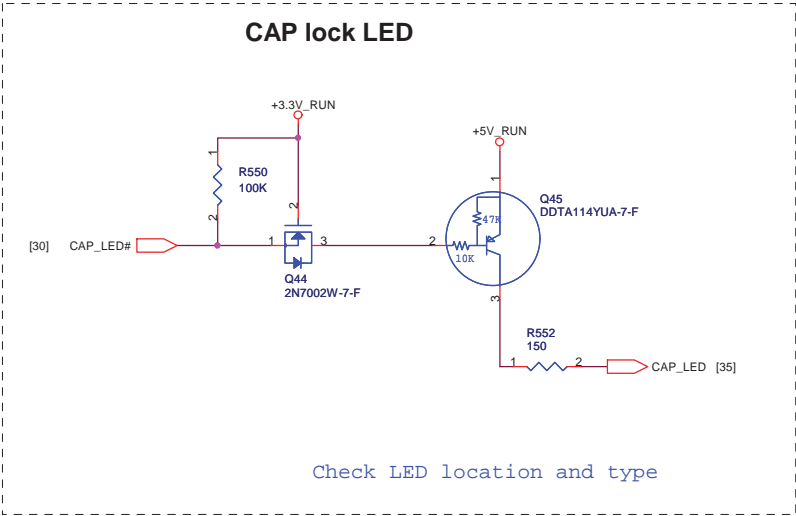
[30] KSI[0..7]

[30] KB_DET#

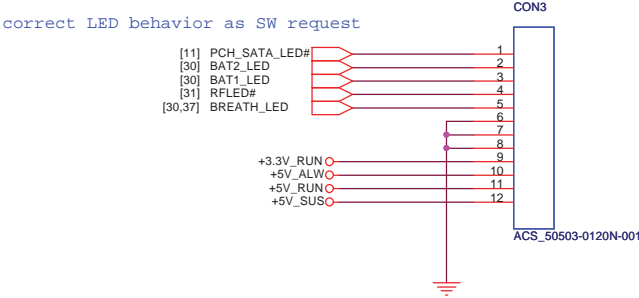
+3.3V_ALW

R303

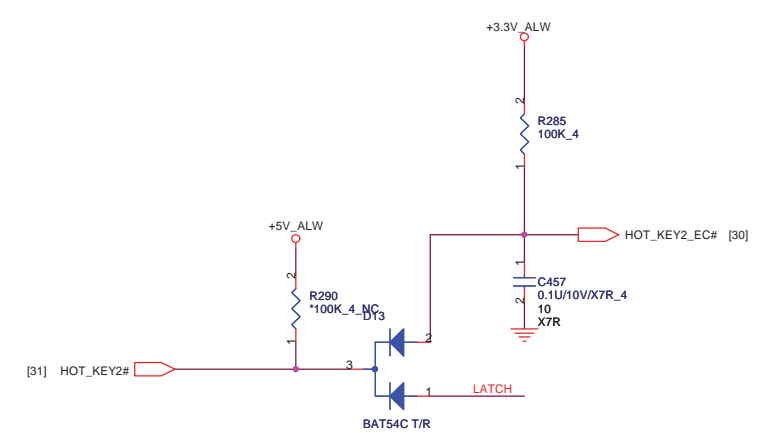
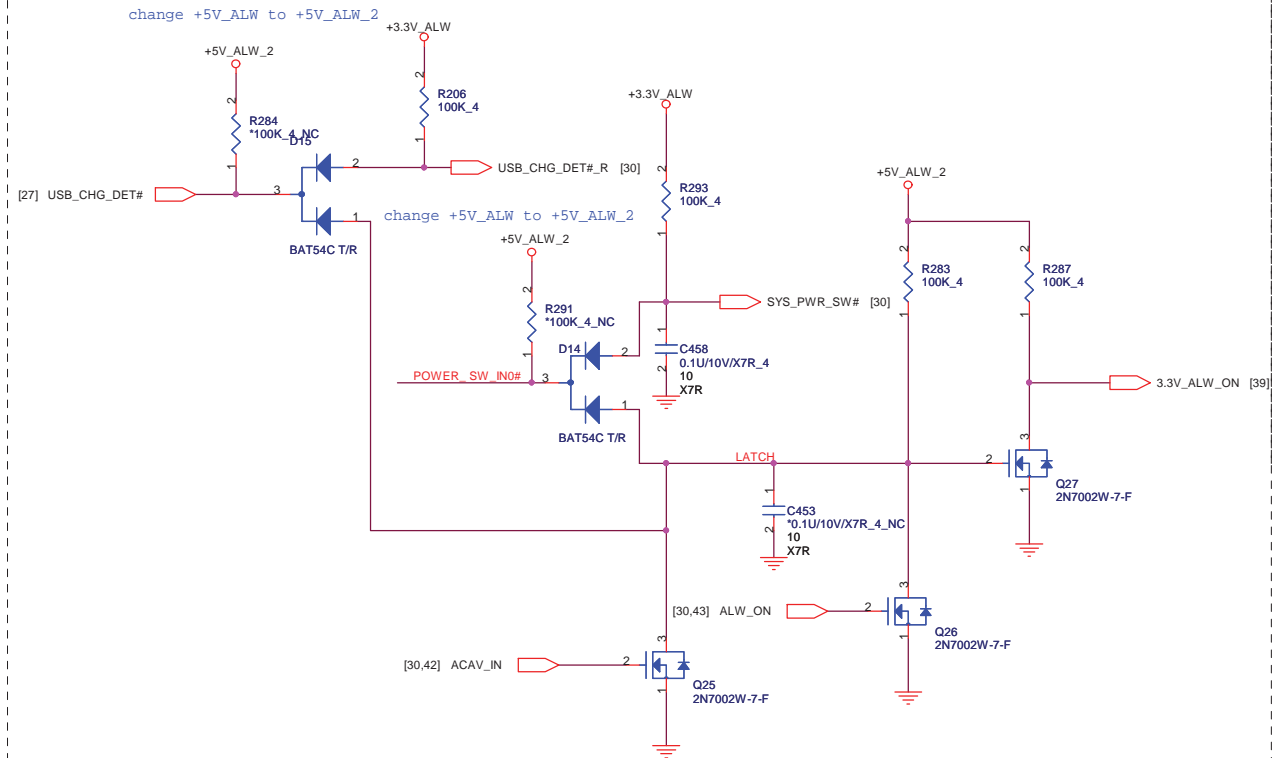
10K



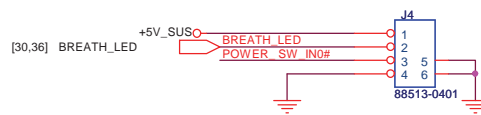
MB to LED Board conn



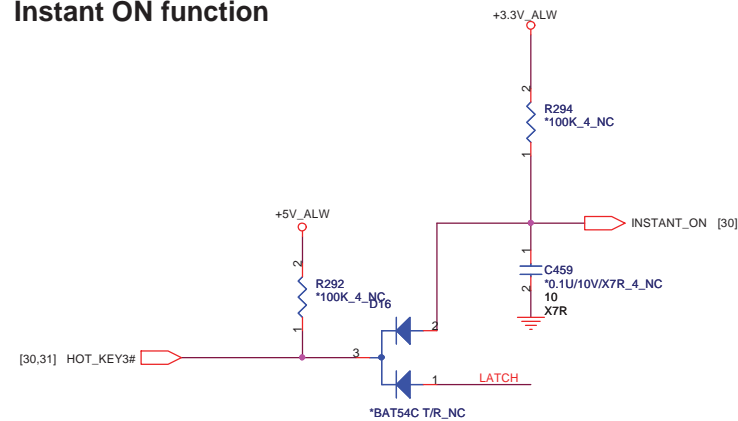
3VALW ON POWER LOGIC



PWR button board form UM7



Instant ON function

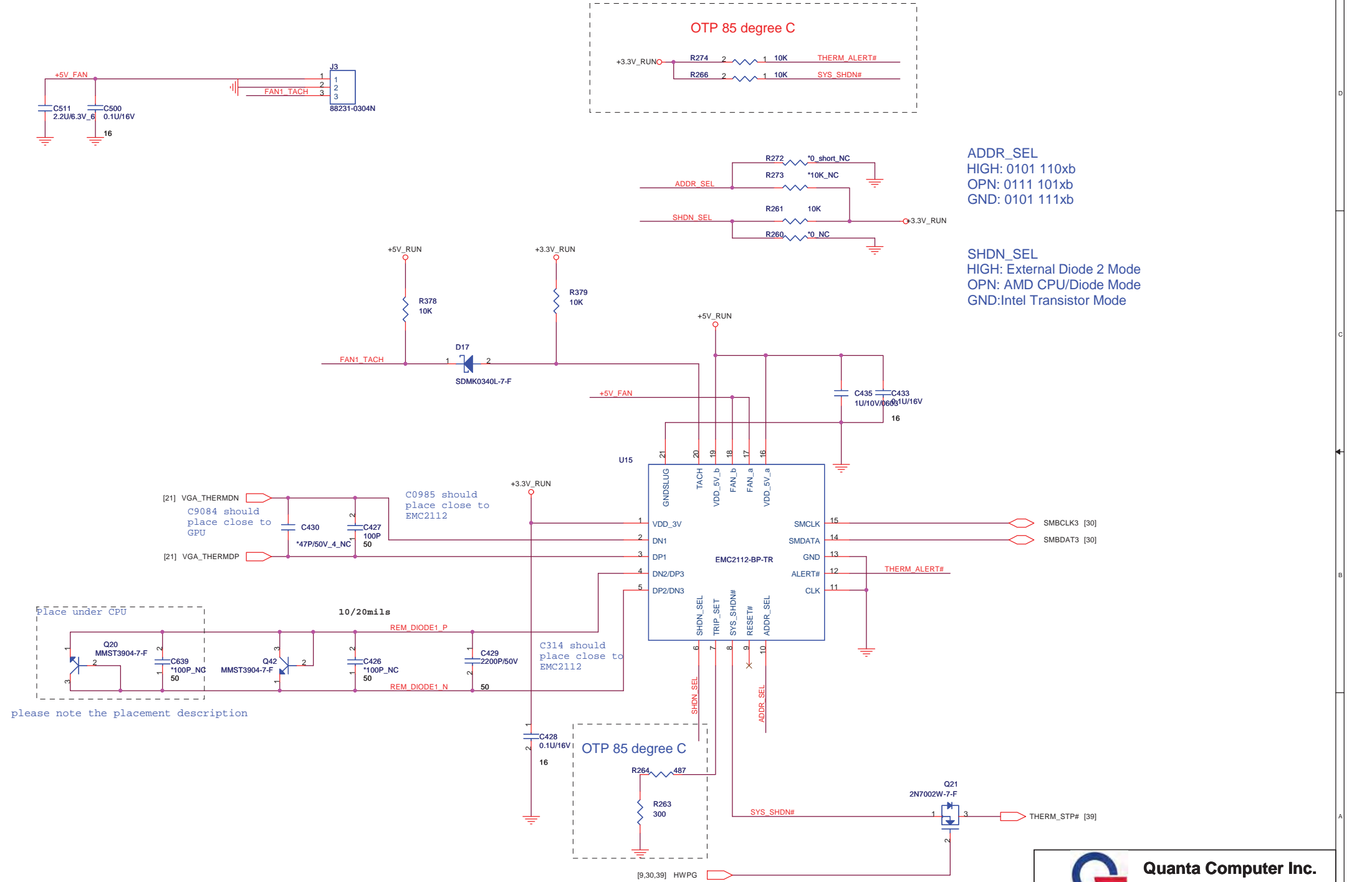


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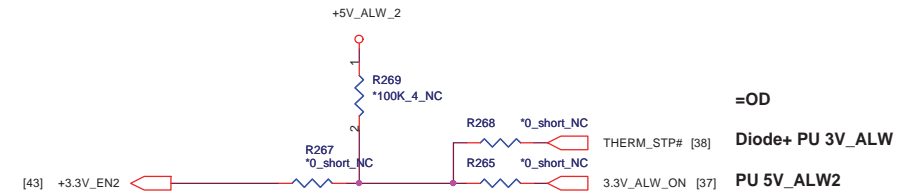
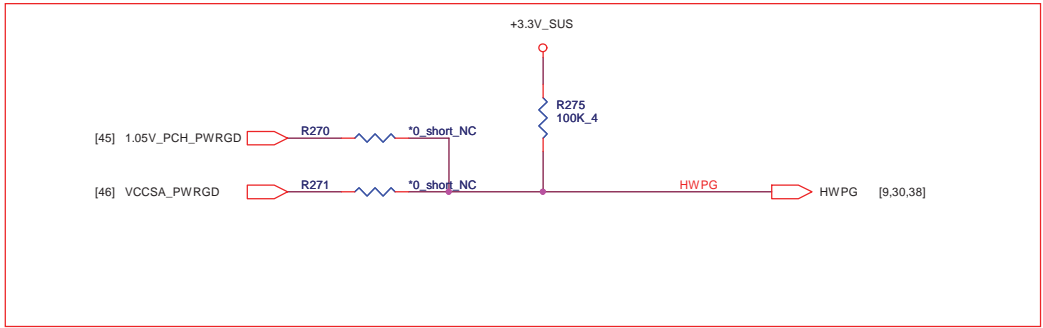
PROJECT : R03A/V03A

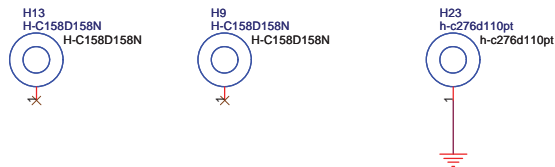
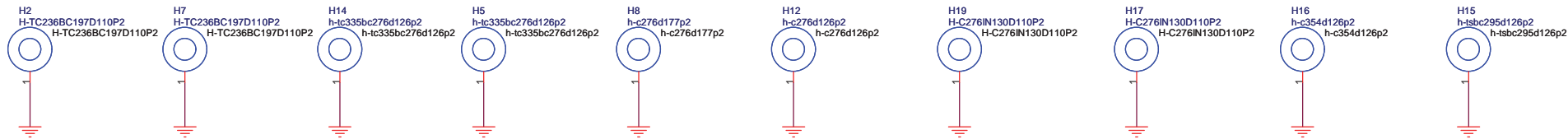
Size	Document Number	Rev
	PWR SW/LED	2A
Date:	Monday, January 24, 2011	Sheet 37 of 50

FAN CONTROL



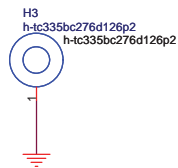
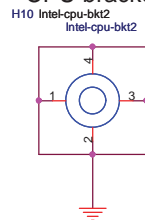
please note the placement description





add a new hole for layout request

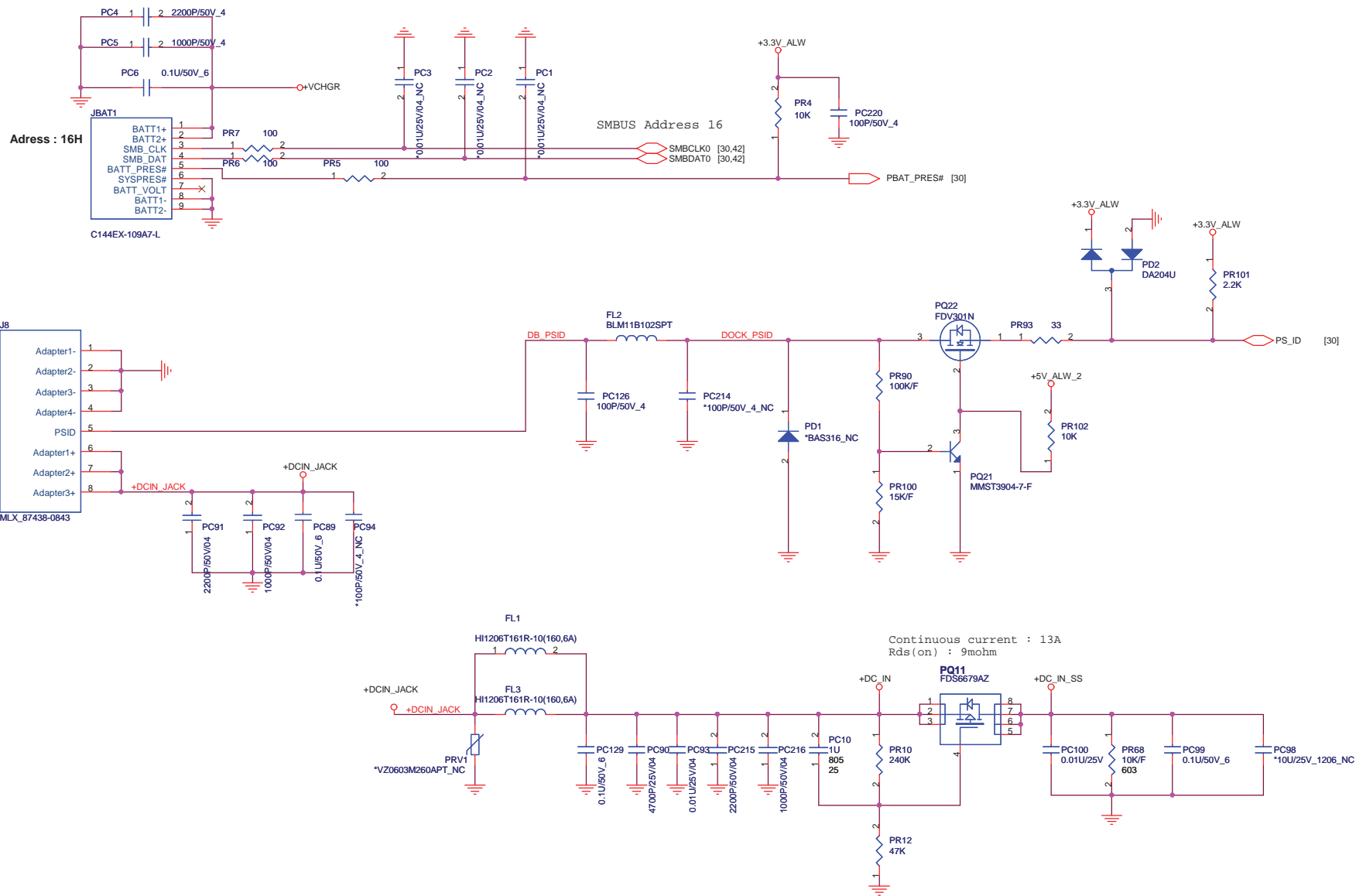
CPU bracket

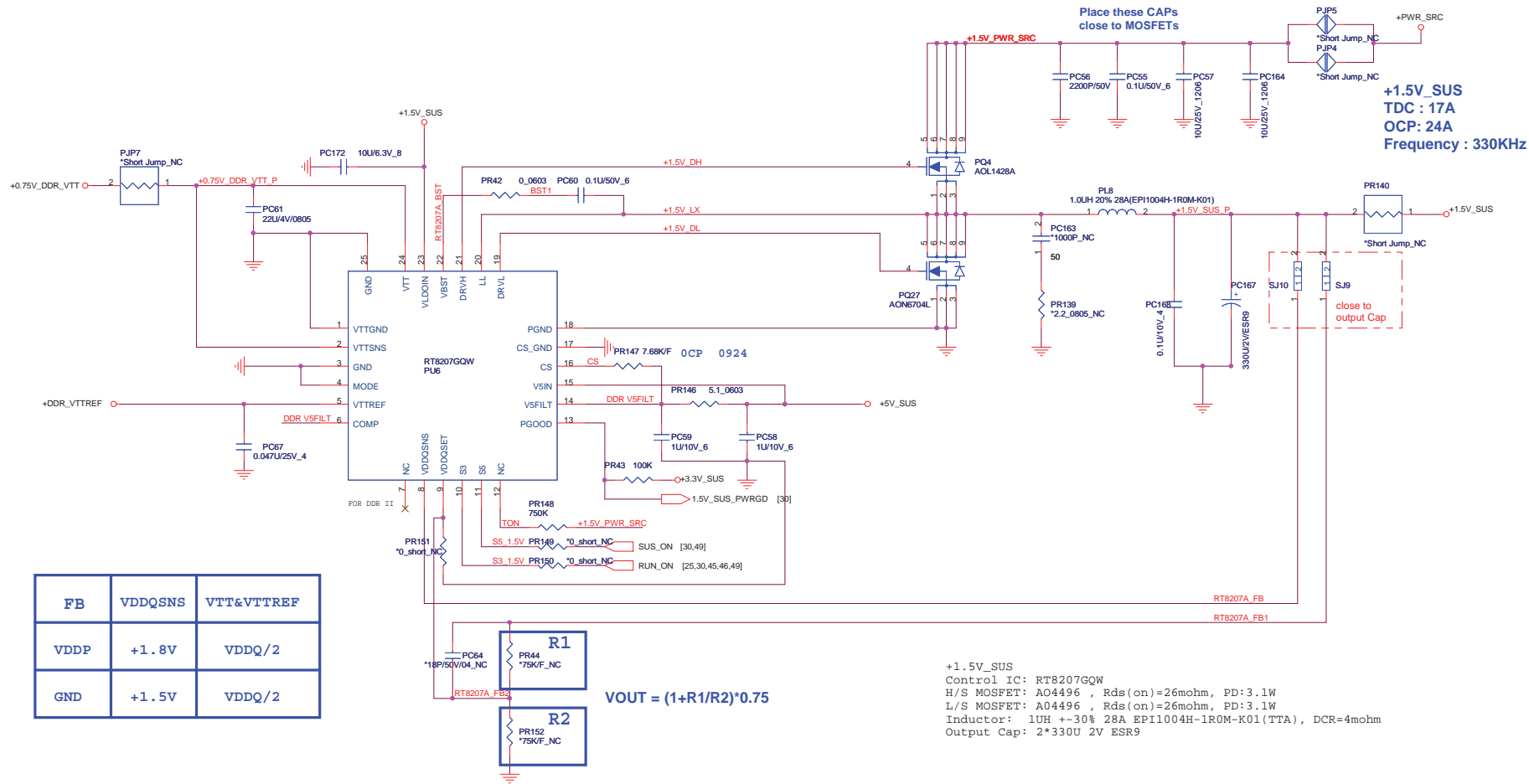


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FB	VDDQSNS	VTT&VTTREF
VDDP	+1.8V	VDDQ/2
GND	+1.5V	VDDQ/2

VDDQ and VTT discharge control

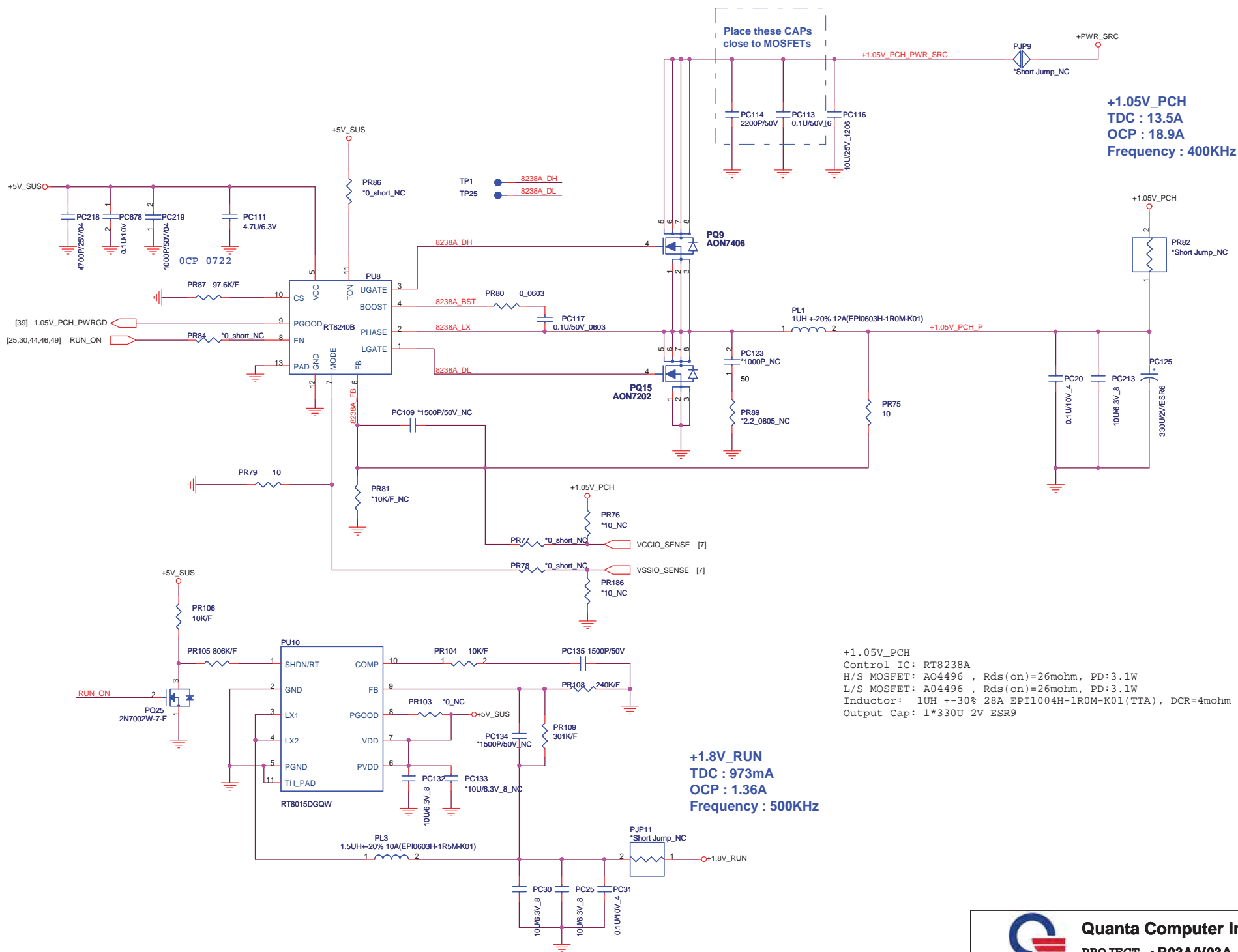
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

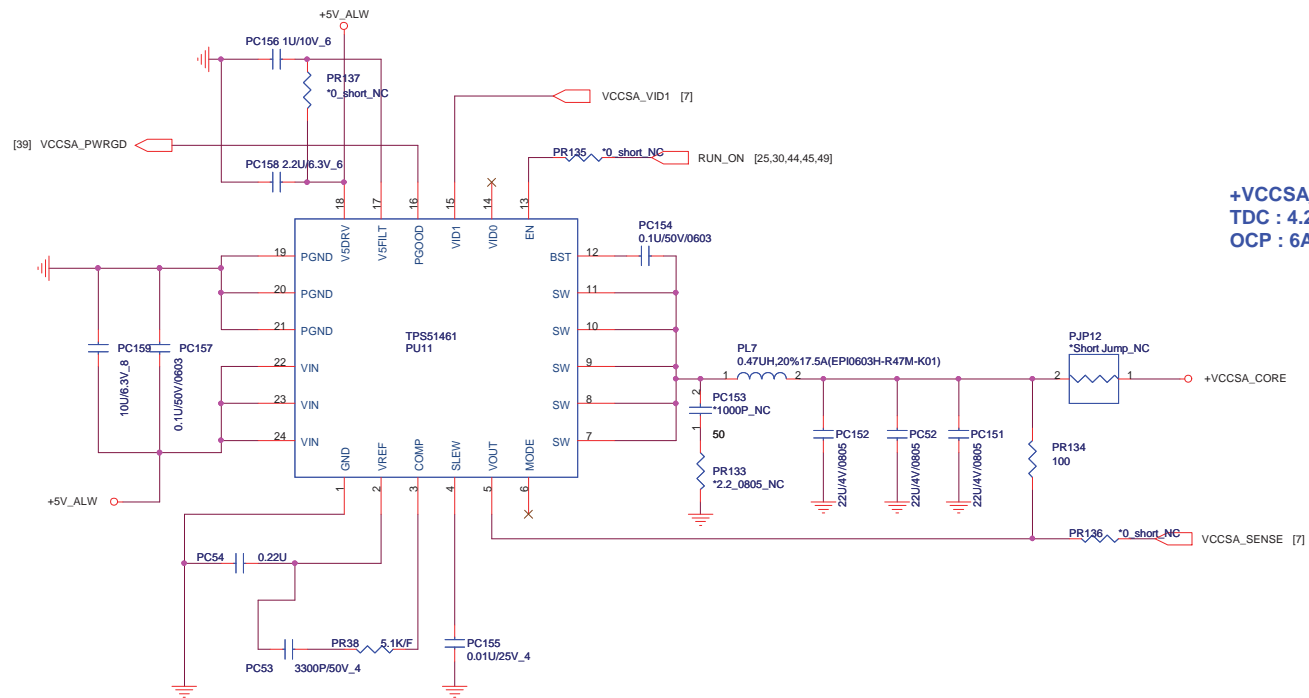
VDDQ output voltage selection

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (H1-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)





+VCCSA	VCCSA_VID1
0.8V	High
0.9V	Low



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VCCSA (TPS51461)

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+VCC_DGFX_CORE	DGPU_VID2(G0)	DGPU_VID1(G1)
0.85V	0	0
0.875V(NA)	0	1
0.95 V	1	0
0.975V	1	1

[21] DGPU_VID1
[21] DGPU_VID2

$$V_o = 0.75 (R1 + R2) / R2$$

+VCC_GFX_CORE
Control IC: RT8208A
H/S MOSFET: FDMS7692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS0308S(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.36UH 20% 28A(EPI1004H-1R0M-K01)(TTA), DCR=2.8mohm
Output Cap: 2*330U, 2.5V(20%, 105C, 3528), ESR=9mohm

+VCC_GFX_CORE
TDC : 30.5A
Peak: 43.6A
OCP : 48A
Freq : 300KHz

+1.05V_GFX
TDC: 2.7A

+1.5V_GFX
TDC : 4.22A

+3.3V_GFX
TDC: 0.96A

