

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EC 8095 – VLSI DESIGN

UNIT – I INTRODUCTION TO MOS TRANSISTOR

COURSE HANDOUTS

PART-A

1. What is meant by channel length modulation

the p–n junction between the drain and body forms a depletion region with a width of L_d that increases with V_{db} (Drain to body voltage). The depletion region effectively shortens the channel length to

$$L_{eff} = L - L_d$$

2. Define a propagation delay for CMOS inverter

The propagation delay of the CMOS inverter is determined by the time it takes to charge and discharge the capacitances present in the logic circuit.

Propagation Delay Time, t_{pd} :

Maximum time from the input crossing 50% to the output crossing 50%

3. Define any two layout design rules

Scalable Design Rules (e.g. SCMOS, λ -based design rules)

Absolute Design Rules (e.g. μ -based design rules)

4. What is latch up? How to prevent a latch up.

Latch Up:

Latch is the generation of a low-impedance path in CMOS chips between the power supply and the ground rails due to interaction of parasitic pnp and npn bipolar transistors. This causes excessive current flows to the devices.

Prevention:

- i. Increase well and substrate doping concentrations to reduce R_{well} and R_{sub} .
For example, using retrograde doped wells.
- ii. Provide alternative (or better) collectors of the minority carriers. For example, the use of guard rings around devices.

5. Define body effect

The threshold voltage V_t is constant or varied, with respect to voltage difference between source and the body is called body effect.

$$V_t = V_{t0} + \gamma \left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s} \right)$$

6. Define lambda layout rule

Lambda rules specify the layout with minimum feature sizes and minimum allowable feature separations in terms of parameter λ and allow linear proportional scaling of all geometrical constraint.

7. What are stick diagram

Stick diagram are the key element of designing a circuit used to convey layer information through the use of a color code.

8. What is CMOS technology

Complementary Metal Oxide Semiconductor (CMOS) in which both n-channel MOS and p-channel MOS are fabricated in the same IC

9. Write a parasitic delay and logical effort for basic gates

Logical Effort:

Gate Type	Number of Inputs				
	1	2	3	4	n
inverter	1				
NAND		4/3	5/3	6/3	$(n+2)/3$
NOR		5/3	7/3	9/3	$(2n+1)/3$
tristate, multiplexer	2	2	2	2	2
XOR, XNOR		4, 4	6, 12, 6	8, 16, 16, 8	

Parasitic Delay :

Gate Type	Number of Inputs				
	1	2	3	4	n
inverter	1				
NAND		2	3	4	n
NOR		2	3	4	n
tristate, multiplexer	2	4	6	8	$2n$

10. Define a threshold voltage for a MOSFET

The threshold voltage of a MOSFET is usually defined as the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor.

11. What are the objective (need) of layout rules?

- To build reliably functional circuits in as small an area as possible.
- To provide a necessary communication link circuit designer and process engineer during manufacturing.
- To obtain a circuit with optimum yield in smallest possible area.

Part-B

1. Explain in detail about the ideal I-V characteristics and non-ideal I-V characteristics of nMOS and pMOS devices.

Ideal I-V characteristics

- Cut-off or Sub-threshold mode → When $V_{gs} < V_t$, $I_{ds} = 0$, then transistor is turned off. No conduction takes place between drain and source.
- Linear or non saturation mode → When $V_{gs} > V_t$ and $V_{ds} < (V_{gs} - V_t)$ → Transistor turned on. Channel or conduction path is created which allows current flow from drain-source.
- Saturation mode → When $V_{gs} > V_t$ and $V_{ds} > (V_{gs} - V_t)$ → Switch is turned on. Channel is created which allows current flow between drain and source. If drain voltage is higher than the gate voltage, portion of channel is turned off. Hence the drain current is independent with drain voltage and current is controlled by V_{gs}

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} & \text{linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} & \text{saturation} \end{cases}$$

Non-ideal I-V characteristics

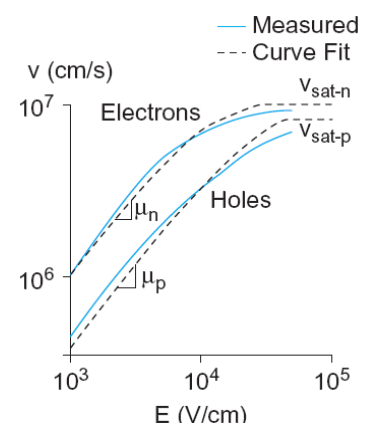
1) Mobility Degradation

Mobility of charge carriers varies by the following factor

- High Temperature
- Type of charge carriers
- doping

2) Velocity Saturation

- At high lateral field strength (E), carrier velocity Increased.
- Carriers scatter off atoms in silicon lattice
- Velocity reaches v_{sat}
- Electrons: 10^7 cm/s
- Holes: 8×10^6 cm/s



$$v = \begin{cases} \frac{\mu_{\text{eff}} E}{1 + \frac{E}{E_c}} & E < E_c \\ v_{\text{sat}} & E \geq E_c \end{cases}$$

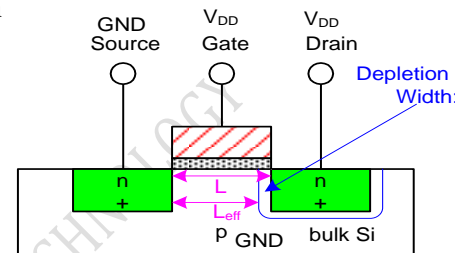
3) Channel Length Modulation

It occurs at Reverse-biased condition p-n junctions form a depletion region.

Hence region between n and p with no carriers. Width of depletion

L_d region grows with reverse bias

$$I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2 (1 + \lambda V_{ds})$$



4) Threshold Voltage (V_t)

It is defined as the voltage applied between the gate and source, which the device starts conduction or turns on.

Parameters define V_t

- 1) Gate conductor material
- 2) Gate insulation material
- 3) Insulator thickness
- 4) Impurities
- 5) Voltage between source and substrate

$$V_t = \underbrace{2\phi_b}_{\text{bulk potential}} + \underbrace{\frac{\sqrt{2\epsilon_{\text{Si}} q N_A} 2\phi_b}{C_{\text{ox}}}}_{\text{Ideal threshold voltage}} + \underbrace{V_{fb}}_{\text{flat band voltage}}$$

$$\phi_b = \frac{KT}{q} \ln \left(\frac{N_A}{N_i} \right) = \text{Bulk potential}$$

5) Body Effect

- Body is a fourth transistor terminal. The change in threshold voltage of the MOS transistor because of the non zero bias to the body is called Body effect.
- It occurs when body or substrate of transistor is not biased at the same level of source.
- Because of vol difference between source and substrate V_t is not constant

$$V_t = V_{t0} + \gamma \left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s} \right)$$

6) Leakage Sources

- **Sub-threshold conduction**
- In ideal transistor if the device turns off abruptly when $V_{gs} < V_t$
- But in practically because of inversion layer some current flows from source to drain.
- This conduction is called leakage and the resulting current is leakage current.
- $I_{ds} \rightarrow$ current at the threshold and its dependant on process and device geometry
- **Gate leakage**

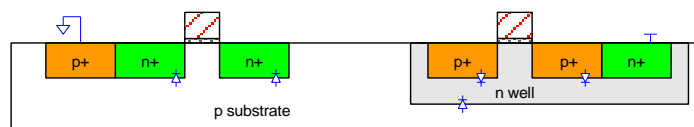
Carriers tunnel thorough very thin gate oxides resulting leakage current flowing into the gate.

$$I_{\text{gate}} = WA \left(\frac{V_{DD}}{t_{\text{ox}}} \right)^2 e^{-B \frac{t_{\text{ox}}}{V_{DD}}}$$

When gate oxide is thin ,current flow from gate-source or drain.

- **Junction leakage**

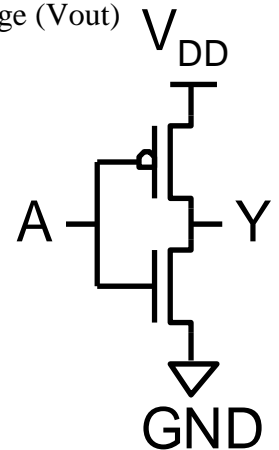
Reverse-biased PN junction diode current



2). Explain DC transfer characteristics of a CMOS inverter with necessary conditions for the different regions of operation.

DC transfer characteristics of the inverter are a function of the output voltage (V_{out}) with respect to the input voltage (V_{in}).

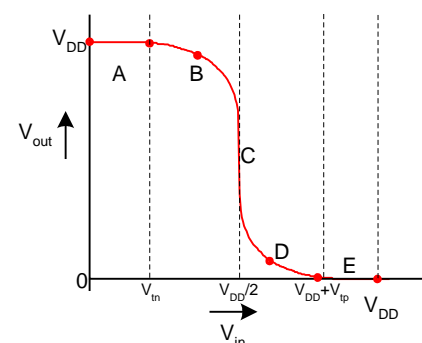
- When $V_{in} = 0 \rightarrow V_{out} = V_{DD}$
- When $V_{in} = V_{DD} \rightarrow V_{out} = 0$



- **Region A occurs when $0 = V_{in} = V_{tn(n-type)}$.**
 - The n-device is in cut-off ($I_{dsn} = 0$).
 - p-device is in linear region,
 - $I_{dsn} = 0$
 - For p-MOS $V_{out} = V_{DD}$.
- **Region B occurs when the condition $V_{tn} = V_{in} = V_{DD}/2$ is met.**
 - Here p-device is in its non-saturated region $V_{ds} = 0$.
 - n-device is in saturation
 - Saturation current I_{dsn} is obtained by setting $V_{gs} = V_{in}$ resulting in the equation:

$$I_{dsn} = \frac{\beta_n}{2} [V_{in} - V_{tn}]^2$$

- **Region C has that both n- and p-devices are in saturation.**
 - Saturation currents for the two devices are:



$$I_{dsp} = -\frac{\beta_p}{2} (V_{in} - V_{DD} - V_{tp})^2; V_{in} < V_{tp} + V_{DD}$$

AND

$$I_{dsn} = \frac{\beta_n}{2} (V_{in} - V_{tn})^2; V_{in} > V_{tn}$$

- **Region D is defined by the inequality**

- p-device is in saturation while n-device is in its non-saturation region.

$$I_{dsp} = -\frac{\beta_p}{2} (V_{in} - V_{DD} - V_{tp})^2; V_{in} < V_{tp} + V_{DD}$$

AND

$$I_{dsn} = \beta_n \left[(V_{in} - V_{tn}) V_{out} - \left(\frac{V_{out}}{2} \right)^2 \right]; V_{in} > V_{tn}$$

- **In Region E the input condition satisfies**

$$V_{in} \geq V_{DD} - V_{tp}$$

- The p-type device is in cut-off: $I_{dsp}=0$
- The n-type device is in linear mode
- $V_{gsp} = V_{in} - V_{DD}$ and this is a more positive value compared to V_{tp} .
- $V_{out} = 0$

3) Discuss the principles of constant field and lateral scaling.

- **Constant field scaling**

- All device dimensions like channel length, width, supply voltage and threshold voltage reduced by a factor $1/s$.
- Voltage V_{DD} is kept constant.
- Substrate doping increased by S .

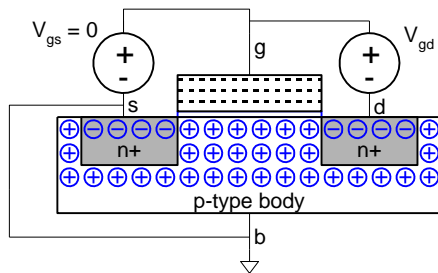
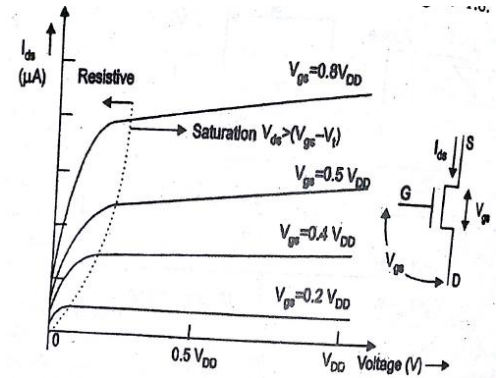
- **lateral scaling**

- Only the gate length is scaled
- Channel length reduced by the factor $1/S$.
- If the feature size shrinks from $6\mu m$ to $1\mu m$ by maintaining a $5V$ constant supply voltage \rightarrow constant voltage scaling.
- This will improve the delay performance and reduce the cost

4). Describe the equation for source to drain current in the three regions of operation of a MOS transistor and draw the VI characteristics

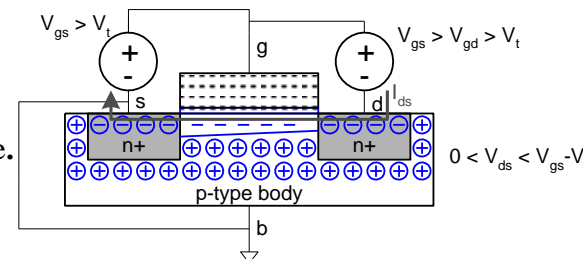
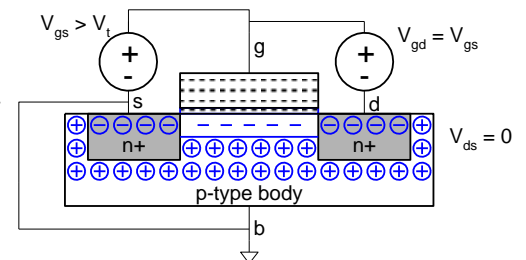
1. Cut-off region

- When $V_{gs} < V_t$, the body has free holes but no free electrons.
- The junction between the body and the source or drain is reverse biased.
- Hence no current will flow
- $I_{ds} \approx 0$



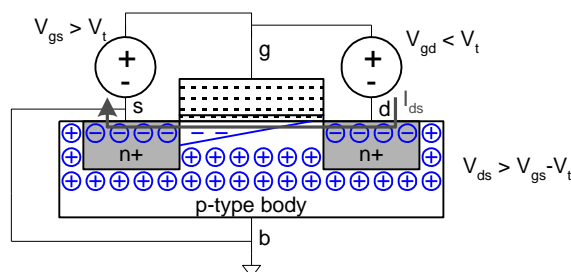
2. Non-saturated region

- Case (i) When $V_{gs} > V_t$, there is a
- conductive path is created between source and drain.
- The number of carriers and conductivity
- increases with the gate voltage.
- The potential difference between drain and source
- is $V_{ds} = V_{gs} - V_{gd}$
- Case (ii) Small positive voltage
- ($0 < V_{ds} < V_{gs} - V_t$) is applied I_{ds} flow drain to source.



3. Saturated region

- When $V_{gs} > V_t$ channel is no longer inverted near the drain and becomes pinched off.
- Electrons are drifted under the positive drain voltage.
- As electrons reach the end of the channel, they are injected into the depletion region and accelerated towards the drain.



KONGUNADU COLLEGE OF ENGINEERING AND TECHNOLOGY (AUTONOMOUS)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EC 8095 – VLSI DESIGN

UNIT – II COMBINATIONAL MOS LOGIC CIRCUITS

COURSE HANDOUTS

PART-A

1. Define Elmore constant

Elmore delay is a simple approximation to the delay through an RC network in an electronic system.

The Elmore delay model estimates the delay from a source switching to one of the leaf nodes changing as the sum over each node i of the capacitance C_i on the node, multiplied by the effective resistance R_{is} on the shared path from the source to the node and the leaf. Application of Elmore delay is best illustrated through examples.

$$t_{pd} = \sum_i R_{is} C_i$$

2. State the advantages of Transmission gate.

A transmission gate is similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. It is a CMOS-based switch, in which PMOS passes a strong 1 but poor 0, and NMOS passes strong 0 but poor 1. Both PMOS and NMOS work simultaneously.

Applications:

Electronic Switch
Analog multiplexers
Logic circuits
Negative voltages

3. What are the factors that causes a power dissipation in CMOS circuits?

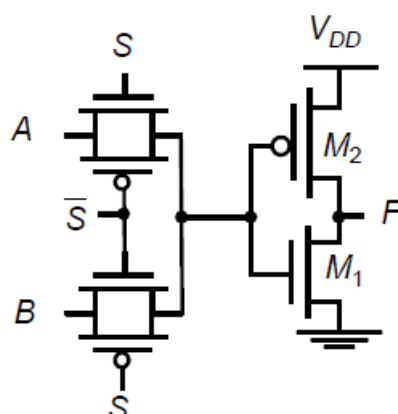
Static Dissipation:

- i. Sub threshold condition through OFF transistors
- ii. Tunneling current through gate oxide
- iii. Leakage through the reverse bias diode
- iv. Contention current in ratioed circuits

Dynamic Dissipation:

- i. Charging and discharging of load capacitance
- ii. Short circuit current while both PMOS and NMOS network are partially ON.

4. Implement a 2 : 1 mux using Pass transistor



$$\bar{F} = (A \cdot S + B \cdot \bar{S})$$

5. Define logical effort

The ratio of the input capacitance of the gate to the input capacitance of the inverter is called logical effort

6. How to avoid monotonicity problem in dynamic CMOS.

The monotonicity problem can be solved by placing a static CMOS inverter between dynamic gates. This is used to convert the monotonically falling output into a monotonically rising signal

7. Distinguish between static and dynamic CMOS design.

Static CMOS	Dynamic CMOS
It required a 2N number of gates to implement a circuit Where N – Number of input	It required only N+1 gates
No Monotonicity problem	Monotonicity problem arises
No need of Clock pulse	Required a careful clocking

8. Define CVSL & critical path

CVSL:

Cascade voltage switch logic is a differential type of logic circuit whereby both true and complement inputs are required.

Critical Path:

It is a longest path in the circuit which decides the most critical function, and requires the attention to timing details.

9. Why keepers are used in domino logic

Keepers must be wide enough to compensate for any leakage current drawn when the output is floating and pull-down network is OFF.

10. Define level restoration

The level restorer is a feedback transistor of an inverter which is help to eliminate the static power dissipation in the inverter and no static current path can exist through the level restorer.

11. What is branching effort

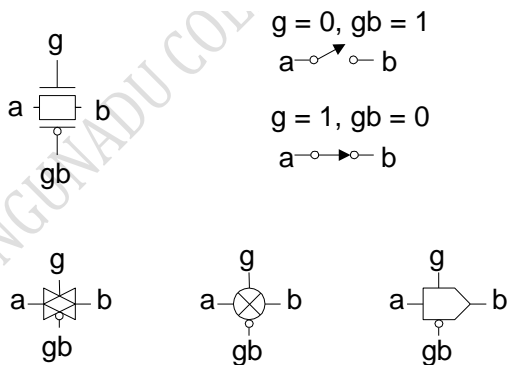
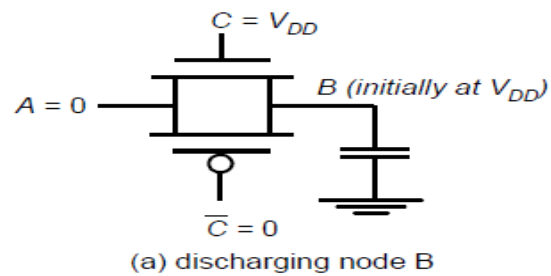
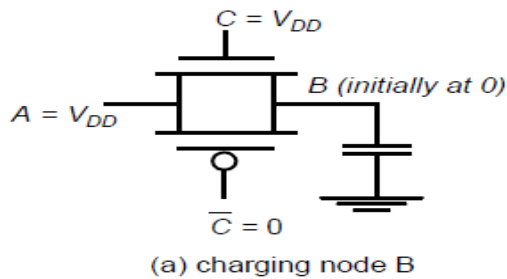
The ratio of total capacitance seen by a stage to a capacitance on the path

$$b = C_{\text{on path}} + C_{\text{off path}} / C_{\text{on path}}$$

PART-B

1) Discuss in detail the characteristics of CMOS transmission gate

- Pass transistors produce degraded outputs but Transmission gates pass both 0 and 1 well as a strong output.
- Transmission gate logic consists of an nMOS and a pMOS transistor in parallel with gates controlled by complementary signals.
- At least one of the two transistor is ON and the output voltage is either strong 0 or strong 1.
- It is superior than CMOS ckts interms of layout density, ckt delay and power consumption.
- Gate is driven by control signal.
- Source is connected with pass variable.

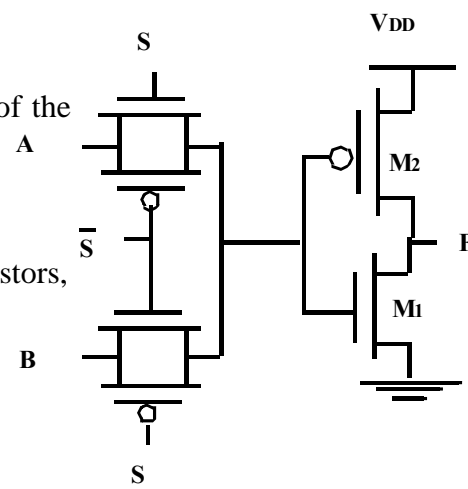


Input	Output
$g = 1, gb = 0$	$0 \rightarrow \text{strong } 0$
$g = 1, gb = 0$	$1 \rightarrow \text{strong } 1$

Transmission gate Multiplexer

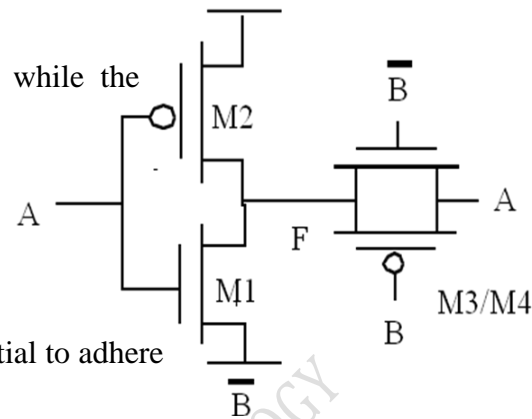
- The gate either selects input A or B on the basis of the value of the control signal S.
- TG output is given by $F = A \cdot S + B \cdot \bar{S}$.
- A complementary implementation of this gate requires 8 transistors, but the transmission gate logic needs only 6 transistors.

$$F = (S \cdot A + \bar{S} \cdot B)$$

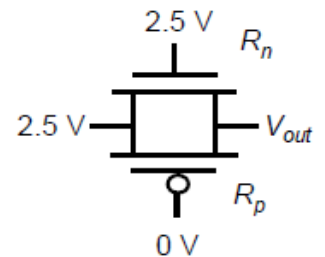
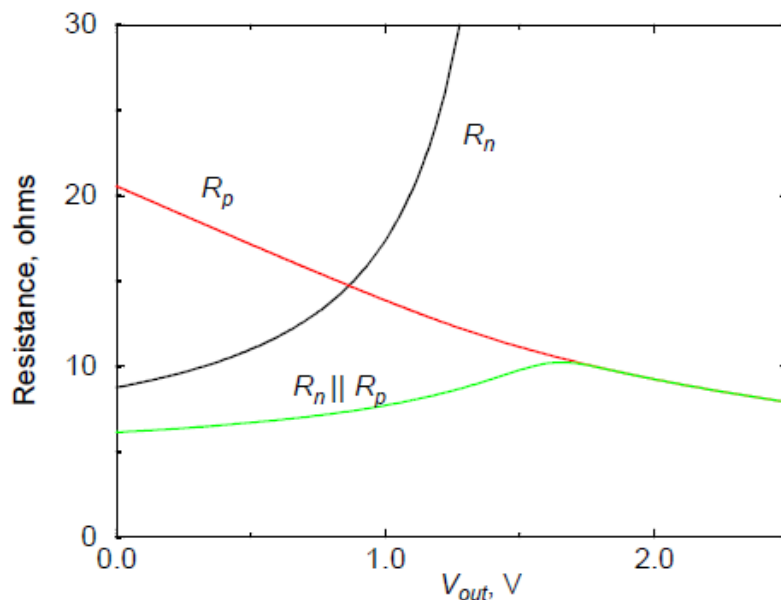


Transmission gate XOR

- For implementation TG-XOR Complementary CMOS requires 12 B transistor but it requires 6.
- For $B = 1$, transistors M1 and M2 act as an inverter while the transmission gate M3/M4 is off; hence $F = AB$.
- For $B = 0$, M1 and M2 are disabled, $F = AB$.
- For the values of A and B, node F always has a connection to either VDD or GND
- When designing static-pass transistor networks, it is essential to adhere to the low-impedance rule under all circumstances.



Performance of Transmission gates



$$R_n = (V_{DD} - V_{out}) / I_{Dn}$$

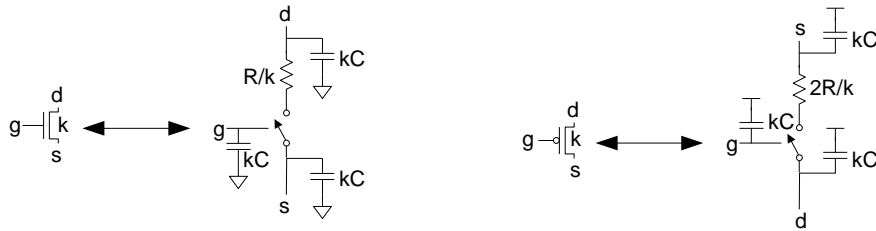
$$R_p = (V_{DD} - V_{out}) / -I_{Dp}$$

2) .Derive the expressions for effective resistance and capacitance estimation Using Elmore's RC delay model.

1)RC Delay Model

- The delay of logic gate is computed as the product of RC.
- Delay of logic gate is depends upon the transistor width in the gate & the capacitance of the load.
- Use equivalent circuits for MOS transistors
- Unit nMOS has resistance R, capacitance C
- Unit pMOS has resistance 2R, capacitance C
- Capacitance proportional to transistor width(k)

- Resistance inversely proportional to transistor width(k)
- If multiple transistor in series $\rightarrow R_{eff} = \text{sum of individual resistance}$.
- If multiple transistor in parallel $\rightarrow R_{eff} = \text{Resistance of the individual transistor}$

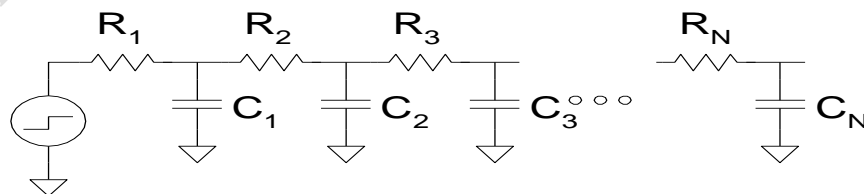


RC Values

- **Capacitance**
 - $C = C_g = C_s = C_d = 2 \text{ fF/mm}$ of gate width in 0.6 μm process and upto 1 fF/mm in 65 nm process.
- **Resistance**
 - $R \approx 10 \text{ KW}$ in 0.6 μm process
 - 1.25 KW in 65 nm process
- **Unit transistors**
 - May refer to minimum contacted device (4/2 1)
 - Or maybe 1 mm wide device

2) Elmore Delay

- Used to estimate delay value in RC ladder circuit
- ON transistors look like resistors.
- Pullup or pulldown network modeled as RC ladder
- Delay is equal to the sum over each node in the ladder of the resistance R_{n-i} between the node and is multiplied by the capacitance on the node.



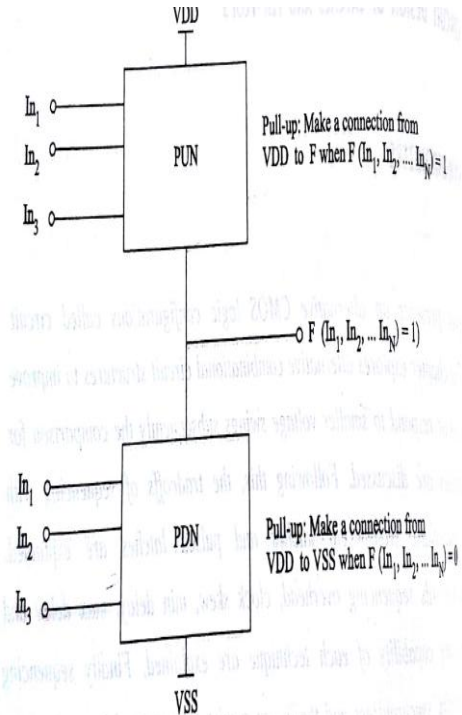
$$t_{pd} \approx \sum_{\text{nodes } i} R_{i \rightarrow \text{source}} C_i$$

$$= R_1 C_1 + (R_1 + R_2) C_2 + \dots + (R_1 + R_2 + \dots + R_N) C_N$$

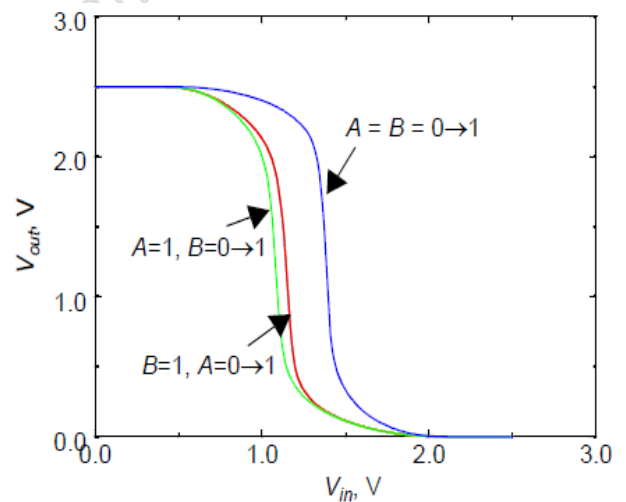
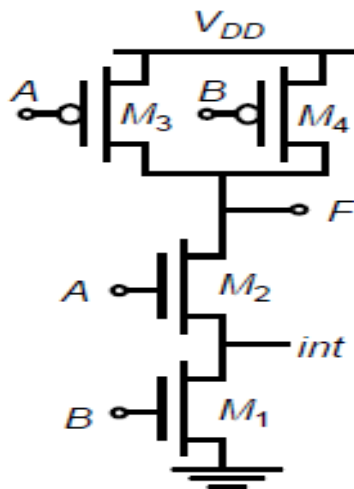
3) Write short notes on i) Static CMOS, ii) Bubble pushing, iii) Compound gates.

i) Static CMOS

- The static CMOS style is really an extension of the static CMOS inverter to multiple inputs.
- CMOS structure is low sensitivity to noise, good performance, and low power consumption with no static power dissipation.
- It is a combination of pull-up network(PMOS) & pull down network(NMOS).
- Each gate output is connected to either VDD or VSS
- The PUN and PDN networks are constructed in a mutually (one and only one of the networks is conducting in steady state).
- Path always exists between VDD and the output F, realizing a high output (“one”),or, alternatively, between VSS and F for a low output (“zero”).



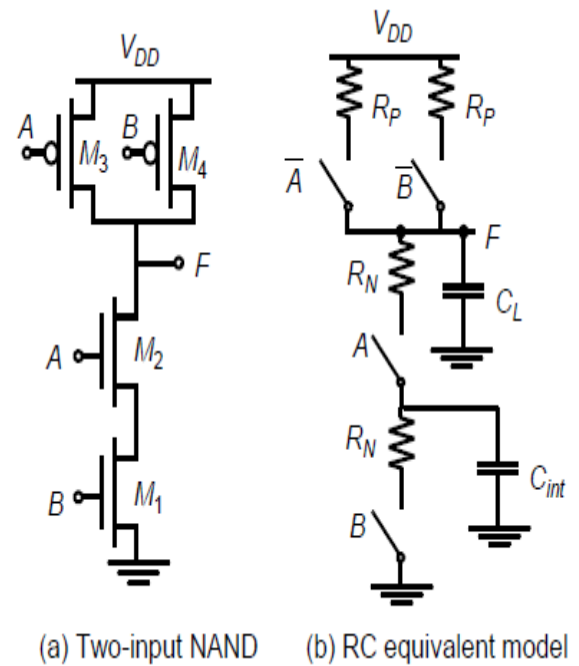
Static Properties of Complementary CMOS (NAND)



- case (a)→both transistors (M3,M4) in the PUN are on simultaneously for $A=B=0$, representing a strong pull-up.
- case (b&c)→only one of the pullup devices is on. The VTC is shifted to the left as a result of the weaker PUN.
- case (b)→ M3 is turned off, and the gate voltage of M2 is set to VDD. M2 may be considered as a resistor in series with M1. Since the drive on M2 is large, this resistance is small and has only a small effect on the voltage transfer characteristics.
- The threshold voltage of transistor $M2 > M1$. ($V_{GS2} = V_A - V_{DS1}$)
- case (c)→ transistor M1 acts as a resistor, causing body effect in M2. $V_{GS1} = V_B$

Propagation Delay of Complementary CMOS Gates

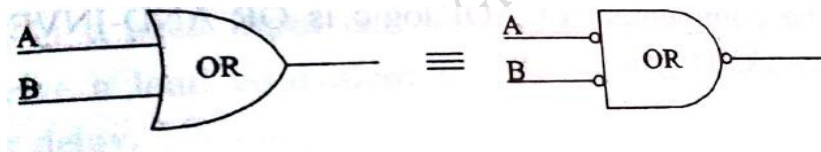
- The computation of propagation delay similar to the static inverter.
- For delay analysis, each transistor is modeled RC switch level model.
- propagation delay depends upon the input patterns.
- If both inputs are driven low, the two PMOS devices are on in parallel. The delay is $0.69 \times (R_p/2) \times C_L$
- when only one device turns on, delay is $0.69 \times R_p \times C_L$.
- For the pull-down path, the output is discharged only if both A and B are switched high, and the delay is given by $0.69 \times (2R_N) \times C_L$



(a) Two-input NAND (b) RC equivalent model

ii) Bubble pushing

- By introducing bubble at the input terminal.
- Static CMOS circuits are dual networks, obtained by Demorgans's theorem



- OR gate is equivalent to a NAND gate with bubbles at its input.
- Similarly (AND=NOR, NAND=NOR, NOR=OR)

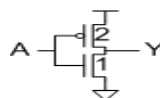
iii) Compound Gates (AOI-OAI Logic)

- AOI \rightarrow AND-OR-INVERT is a two level logic functions designed by one or more AND gates followed by a OR gate.
- OAI \rightarrow OR-AND-INVERT is a two level logic functions designed by one or more OR gates followed by a AND gate.

Logical effort of common of Gates

- INVERTER $\rightarrow g=n=1$
- NAND $\rightarrow g=(n+2)/3$
- NOR $\rightarrow g=(2n+1)/3$
- Parasitic delay=(summing size of transistor attached to the output/3)

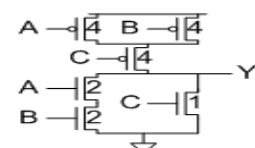
unit inverter
 $Y = \overline{A}$



$$g_A = 3/3$$

$$p = 3/3$$

AOI21
 $Y = \overline{AB + C}$



$$g_A = 6/3$$

$$g_B = 6/3$$

$$g_C = 5/3$$

$$p = 7/3$$

4) Illustrate the operation of dynamic CMOS Domino and NP Domino logic with necessary diagrams.

Dynamic CMOS

- Requires only $N+2$ transistors, less than static CMOS ($2N$).
- Logic function is implemented by the PDN only.
- The operation of this circuit is divided into two major phases: precharge and evaluation, with the mode of operation determined by the clock signal CLK.
- Full swing output ($V_{OL}=GND$ and $V_{OH}=VDD$)
- Faster switching speed.
- Small fan-out. (low no transistor, low no of capacitor)
- Power dissipation is good. (no short ckt power)
- PDN starts when input $\rightarrow V_{th}$

Modes of Operation

Precharge

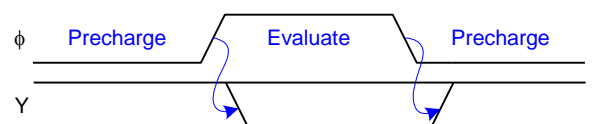
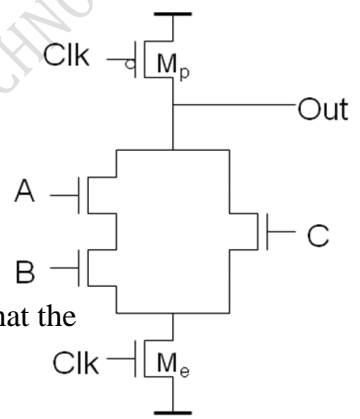
- When $CLK = 0$, the output node Out is precharged to VDD by the PMOS transistor M_p .
- During that time, the evaluate NMOS transistor M_e is off, so that the pull-down path is disabled.

Evaluation

- For $CLK = 1$, the precharge transistor M_p is off, and the evaluation transistor M_e is turned on.
- The output is conditionally discharged based on the input values and the pull-down topology.
- If the inputs are such that the PDN conducts, then a low resistance path exists between Out and GND and the output is discharged to GND.
- If the PDN is turned off, the precharged value remains stored on the output capacitance.
- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.

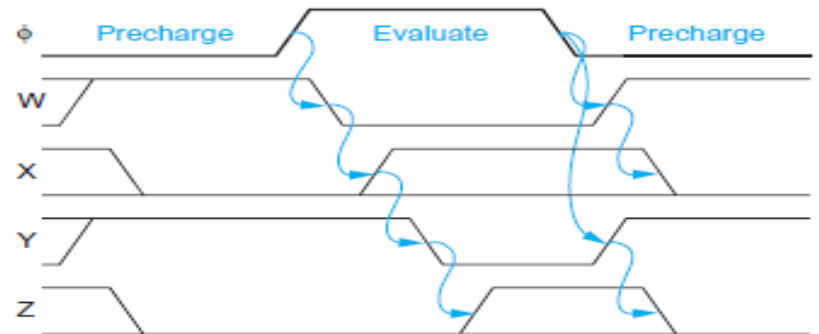
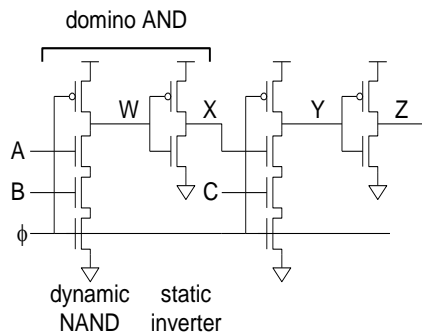
Conditions on Output

- During the precharge phase ($CLK=0$), the output is precharged to VDD regardless of the input values since the evaluation device is turned off.
- During evaluation ($CLK=1$), a conducting path is created between Out and GND if (and only if) $A \cdot B + C$ is TRUE.



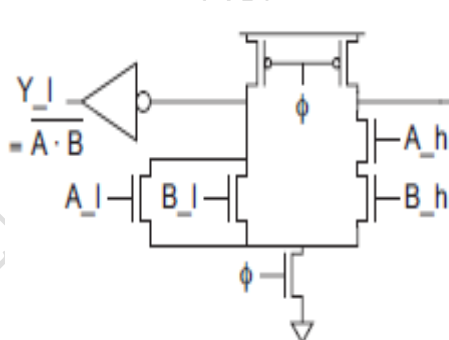
ii)Domino logic

- It converts the monotonically falling output into a monotonically rising signal suitable for the next gate.
- A single clock can be used to pre-charge and evaluate all the logic gates within the chain.
- The dynamic output is monotonically falling during evaluation, so the static inverter output is monotonically rising.
- Precharge occurs in parallel, but evaluation occurs sequentially.



iii)Dual-Rail Domino Logic

- Domino only performs non-inverting functions(AND, OR but not NAND, NOR, or XOR)
- Dual-rail domino gates accept both true and
- complementary inputs and compute both true and complementary outputs.
- Before computation completes, both rails are precharged.
- When the computation completes, one rail will be asserted.
- NAND gate can be used for completion detection



sig_h	sig_l	Meaning
0	0	Precharged
0	1	'0'
1	0	'1'
1	1	invalid

5)What are the sources of power dissipation in CMOS and discuss various design techniques to reduce power dissipation in CMOS

- Static Power dissipation→ due to leakage current when ckt is in idle mode.
- Dynamic Power dissipation→ when the ckt is working due to charging and discharging of capacitor.
- Short circuit Power dissipation→ during switching

1) Static Power

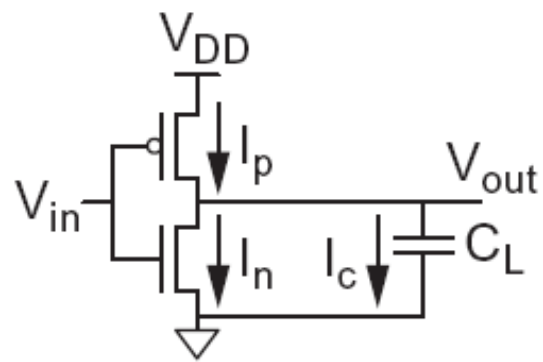
- Static power is consumed even when chip is off. (millions of transistor produce leakage current when temp increases)
- Estimate static power consumption.
 - Subthreshold leakage
 - Gate leakage 5 nA/mm
 - Junction leakage
 - $P_s = \sum_{i=1}^n (I_{static} \times \text{Supply voltage})$

2) Dynamic Power dissipation

- When the gate output rises, Energy stored in capacitor is $E_C = \frac{1}{2} C_L V_{DD}^2$
- But energy drawn from the supply is

$$E_{VDD} = \int_0^{\infty} I(t) V_{DD} dt = \int_0^{\infty} C_L \frac{dV}{dt} V_{DD} dt$$

$$= C_L V_{DD} \int_0^{V_{DD}} dV = C_L V_{DD}^2$$



- Half the energy from VDD is dissipated in the pMOS transistor as heat, other half stored in capacitor
- When the gate output falls
- Energy in capacitor is dumped to GND
- Dissipated as heat in the nMOS transistor $P_{switching} = \alpha C V_{DD}^2 f$

3) Short Circuit Current

- During switching, both nMOS and pMOS will conduct and provide a direct path between VDD for short circuit power dissipation.
- $P_{short} = V_{DD} \times I_{short}$

Total Power Dissipation

- Static power $\rightarrow P_{static} = (I_{sub} + I_{gate} + I_{junct} + I_{contention}) V_{DD}$
- Dynamic power $\rightarrow P_{dynamic} = P_{switching} + P_{shortcircuit}$
- Short Circuit Power $\rightarrow P_{short} = V_{DD} \times I_{short}$
- Total Power $\rightarrow P_{total} = P_{dynamic} + P_{static} + P_{short}$

KONGUNADU COLLEGE OF ENGINEERING AND TECHNOLOGY

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EC 8095 – VLSI DESIGN

UNIT – III SEQUENTIAL CIRCUITS DESIGN

COURSE HANDOUTS

PART -A

1. Compare SRAM and DRAM.

Both SRAMs and DRAMs are volatile in nature, (i.e.) Information is lost if power line is removed. However SRAMs provide high switching speed, good noise margin but require large chip area than DRAMs.

2. Define metastability

Metastability is a unknown state is neither 0 or 1. metastability happens for the design systems violating setup or hold time requirement.

3. Define setup and holding time

Set up time (t_{su}):

The time that the data input (D) is valid before the clock transition that is 0 to 1 transition for a positive edge -triggered registers

Hold time (t_{hold})

The time that the data input must remain valid after the clock edge.

4. Distinguish between a latches and flip flop.

S.No	Latches	Flip Flop
1	A Latch is Level-Sensitive	A FF is edge triggered.
2	A latch stores when the clock level is low and is transparent when the level is high.	A FF stores when the clock rises and is mostly never transparent.

5. Define Skew and Jitter

Skew:

Clock skew defined as a spatial variation in arrival time of a clock transition on an integrated circuit

Jitter:

Clock jitter is a temporal variation of the clock period at a given point on the chip.

6. Define pipelining

Pipelining is a popular design technique often used to accelerate the operation of the data path in digital processors. The major advantages of pipelining are to reduce glitching in complex logic networks and getting lower energy due to operand isolation.

7. What is C²MOS register

The positive edge triggered register based on master slave concept insensitive to clock overlap. This is called clocked CMOS or C²MOS.

8. What is NORA CMOS?

NORA-CMOS is a logic circuit that combines C²MOS pipeline and NORA dynamic logic function blocks. Each module consists of a block of combinational logic with a mixture of static and dynamic logic followed by a C²MOS latch.

9. Write the importance of Sense amplifiers

Sense amplifier play a major role in the functionality, performance and reliability of memory circuits.

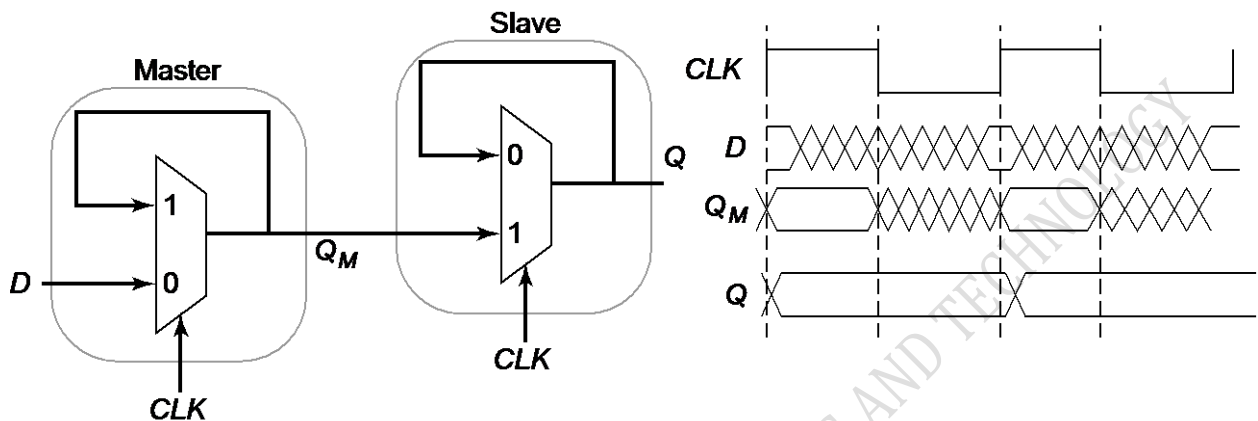
The following are the functions of sense amplifier

- i. Amplification
- ii. Delay reduction
- iii. Power reduction
- iv. Signal restoration

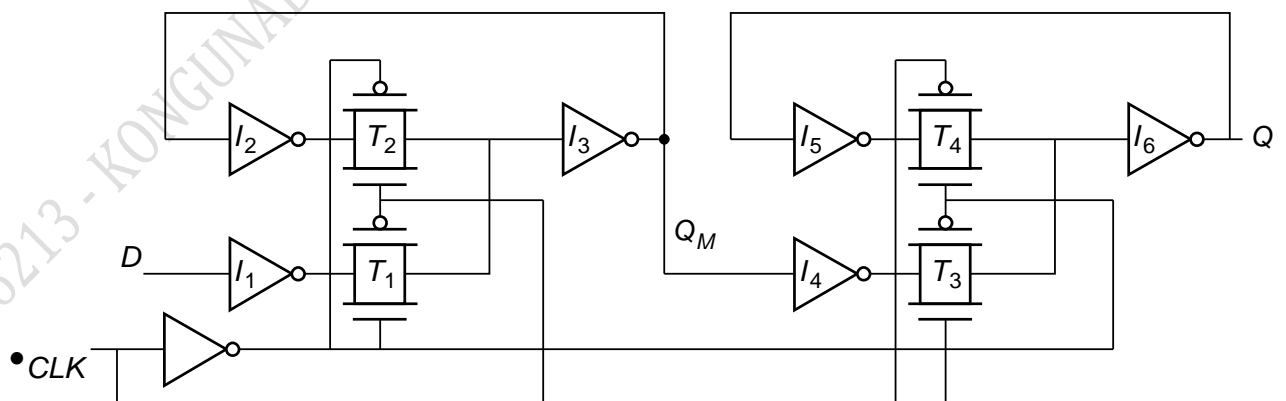
10. Define Race condition?

When a CLK and CLK both are high for a short period of time (overlap period), both sampling pass transistors conduct and there is a direct path from the D input to a Q output. So output change at the rising edge of clock, which is undesired for a negative edge triggered register. This is called race condition

1. a.) Explain the operation of master-slave edge based triggered register.

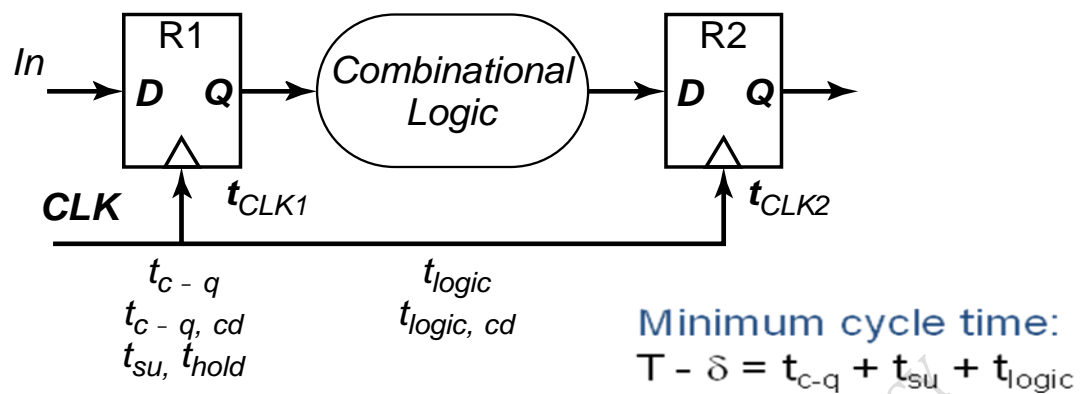


- The register consists of cascading a negative latch (master stage) with a positive latch (slave stage).
- If clock is Low, the master stage is ON and the D input is passed to the master stage output Q_M. During this period, the slave stage is OFF or hold mode, keeping its previous value using feedback.
- On the rising edge of the clock, the slave stage is ON and copy the Q_M value to Q, while the master stage is off and remains in a hold mode.
- Since Q_M is constant during the high phase of the clock, the output Q makes only one transition per cycle.



- When the clock is low, T₁ is on and T₂ is off, and the D input is copied to Q_M via I₃. During this period, T₃ is off and T₄ is on and the cross-coupled inverters (I₅, I₆) holds the state of the slave latch.
- When the clock goes high, T₁ is off and T₂ is on, and the cross-coupled inverters I₃ and I₄ holds the state of Q_M. Also, T₃ is on and T₄ is off, and Q_M is copied to the output Q.

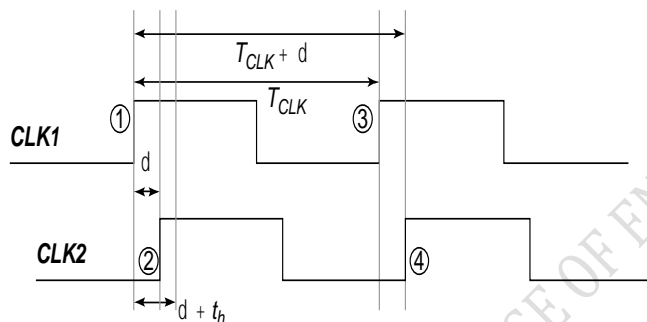
2) Describe in details about timing basics and clock distribution techniques in synchronous design.



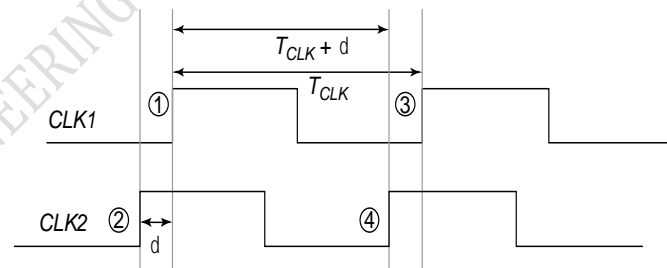
- The clock at registers 1 and 2 have the same clock period and transition the exact same time. The following timing parameters characterize the timing of the sequential circuit.

• Clock Skew

Positive Skew



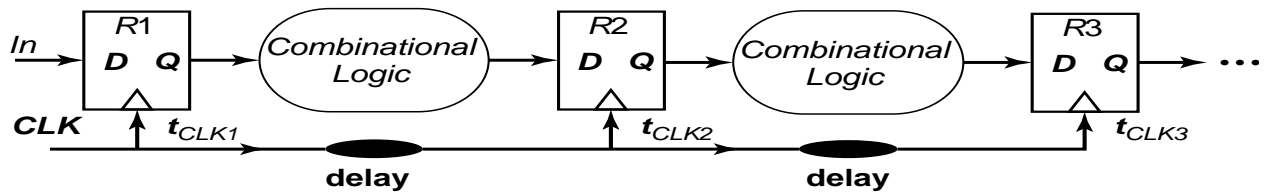
Negative Skew



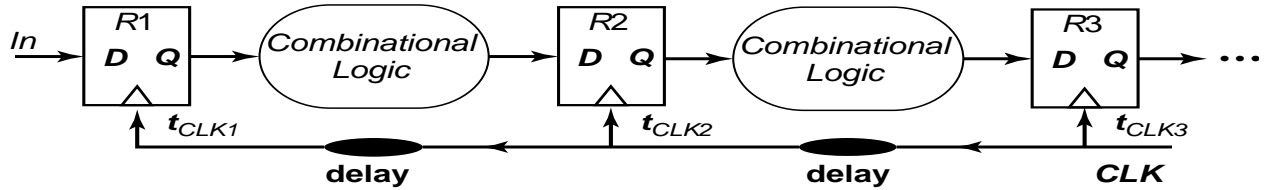
- The spatial variation in arrival time of a clock transition on an integrated circuit is commonly referred to as *clock skew*.
- The clock skew between two points i and j on a IC is given by $\delta_{(i,j)} = t_i - t_j$
- where t_i and t_j are the position of the rising edge of the clock with respect to a reference.
- The clock skew can be positive or negative depending upon the routing direction and position of the clock source.

Positive and Negative Skew

- $\delta > 0 \rightarrow$ This corresponds to a clock routed in the same direction as the flow of the data through the pipeline.
- $\delta < 0 \rightarrow$ When the clock is routed in the opposite direction of the data, the skew is negative and condition.

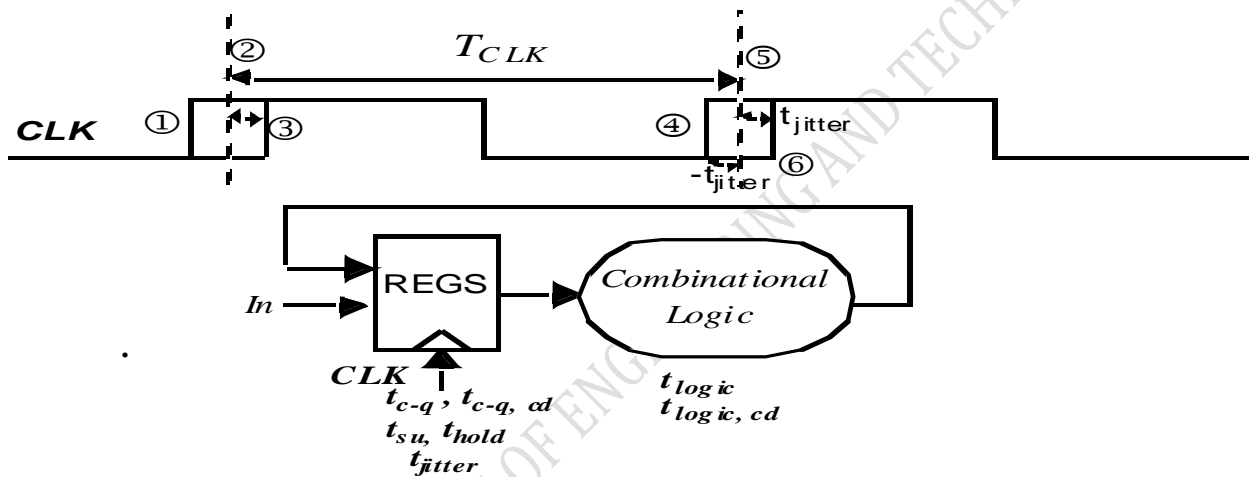


(a) Positive skew



(b) Negative skew

Impact of Jitter



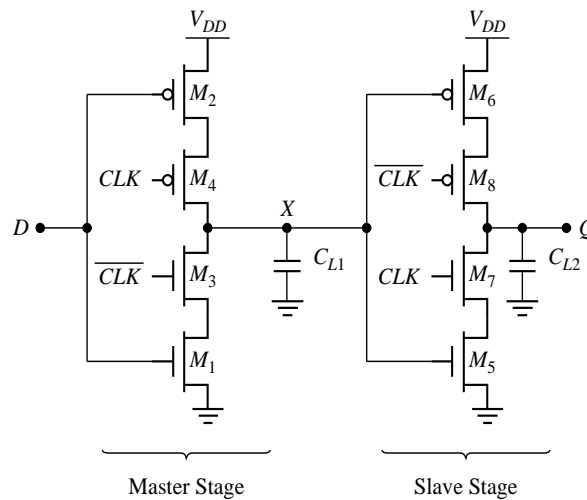
- Clock jitter refers to the temporal variation of the clock period at a given point.
- The clock period can reduce or expand on a cycle-by-cycle basis
- If launching edge is late and receiving edge is early, the data will not be too late if:
- $T_{c-q} + T_{LM} + T_{SU} < T - T_{JL,1} - T_{JL,2} - d$
- Minimum cycle time is determined by the maximum delays through the logic
- $T_{c-q} + T_{LM} + T_{SU} + d + 2 T_{JI} < T$

3). Write Short notes on following

(i) C²MOS Register

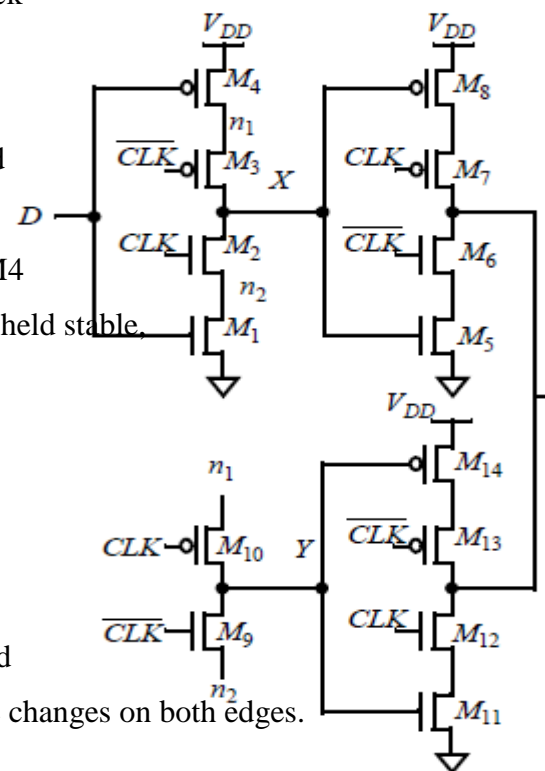
- If CLK = 0 → The first tri-state driver is ON, and the master stage acts as an inverter.
- The master stage (M3-M4) is in the evaluation mode and the slave stage is in a hold mode.
- Both transistors M7 and M8 are off, decoupling the output from the input. The output Q retains its previous value stored in CL2.
- If CLK = 1 → The master stage is in hold mode (M3-M4 off), slave stage evaluates (M7-M8 on).

- The value stored on CL1 propagates to the output node through the slave stage.

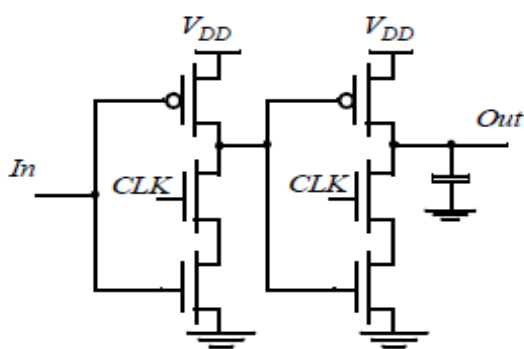


C²MOS based Dual-edge Registers

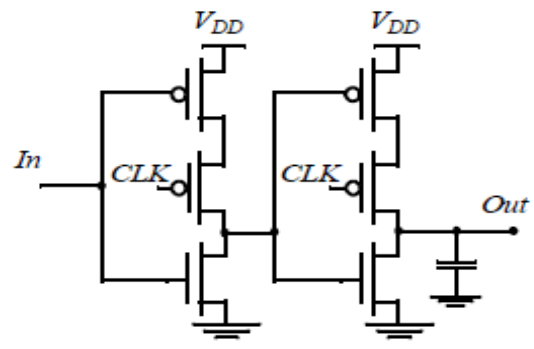
- This sequential circuit sampling the input on both clock edges.
- It consists of two parallel master slave based edge-triggered registers, whose outputs are multiplexed using the tri-state drivers.
- When clock is high, the positive latch transistors M1-M4 is sampling the inverted D input on node X. Node Y is held stable, since devices M9 and M10 are turned off.
- When clock is low, the top slave latch M5-M8 on, and drives the inverted value of X to the Q output.
- When clock is low, transistors (M9, M10) is turned on, sampling the inverted D input on node Y.
- On the rising edge, the bottom slave latch conducts, and drives the inverted version of Y on node Q. Data hence changes on both edges.



(ii) True Single phased clocked register



Positive Latch



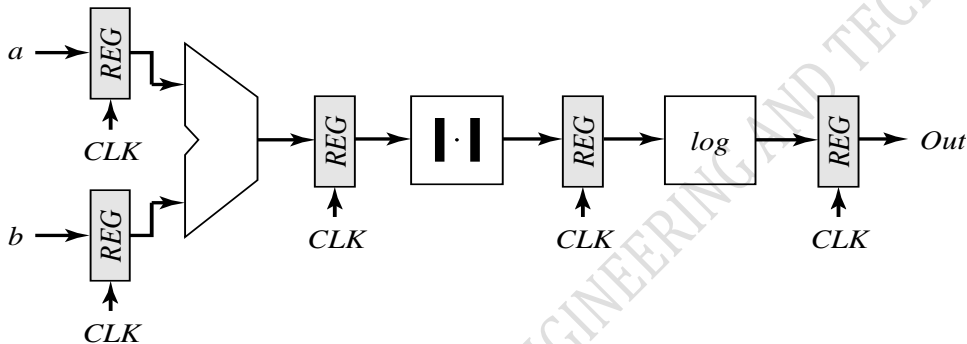
Negative Latch

- It uses a single phase clock.
- For the positive latch, when CLK is high, the latch is in the transparent mode.
- The latch is non-inverting state , and propagates the input to the output.
- when CLK = 0, both inverters are disabled, and the latch is in hold-mode.
- pull-up networks are activated, and the pull-down circuits are deactivated.
- As a result , no signal can ever propagate from the input of the latch to the output in this mode.

4) Discuss in detail various pipelining approaches to optimize the sequential circuits.

- Pipelining is design technique used to accelerate the operation of the datapaths in digital processors.

Pipelined circuit compute $\log(|a + b|)$



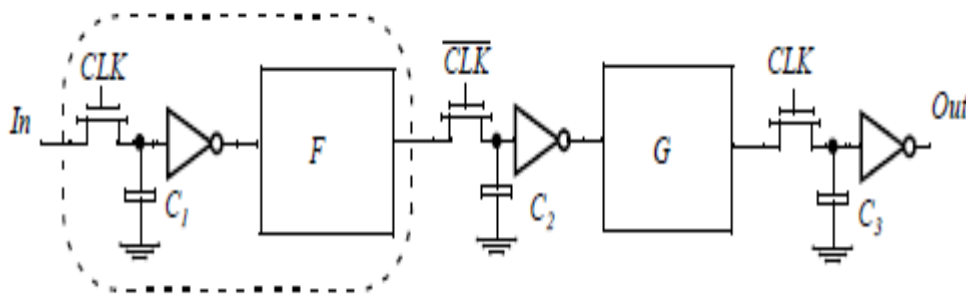
- Pipelining is a technique to improve the resource utilization, and increase the functional throughput.
- Use registers between the logic blocks.
- The computation for one set of input data to spread over a number of clock periods.
- The result for the data set (a_1, b_1) only appears at the output after three clock-periods.
- At that time, the circuit has already performed parts of the computations for the next datasets, (a_2, b_2) and (a_3, b_3).
- The advantage of pipelined operation is need minimum clock period.
- The combinational circuit block has been partitioned into three sections, each of which has a smaller propagation delay than the original function.
- The minimum allowable clock period is

$$T_{\min, \text{pipe}} = t_{c-q} + \max(t_{pd, \text{add}}, t_{pd, \text{abs}}, t_{pd, \text{log}})$$

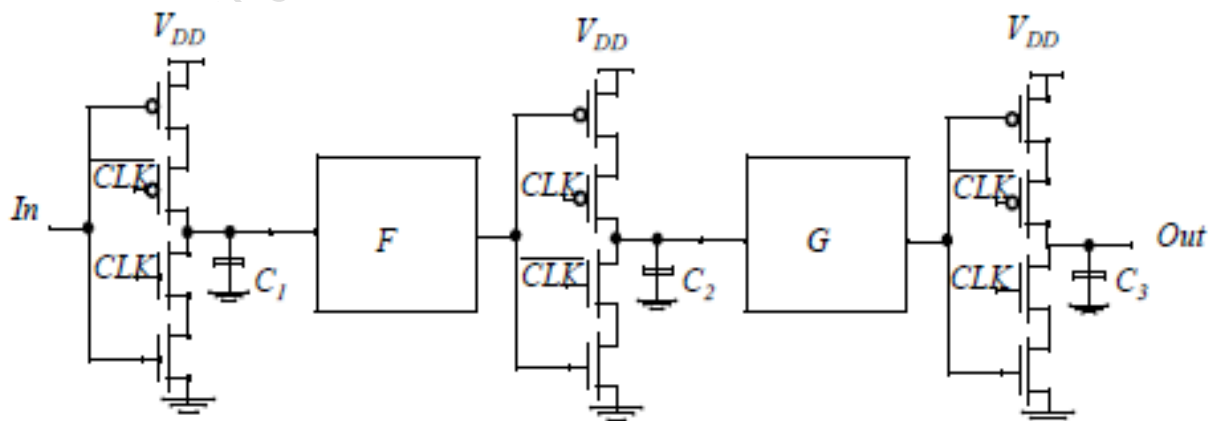
Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 + b_1$		
2	$a_2 + b_2$	$ a_1 + b_1 $	
3	$a_3 + b_3$	$ a_2 + b_2 $	$\log(a_1 + b_1)$
4	$a_4 + b_4$	$ a_3 + b_3 $	$\log(a_2 + b_2)$
5	$a_5 + b_5$	$ a_4 + b_4 $	$\log(a_3 + b_3)$

ii) Latch- Vs Register-Based Pipelines

- The pipeline system is implemented based on pass-transistor-based positive and negative latches instead of edge triggered registers.
- Logic is introduced between the master and slave latches of a master-slave system.
- When the clocks CLK and $\overline{\text{CLK}}$ are non-overlapping, correct pipeline operation is obtained.
- Input data is sampled on C1 at the Positive edge of CLK and the computation of logic block F starts and is stored on C2 on the falling edge of CLK, Computation of logic block G starts.
- The value stored on C2 at the end of the CLK low phase is the result of passing the previous input through the logic function F.
- When overlap exists between CLK and $\overline{\text{CLK}}$, the next input is already being applied to F, and its effect might propagate to C2 before CLK goes low



iii) NORA-CMOS Based Pipelined Structures



- A C^2MOS -based pipelined circuit is race-free as long as all the logic functions F between the latches are non-inverting.
- During a (0-0) overlap between CLK and $\overline{\text{CLK}}$, all C^2MOS latches, simplify to pure pull-up networks.
- The only way a signal can race from stage to stage under this condition is when the logic function F is inverting.

KONGUNADU COLLEGE OF ENGINEERING AND TECHNOLOGY

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EC 8095 – VLSI DESIGN

UNIT – IV DESIGN OF ARITHMETIC BUILDING BLOCKS AND SUBSYSTEMS

COURSE HANDOUTS

PART -A

1. List of the components of data path

A Datapath consists of interconnection of combinational functions such as arithmetic (addition, multiplication, comparison and shift) or logical (AND, OR and XOR) operations.

2. Give the application of high speed adder

Mainframe computer, servers, multimedia processors.

3. How to design a high-speed adder

In a high speed adder, a carry propagation delay is reduced by using carry bypass adder or linear carry select adder or square root carry select adder or carry lookahead adder.

4. What is latency

The latency is, time taken for to get a output in a register, after giving a input.

5. What is meant by bit-sliced data path organization

Data in a processor are operated in word-based manner. Datapath in microprocessor are 32 or 64 bit wide. The signal processing data paths in digital Subscriber Line (DSL) modems, magnetic disk drives, or compact-disc players are 5 to 24 bits wide. A 32 bit processor operates on data words that are 32 bit wide. This is because the same operation is performed on each bit of the data word. The Datapath consists of 32 bits slices and each operations on a single bit hence called bit-sliced.

6. Define a propagation delay for n-bit fast adders

The propagation delay for n-bit carry bypass adder is

$$t_{\text{adder}} = t_{\text{setup}} + M t_{\text{carry}} + (N/M-1)t_{\text{bypass}} + (M-1)t_{\text{carry}} + t_{\text{sum}}$$

The propagation delay for n-bit linear carry select adder is

$$t_{\text{carry}} = t_{\text{setup}} + M t_{\text{carry}} + (N/M)t_{\text{mux}} + t_{\text{sum}}$$

The propagation delay for n-bit square root carry select adder is

$$t_{\text{add}} = t_{\text{setup}} + M t_{\text{carry}} + (\sqrt{2N})t_{\text{mux}} + t_{\text{sum}}$$

7. Why barrel shifter is very useful in arithmetic circuits

- i. A barrel shifter is a digital circuit that can shift a data word by a specified number of bits without the use of any sequential logic, only pure combinatorial logic

- ii. Barrel shifter performs a six operation, namely; logical right shift, logical left shift, arithmetic right shift, arithmetic left shift, rotate right, rotate left
- iii. Propagation delay is constant and independent of the shift value.
- iv. Layout size is not dominated by transistors.

8. Write the principle of fast multiplier

Fast multiplier is similar to manually computing multiplier operation. All the partial products are generated at the same time and organized in an array, but in fast multiplier to compute a final products a multi operand addition is used.

9. Define mirror adder

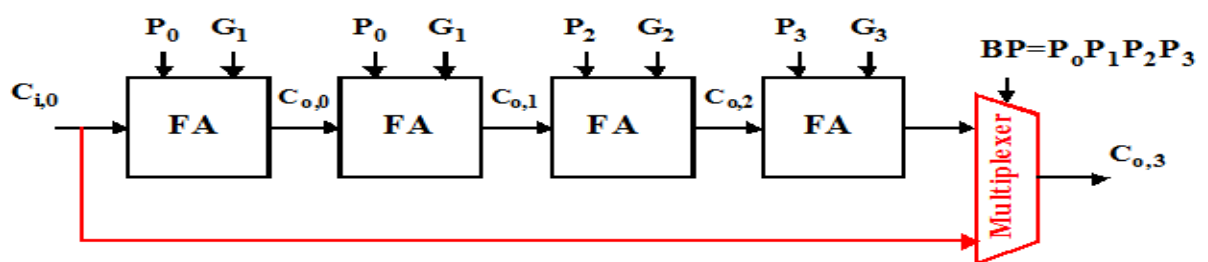
In a mirror adder, the realization of pMOS network is identical to nMOS rather than the conduction complement. Thus, topology is called mirror adder.

10. Define DVS.

To obtain required throughput for high workloads and minimize energy for low workloads, both supply and frequency must be dynamically varied according to the requirements applications that is currently being executed. This technique is called dynamic voltage scaling (DVS)

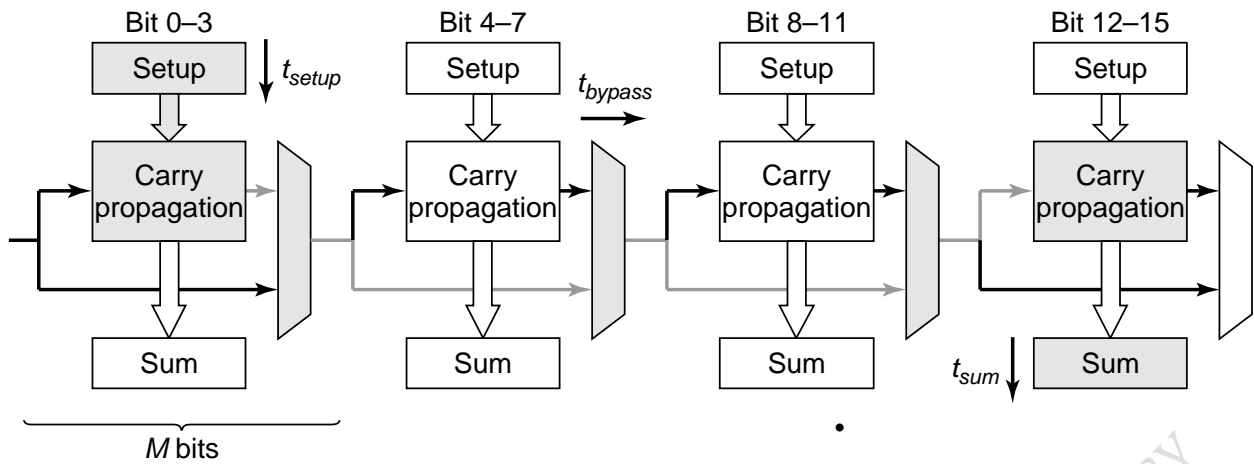
PART -B

1) Design a 16 bit carry bypass and carry select adder and discuss their features



Idea: If (P_0 and P_1 and P_2 and $P_3 = 1$)
then $C_{o,3} = C_0$, else “kill” or “generate”.

- When $BP = P_0 P_1 P_2 P_3$ is 1 \rightarrow the very first incoming carry pass to bypass transistor, otherwise the carry is obtained via the normal route.



•For computing delay of an N-bit adder, the total adder is divided in to N/M equal length with M bits.

•The worst case delay for 16-bit carry bypass adder is given by

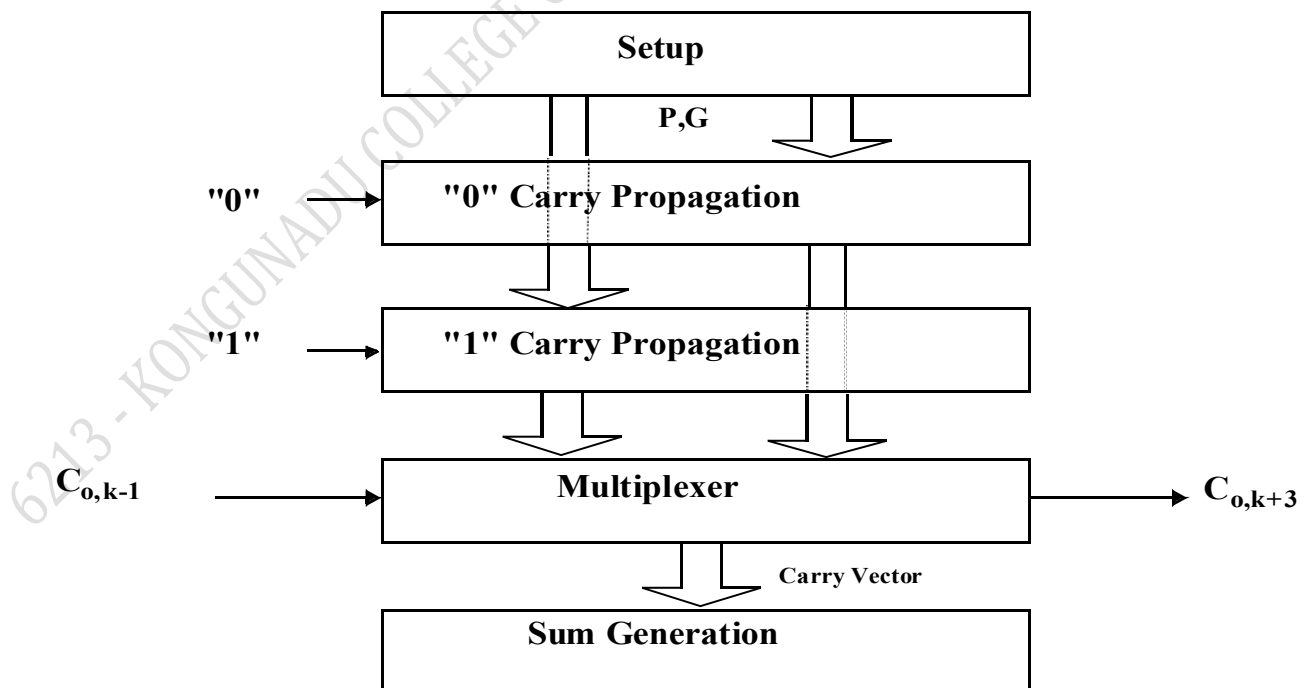
$$t_{\text{adder}} = t_{\text{setup}} + M t_{\text{carry}} + (N/M - 1) t_{\text{bypass}} + (M - 1) t_{\text{carry}} + t_{\text{sum}}$$

• t_{setup} → fixed overhead time to create the generate and propagate signal

• t_{carry} → propagation delay through single bit

• t_{bypass} → propagation delay through the bypass mux of a single stage

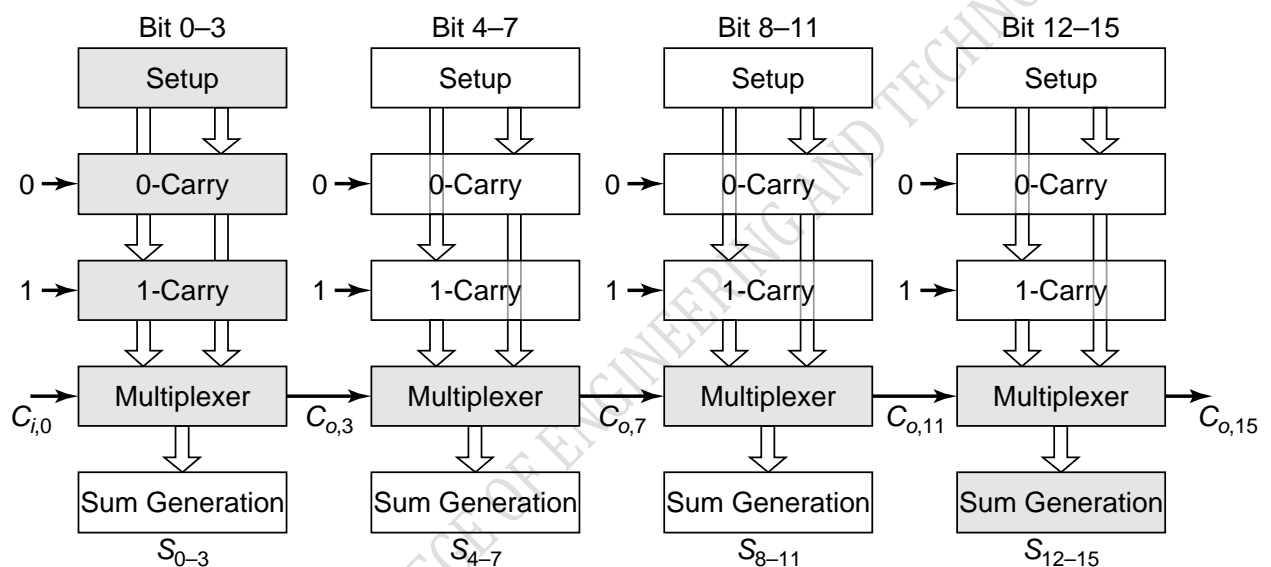
• t_{sum} → time to generate the sum of the final stage



•In ripple carry adder, every full adder has to wait for the incoming carry.

•In this method, consider both the possible values of carry input(0 or 1)and evaluate the result for both in advance.

- Once the real value of incoming carry is known, the correct result is selected using a multiplexer stage with min delay.
- The worst case propagation delay is given as
- $t_{\text{carry}} = t_{\text{setup}} + Mt_{\text{carry}} + (N/M)t_{\text{mux}} + t_{\text{sum}}$
- $N \rightarrow$ Total number of bits
- $M \rightarrow$ Number of bits per stage respectively
- $t_{\text{carry}} \rightarrow$ delay of carry through a single full adder.
- The carry delay in a single block is proportional to the length of that stage or equals M
- The proportional delay of adder is linearly proportional to N.
- Because the block-select signal selects between 0 and 1 ripple through all stages in the worst case.



Advantages

- Less propagation delay
- Reduce the computation delay

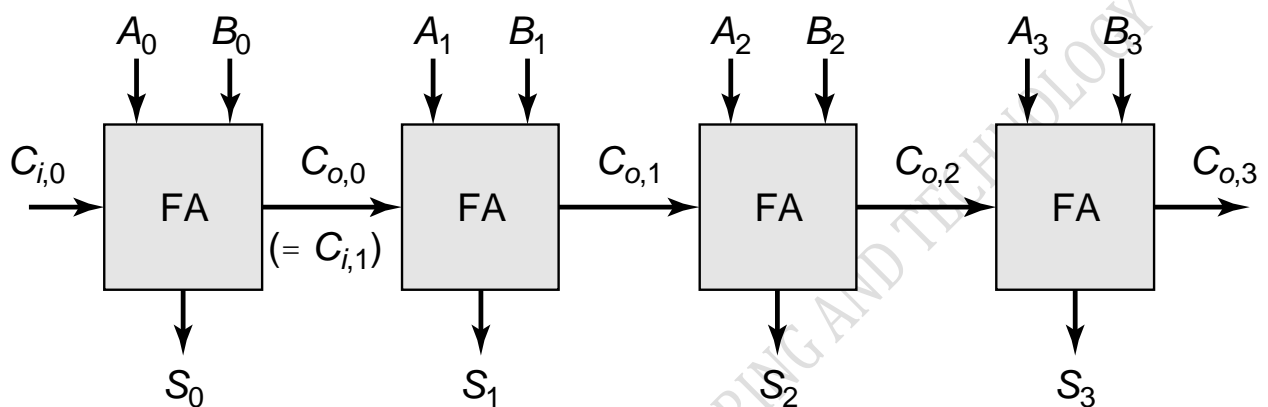
Drawbacks \rightarrow High power consumption

2) Sketch the structure of ripple carry adder and explain its operation. How the drawbacks in ripple carry adder overcome by carry look ahead adder and discuss.

Ripple-Carry Adders

- N-bit Adder can be constructed by cascading N full adder circuits in series, connecting $C_{0,k-1}$ to $C_{i,k}$ for $k=1$ to $N-1$ and the first carry in $c_{i,0}$ to 0.
- In ripple carry adder the Carry bit ripples from one stage to the other.
- The circuit delay depends upon the number of logic stages that must be traversed and is a function of the applied input signals.

- For some input signals→no ripple occurs. or
- For some input signals→ the carry has to ripple all the way from LSB to MSB.
- The propagation delay(critical path) is the worst case delay over all possible input patterns.
- Delay is proportional to the number of bits in the input words N is given by
- t_{carry}→ propagation delay from C_i to C₀
- t_{sum}→ propagation delay from C_i to S



Advantages

- Consumes less power
- Compact layout giving Smaller chip area

Drawbacks

- Delay is linearly proportional to the number of bits
- Performance decrease with increase in number of bits.
- Worst case delay for N-bit adder is 2N gate delay.

(ii) carry look ahead adder

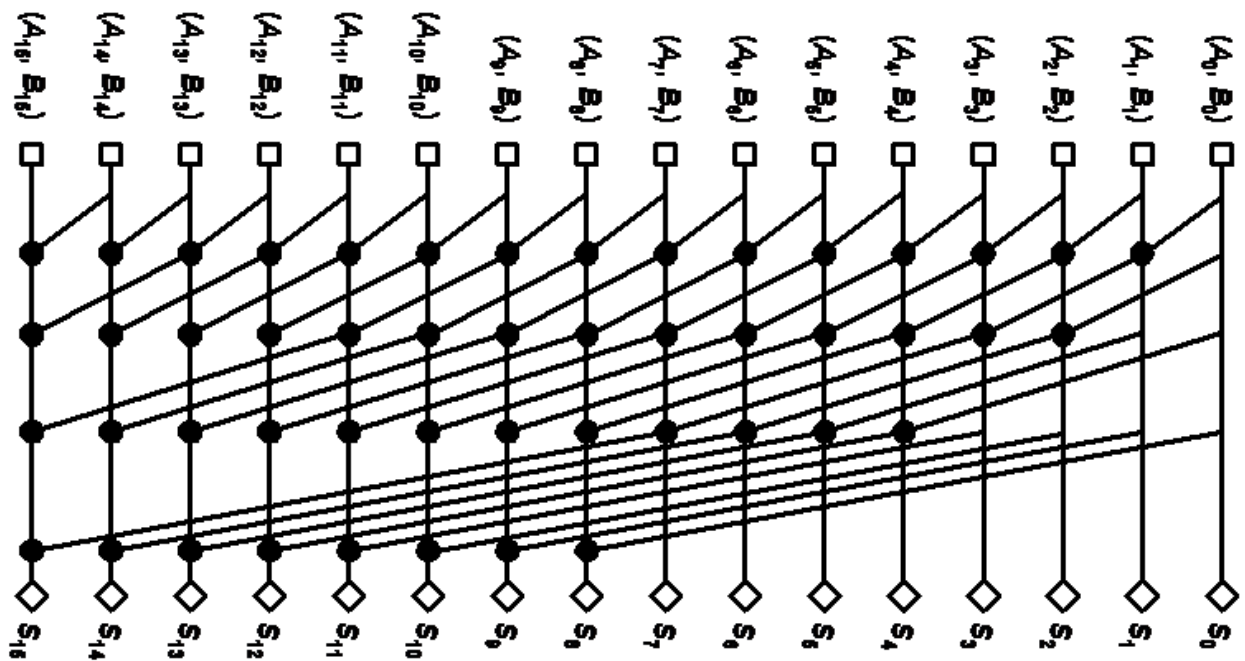
- For high speed adders, the carry propagation and generation are organized into
- recursive trees.
- For effective implementation→decomposing the carry propagation into subgroups of Nbits.

$$\begin{aligned}
 C_{o,0} &= G_0 + P_0 C_{i,0} \\
 C_{o,1} &= G_1 + P_1 G_0 + P_1 P_0 C_{i,0} \\
 C_{o,2} &= G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_{i,0} \\
 &= (G_2 + P_2 G_1) + (P_2 P_1)(G_0 + P_0 C_{i,0}) = G_{2:1} + P_{2:1} C_{o,0}
 \end{aligned}$$

- Carry propagation process is decomposed into subgroups of 2 bits generate (G_{i,j}) and propagate (P_{i,j}).

- $G_{i,j}$ is true \rightarrow if the groups generate carry
- $P_{i,j}$ is true \rightarrow if an incoming carry propagates through the complete group.

16-bit radix-2 Kogge-Stone tree



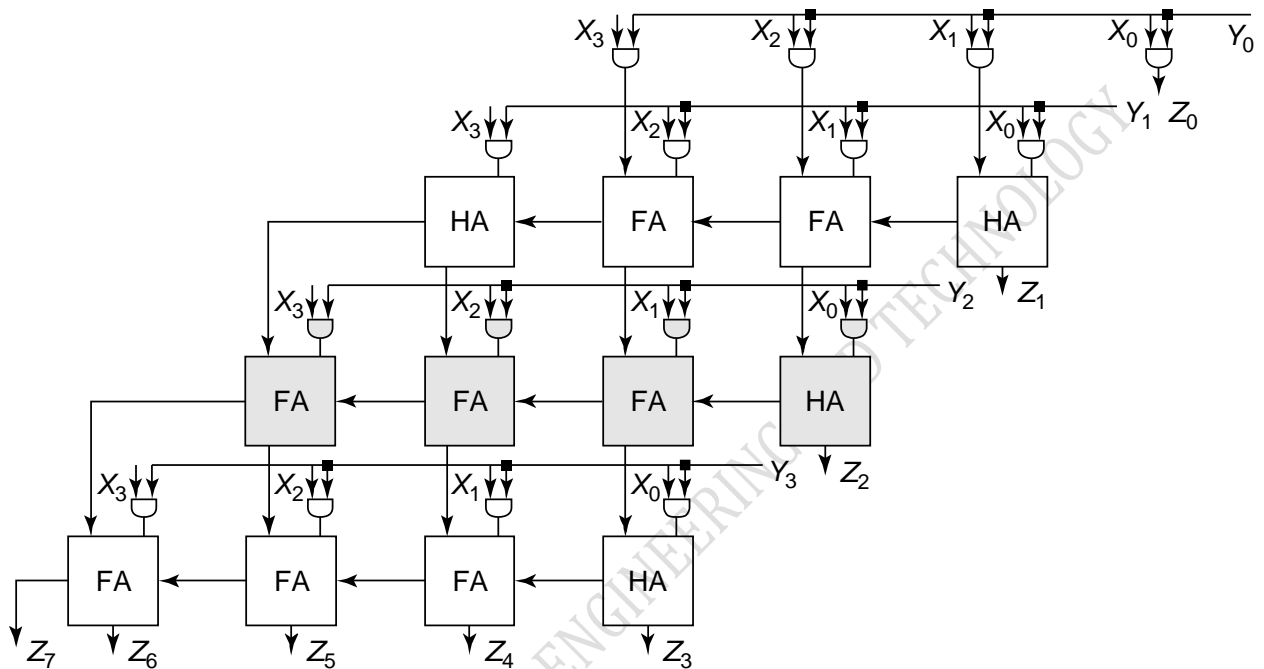
- The carry at position 15 is computed by combining the results of blocks(0:7) and(8:15).
- Each of these in turn is composed hierarchically.
- For instance,(4:7) is the composition of (0:3)..
- Also (8:15) is the composition of (4:11)..
- Also (0:3) consists of (0:1) and (2:3)etc..,

3) Design a 4X4 array multiplier and write down the equation for delay.

- Generation of N partial products requires $N \times M$ 2-bit AND gates.
- Multipliers most area is utilized to add the N partial products.
- This requires N-1 M-bit address.

- Shifting of the partial products for proper alignment is performed by simple routing and does not require any logic.
- The overall structure compacted into a rectangle to get a very efficient layout.
- Propagation delay is given by

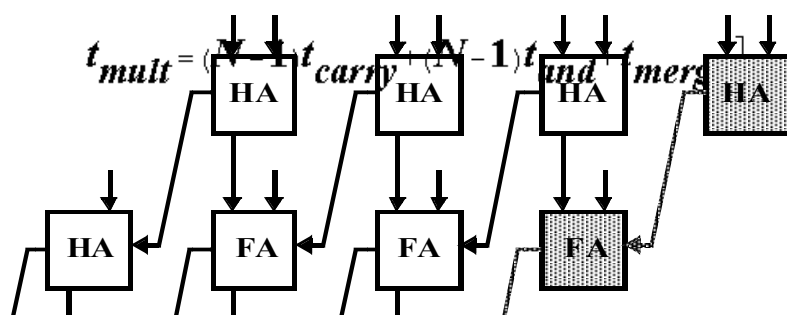
$$t_{mult} \approx [(M-1) + (N-2)]t_{carry} + (N-1)t_{sum} + (N-1)t_{and}$$



- t_{sum} → delay between the input carry and sum bit of the full adder
- t_{carry} → propagation delay between input and output carry.
- t_{and} → AND gate delay
- All critical paths have same length.
- Speeding up one of them by replacing one adder by a fast one such as a carry-select adder does not make much sense.

4) Give a note on 4X4 carry save multiplier.

- An extra adder called vector-merging adder is added to generate the final result.
- The resulting multiplier is called a carry-save multiplier.
- In this carry bits are not immediately added but are saved for the next adder stage.
- In the final stage, carry and sum are merged using a carry look ahead adder.
- The worst case critical path is given by



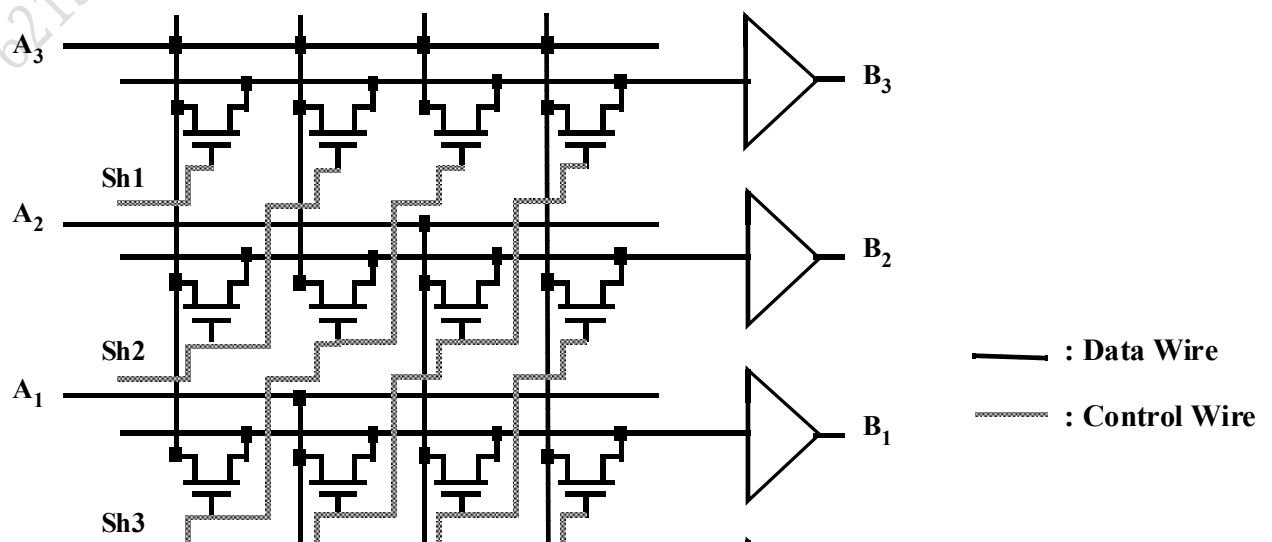
Advantages

- Shorter worst case critical path
- Drawbacks
- Increased area cost (because of extra adder)

5) Write a short note on

(i) Barrel shifter.

- It consists of an array of transistors, in which the number of rows equals the word length of the data and the number of columns equals the maximum shift width.
- The control wires are routed diagonally through the array.
- Switch gates formed together in groups of fours and also form 4 separate groups corresponding to shifts of 0, 1, 2, and 3 bits. This arrangement is called barrel shifter.
- Barrel shifters perform 6 operations namely logical right & left shift, arithmetic right shift & left shift, rotate right & rotate left.
- The inter bus switches have gate inputs connected in stair case manner in groups of four and have four shift control inputs that mutually exclusive in the active state.
- CMOS gates are used as switches.
- Barrel shifter connects the input lines representing a word to a group of output lines with required shift determined by control inputs Sh0, Sh1, Sh2, and Sh3.
- Control inputs decide the direction of the shift.
- If input word has n-bits, shifts from 0 to n-1 bit positions are possible.



- Layout size in barrel shifter is not dominated by the active transistors, but by the number of wires running through the cell.
- The size of the cell is bounded by the pitch of the metal wires.
- When selecting a shifter, the format in which to present the shift value is provided.
- Barrel shifter needs a control wire for every shift bit.
- A 4-bit shifter needs four control signals.
- In a processor the required shift value comes in an encoded binary format.
- The encoded control word needs two control signals and is represented as 11 for a shift over 3 bits.

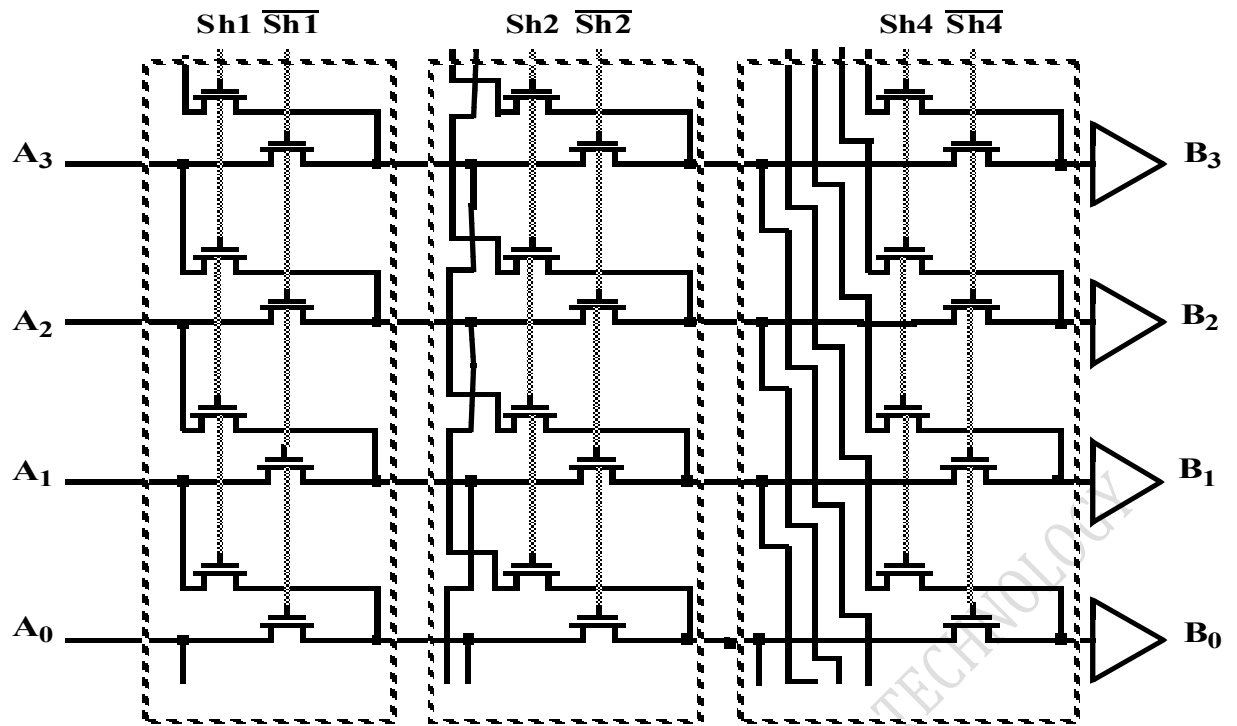
Advantages

- Signal has to pass through at most one transmission gate
- Propagation delay is constant and independent of the shift value
- Layout size is not dominated by transistors.

Drawbacks

- Capacitance at the input of the buffers rises linearly with the max shift width.
- Used for small shift values
- Separate decoder is needed for decoding control inputs

(ii) Logarithmic shifter



- Logarithmic shifter uses staged approach for shifting.
- The total shift value is decomposed into shifts over powers of two.
- A shifter with a maximum shift width of M consists of a $\log_2 M$ stages, where the i th stage either shifts over 2^i or passes data unchanged.
- To shift over 5 bits, the 1st stage is set to shift mode, the 2nd to pass mode and the last stage again to shift.
- The control word for this shifter is already encoded and no separate decoder is required.
- Speed of the logarithmic shifter depends on the shift width in a logarithmic way.
- An M -bit shifter requires $\log_2 M$ stages. The series connection of pass transistors slows down the shifter for larger shift values.
- For larger shift values, the logarithmic shifter becomes more effective, in terms of both area and speed.
- The logarithmic shifter is easily parameterized, allowing for automation generation.

KONGUNADU COLLEGE OF ENGINEERING AND TECHNOLOGY

(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EC 8095 – VLSI DESIGN

UNIT – V IMPLEMENTATION STRATEGIES & TESTING

COURSE HANDOUTS

PART – A

1. What is meant by CBIC and standard cell?

Cell based ASIC or cell based integrated circuits(CBIC), which uses a predesigned logic cells like AND gates, OR gates, multiplexers and flipflops.

Here the predesigned logic cells are known as standard cell. The standard cell are also called as flexible blocks.

2. Name the elements in a configuration logic block

In general logic block consist of few logic cells, a typical logic cell consists of LUT (Look Up Table), a full adder and a D-type flip flop.

3. What are the feed through cells? State their uses

- ✓ In a cell-based ASIC, a connection that needs to cross over a row of standard cells uses a feedthrough.
- ✓ Feedthrough is a piece of metal used to pass a signal through a cell.

4. State the features of full custom design

- ✓ Some (possibly all) logic cells that are customized.
- ✓ All mask layers that are customized.
- ✓ Manufacturing lead time is typically eight-weeks.
- ✓ Needs less area and low power consumption

5. Compare full custom with semi-custom

Full Custom	Semi-Custom
All the logic cells and masks are customized	All the logic cells are predesigned, and some of the mask layers are customized.
Increased manufacturing and design time	Less Time.
Highly complex in design system.	This uses cell library so Easier design process
Example- microprocessor	Example – FPGA, PLD

6. What is ULSI?

Ultra Large Scale Integration (ULSI) is a process of embedding a million of transistor with in a single chip.

7. What are the various ways of routing procedure.

Routing architecture comprises of programmable switches and wires. Routing provides connection between I/O blocks and logic blocks, and between one logic block and another logic block.

- ✓ General purpose programmable interconnect
- ✓ Direct interconnection between adjacent CLB,s
- ✓ Long Line Interconnects.

8. Define ASIC?

Application Specific Integrated Circuits (ASIC) is an integrated circuit designed for a special purpose application.

9. What is antifuse?

- ✓ An Antifuse is an electrically one time programmable two-terminal device with small area and low parasitic resistance and capacitance.
- ✓ An antifuse is normally high resistance ($>100\text{M}\Omega$). on application of appropriate programming voltages, the antifuse is changed permanently to a low-resistance structure($200- 500\Omega$)

10. Compare channeled gate array and channel less gate array

Channeled gate array	Channel less gate array
Only the interconnect is customized	Only the top few mask layers are customized
The interconnect uses predefined spaces between rows of base cells	No predefined areas are set aside for routing between cells
Routing is done using spaces	Routing is done using the area of transistors unused
Logic density is less	Logic density is higher

11. Compare antifuse and SRAM

Antifuse	SRAM
One time programable device	SRAM bits can be programmed many times
Consume lesser area	FPGA → consumes extra area
Low delay, high speed	Very high delay

12. Define FPGA

- ✓ Pre-fabricated silicon devices that comprise of an array of uncommitted circuit elements (logic blocks) and interconnect resources
- ✓ An IC designed to be configured at laboratory by end-user after manufacturing

13. What is macros.

The logic cells in a gate array library are called macros

PART -B

1. Briefly explain in detail about full custom and Semi custom ASIC with its classification.

1) Full-Custom ASICs

- An engineer (expert) designs some or logic cells ,circuits or layout specifically for one ASIC.
- Designer hand draws geometries which specify transistors and other devices for an integrated circuit.
- Involves the creation of a a completely new chip, which consists of about a dozen masks (for the photolithographic manufacturing process).
- Fabrication time from geometry submission to returned chips is at least 6-8 weeks
- There is no existing cell library available to be used for the entire design.
- Full custom ASIC cannot be modified to suit different applications.
- Full-custom design offers the highest performance Fabrication costs are high
- The disadvantages of full-custom design include increased design time, complexity, design expense, and highest risk.
- Eg→Microprocessors,analog/digital (communications), sensors and actuators, and memory (DRAM).

2)Standard-Cell-Based ASICs

- Designer uses a library of standard cells. (AND gates,OR,MUX).
- Designer does not have to be a VLSI expert.
- Manufacturing lead time is about 2-4 weeks.
- The predesigned logic cells are known as standard cells.
- An automatic place and route tool does the layout.
- Design time can be much faster than full custom because layout is automatically generated.
- The Standard cells areas are called flexible blocks.Flexible blocks in CBIC are built of rows of standard cells.
- This is used in combination with larger predesigned cells,like microcontrollers or microprocessor.These are called megacells.
- Megacells are also called megafunctions , full-custom blocks , system-level macros(SLMs), fixed blocks , cores , or Functional Standard Blocks (FSBs)
- Standard cells can be placed anywhere on the silicon.
- Standard cells are designed to fit together like bricks in a wall.
- Power and ground buses (VDD,VSS,GND) run

standard-cell
area



horizontally on metal lines inside the cells.

- Groups of standard cells fit horizontally together to form rows.
- The rows stack vertically to form flexible rectangular blocks.

Connect a flexible block built from several rows of standard cells to other standard cells blocks .

3)Gate-Array-Based ASICs

- In a gate-array-based ASIC, the transistors are predefined on the silicon wafer.
- The predefined pattern of transistors is called the base array.
- The smallest element that is replicated to make the base array is called the base or primitive cell
- To distinguish this type of gate array from other types of gate array, it is often called a masked gate array (MGA).
- The designer chooses from a gate-array library of predesigned and pre-characterized logic cells.

The logic cells in a gate-array library are often called macros .

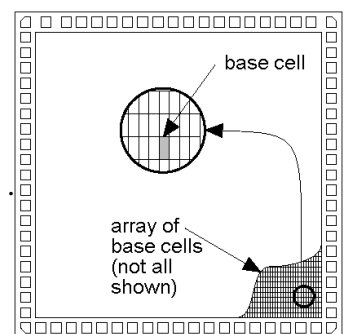
- After validation, automatic placement and routing are typically used to convert the macro-based design into a layout on the ASIC using primitive cells

Types of MGAs:

- Channeled Gate Array
- Channelless Gate Array
- Structured Gate Array
- PLD
- FPGA

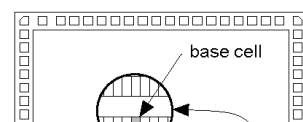
3.1)Channeled Gate Array

- Only the interconnect is customized
- The interconnect uses predefined spaces between rows of base cells .
- Manufacturing lead time is between two days and two weeks.
- A channeled gate array is similar to a CBIC.
- Both use rows of cells separated by channels used for interconnect.
- One difference is that the space for interconnect between rows of cells are fixed in height in a channeled gate array, whereas the space between rows of cells may be adjusted in a CBIC



3.2)Channelless Gate Array

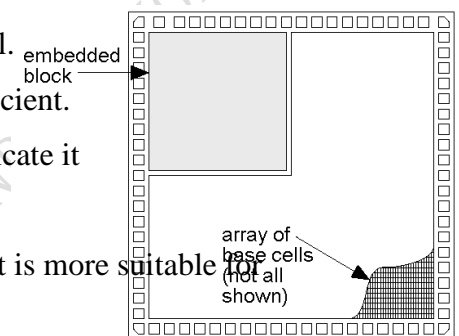
- Channelless gate array architecture is widely used.



- The routing on a channelless gate array uses rows of unused transistors
- Only some (the top few) mask layers are customized the interconnect.
- Manufacturing lead time is between two days and two weeks.
- The key difference between a channelless gate array and channeled gate array is that there are no predefined areas set aside for routing between cells on a channelless gate array.
- Routing over the top of the gate-array devices

3.3) Structured Gate Array/ Masterslice/ Masterimage

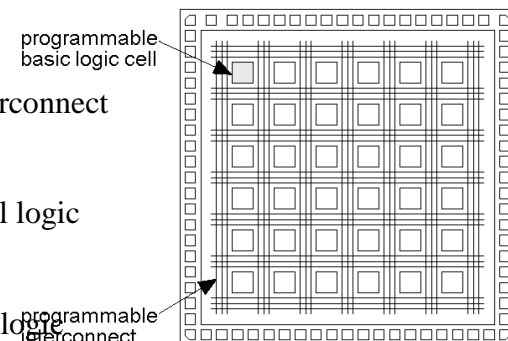
- An embedded gate array or structured gate array combines some of the features of CBICs and MGAs.
- The disadvantages of the MGA is the fixed gate-array base cell.
- This makes the implementation of memory, difficult and inefficient.
- In an embedded gate array we set some of the IC area and dedicate it to a specific function.
- This embedded area either can contain a different base cell that is more suitable for building memory cells, or circuit block of microcontroller.



3.4) Field Programmable Gate Array-FPGA

Features

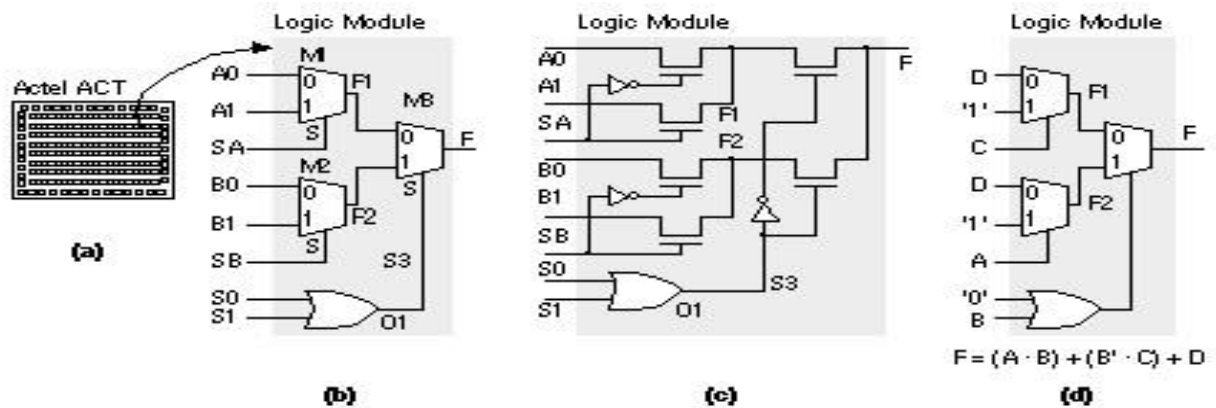
- None of the mask layers are customized
- A method for programming the basic logic cells and the interconnect
- The core is a regular array of programmable basic logic cells that can implement combinational as well as sequential logic (flip-flops)
- A matrix of programmable interconnect surrounds the basic logic cells
- Programmable I/O cells surround the core
- Design turnaround is a few hours



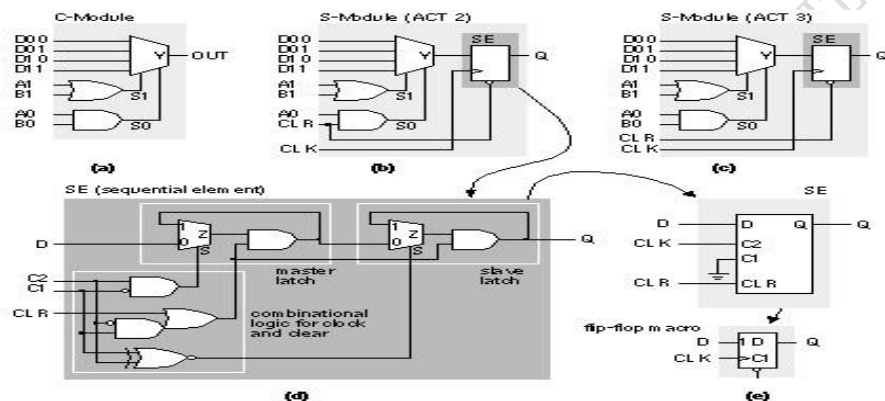
2. With the neat sketch explain the Basic building blocks of FPGA architecture.

1.1) ACTEL FPGA

- ACT1 module has three 2:1 Muxs with AND-OR logic at the select of final MUX and implements all 2 input functions, most 3 input and many 4 input functions.
- Software module generator for ACT1 takes care of all this.
- Apart from variety of combinational logic functions, the ACT1 module can implement sequential logic cells in a flexible and efficient manner. For example an ACT1 module can be used for a transparent Latch or two modules for a flip flop.

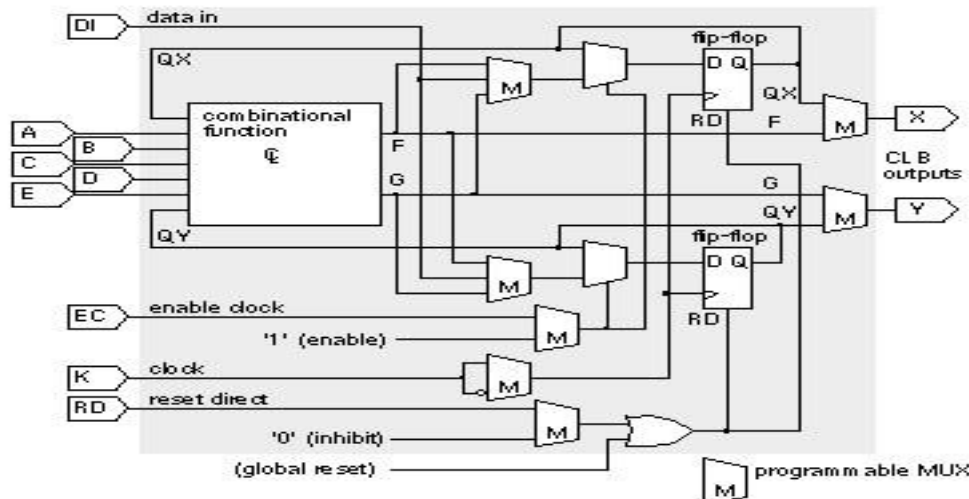


1.2)ACT 2 and ACT 3 Logic Modules



- The ACT 2 and ACT 3 architectures use two different types of Logic Modules, and one of them does include the equivalent of a D flip-flop.
- The ACT 2 C-Module is similar to ACT 1 but is capable of implementing five-input logic functions.
- The use of MUXes in the Actel Logic Modules (and in other places) can cause confusion in using and creating logic macros.
- For the Actel library, setting S = '0' selects input A of a two-input MUX.
- For other libraries setting S = '1' selects input A.
- This can lead to some very hard to find errors when moving schematics between libraries.
- Similar problems arise in flip-flops and latches with MUX inputs.
- A safer way to label the inputs of a two-input MUX is with '0' and '1', corresponding to the input selected when the select input is '1' or '0'.
- This notation can be extended to bigger MUXes

2.1)XC3000 CLB



- The XC3000 CLB, has 5 logic inputs (A E), a common clock input (K), an asynchronous direct-reset input (RD), and an enable (EC).
- Independently connect each of the two CLB outputs (X and Y) to the output of the flip-flops (QX and QY) or to the output of the combinational logic (F and G).
- A 32-bit look-up table (LUT), stored in 32 bits of SRAM, provides the ability to implement combinational logic.
- Eg→To implement the function $F = A \cdot B \cdot C \cdot D \cdot E$
- Set the contents of LUT cell number 31 (with address '11111') in the 32-bit SRAM to a '1'; all the other SRAM cells are set to '0'.
- When you apply the input variables as an address to the 32-bit SRAM, only when $ABCDE = '11111'$ will the output F be a '1'.

Method1

- Split the 32-bit LUT in half to implement two functions of four variables each. choose four input variables from the seven inputs (A E, QX, QY).
- choose two of the inputs from the five CLB inputs (A E); then one function output connects to F and the other output connects to G.

Method2

- Split the 32-bit LUT in half, using one of the seven input variables as a select input to a 2:1 MUX that switches between F and G. This allows you to implement some functions of six and seven variables.

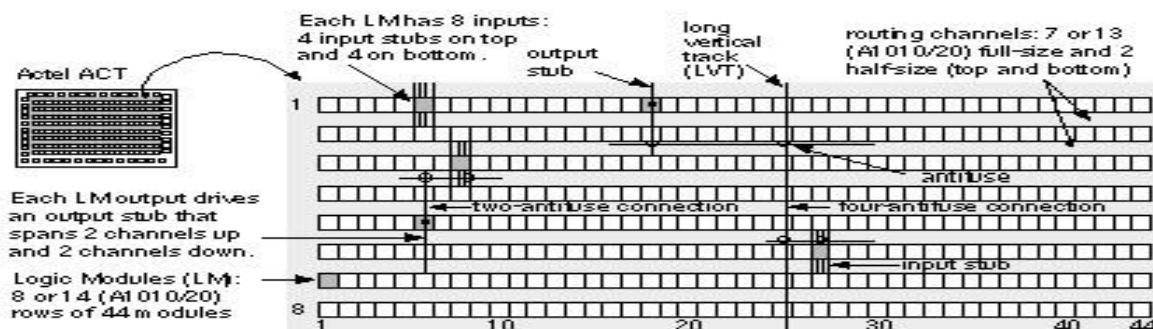
3. Classify the types of FPGA routing techniques and explain.

- All FPGAs contain some type of programmable interconnect .
- The structure and complexity of the interconnect is largely determined by the programming technology and the architecture of the basic logic cell.
- The raw material building the interconnect is aluminum-based metallization, which has a sheet resistance of approximately 50 m W /square and a line capacitance of 0.2 pFcm⁻¹ .
- The first programmable ASICs were constructed using two layers of metal.
- Newer programmable ASICs use three or more layers of metal interconnect.

Types of Interconnecting architectures

1. Actel Interconnect
2. Xilinx LCA
3. XILINX EPLD
4. ALTERA MAX(5000, 7000,9000)
5. ALTERA MAX

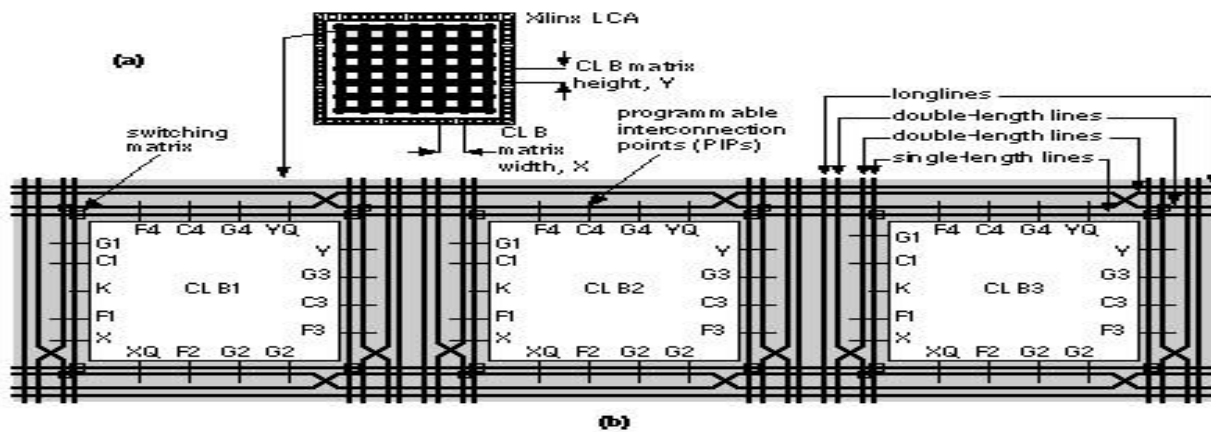
1)Actel ACT



The Actel ACT family interconnect is similar to a channeled gate array.

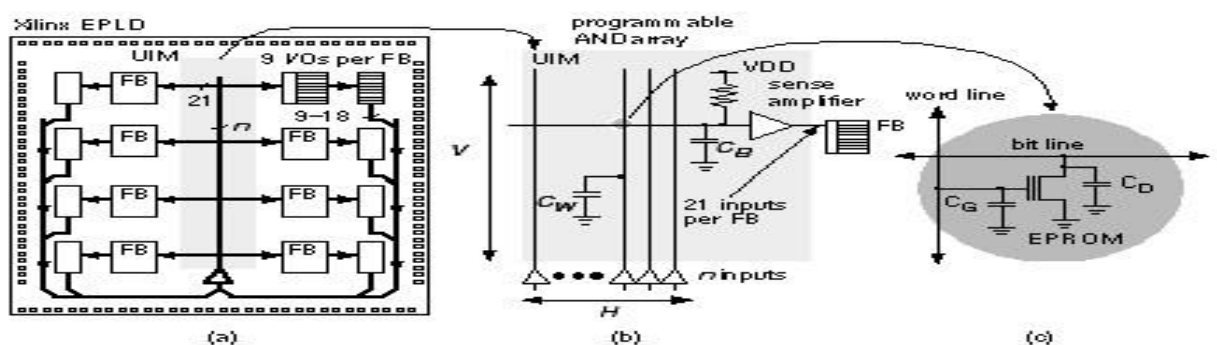
- The channel routing uses dedicated rectangular areas of fixed size within the chip called wiring channels (or just channels).
- The horizontal channels run across the chip in the horizontal direction.
- In the vertical direction there are similar vertical channels that run over the top of the basic logic cells, the Logic Modules. Within the horizontal or vertical channels wires run horizontally or vertically, respectively, within tracks .
- Each track holds one wire. The capacity of a fixed wiring channel is equal to the number of tracks it contains.
- Figure 7.2 shows a detailed view of the channel and the connections to each Logic Module the input stubs and output stubs .

2)Xilinx LCA



- The vertical lines and horizontal lines run between CLBs.
- The general-purpose interconnect joins switch boxes (also known as magic boxes or switching matrices).
- The long lines run across the entire chip. It is possible to form internal buses using long lines and the three-state buffers that are next to each CLB.
- The direct connections (not used on the XC4000) bypass the switch matrices and directly connect adjacent CLBs.
- The Programmable Interconnection Points (PIP s) are programmable pass transistors that connect the CLB inputs and outputs to the routing network.
- The bidirectional (BIDI) interconnect buffers restore the logic level and logic strength on long interconnect paths.

3) Xilinx EPLD

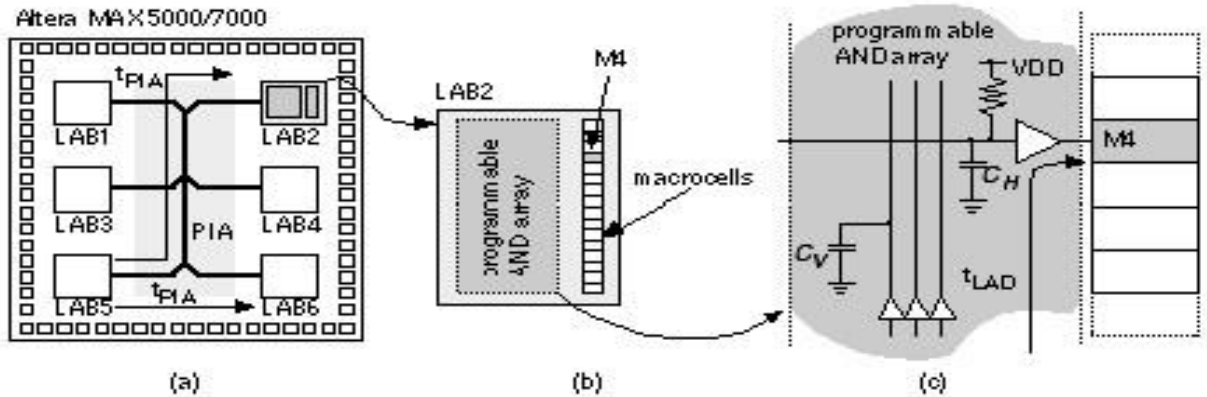


The Xilinx EPLD family uses an interconnect bus known as Universal

- Interconnection Module (UIM) to distribute signals within the FPGA.
- Which uses programmable AND array with constant delay from any input to any output.
- C_G -is the fixed gate capacitance of the EPROM device.
- C_D -fixed drain parasitic capacitance of the EPROM device.
- C_B -variable horizontal bus (bit line) capacitance.
- C_W -is the variable vertical bus (word line) capacitance.

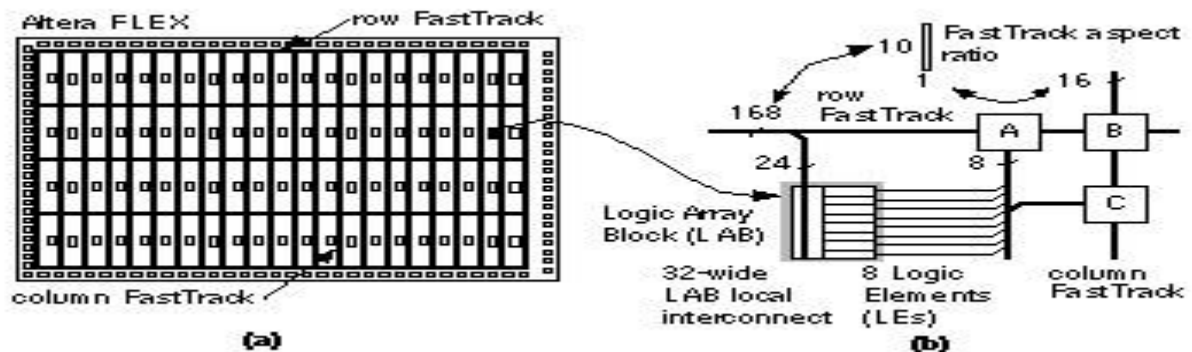
- UIM has 21 output connections to each FB.
- The XC7272 UIM (with a 4x2 array of eight FBs and has 168 (8 x 21) output connections.
- Most of the nine I/O cells attached to each FB have two input connections to the UIM, one from a chip input and one feedback from the macrocell output.

4) Altera MAX 5000 and 7000



- which uses a fixed number of connections over programmable interconnection schemes
- Fixed routing delay.
- Interconnect structure is Simplified and improved speed of the placement and routing software.
- The delay between LAB1 and LAB2 is the same as the delay between LAB1 and LAB6

6) Altera FLEX



- The interconnect used in the Altera FLEX family of complex PLDs.
- Altera refers to the FLEX interconnect and MAX 9000 interconnect by the same name, FastTrack.
- These two are different because the granularity of the logic cell arrays is different.
- The FLEX architecture is of finer grain than the MAX arrays because of the difference in programming technology.
- The FLEX horizontal interconnect is much denser (at 168 channels per row) than the vertical interconnect (16 channels per column). Which creating an aspect ratio for the interconnect of over 10:1 (168:16).
- This imbalance is partly due to the aspect ratio of the die, the array, and the aspect ratio of the basic logic cell, the LAB.